-81dB PSRR regulated cascode fully MOS bandgap reference for power management in RF energy harvesting systems

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Article Info

ABSTRACT

In the midst of technological advance where everything is connected via the internet, IoT is emerging as a potential solution to everything, ranging from health wearables to smart city. An RFEH power management system has promising benefits that could further improve the powering of IoT devices as it has potential for clean energy as well as other advantages which consists of a rectifier, bandgap reference and LDO as the main core. However, the main challenge is supplying clean and low noise power to sensitive circuits such as low power sensors, VCOs and PLLs. A high PSRR bandgap reference that rejects noise at the power supply is needed so that the circuitry powered by RFEH systems would be able to function properly. This paper presents a bandgap with MOS PTAT and CTAT extraction achieving a PSRR of -81dB at a Vref of 0.415V was designed on 130nm CMOS technology targeting IoT RFEH devices that operate at sub-threshold and near-threshold region that exhibits improvement over the base design.

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1. INTRODUCTION

RF energy harvesting (RFEH) is a promising way to scavenge energy from the environment to power up Internet of Things (IoT) sensors and low-power applications. The scaling down of technology nodes also contribute to more low-power devices, making RFEH even more desirable. This is because RFEH offers interesting attributes such as reduced cost and lower periodic maintenance which is especially useful when involving IoT devices in harsh environments that complicate the maintenance process. Apart from that, the lifetime of the storage can be extended [1].

Circuitry reported in literature that can potentially benefit from RFEH include low power sensors such as [2] and SRAM devices [3] which operate at sub-threshold or near threshold are the perfect candidate for RFEH systems. In order to power up low power devices through RFEH, a power management system such as the one shown in Figure 1 can be employed. The power management system for RFEH contains blocks such as an antenna, a matching network, a rectifier, a bandgap reference and an LDO. The power management system works such that RF signal is first collected through the antenna and is fed into a matching network which functions to maximize power transfer and to provide passive amplification.

The signal then passes through a rectifier which converts the RF signal into DC signal. The DC signal is then fed into the LDO to be regulated. The bandgap serves as a reference voltage to the regulator that provides a stable voltage across variations in temperature.
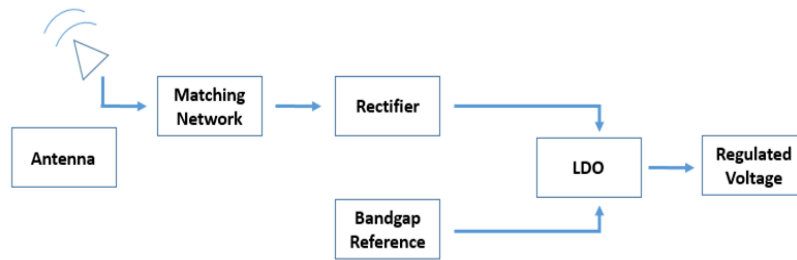
Figure 1. Power management block for RFEH systems

In low power sensors, the accuracy of the functionality may be affected especially since the sensors are required to detect minute levels of changes in stimuli and are therefore very sensitive to noise. The same applies to the VCO where it is particularly sensitive to noise in the power supply. Any noise injected through the power supply will affect the control voltage of the VCO to operate optimally, resulting in jitter in the PLL affecting the reliability of clock generation [4]. An example of a near-threshold PLL is described in [5]. Low power sensors, VCOs and PLLs and are an integral part of IoT as they are used for sensor applications and clock generation respectively, it is of paramount importance that these blocks are supplied with clean power supply. Since bandgap reference is one of the essential blocks in determining the performance of the power management system, this work discusses the block in detail.

The function of a bandgap reference circuit is to provide a stable voltage reference over temperature variations. This is done by exploiting the temperature dependent characteristics of the BJT. Traditional bandgap circuits have a standard voltage reference of approximately 1.2V which is the bandgap voltage of silicon. This is however not achievable at power supply lower than 1.2V. As such, some modern bandgaps have moved to sub-1V architectures such as [6] that can scale down the reference voltage by means of resistor ratio whenever needed and can support lower supply voltages. An ideal bandgap circuit should have a good temperature coefficient, high PSRR and good accuracy [7]. However, achieving all the mentioned specifications will possibly incur tradeoffs in terms of minimum supply voltage, area, power consumption or output swing among other things. This work aims to focus on power supply rejection ratio (PSRR) since it is an important specification in RFEH power management system.

Papers such as [8], [9], and [10] focus on the PSRR specification of bandgap reference. The techniques involved to increase PSRR involve voltage regulation of the transistor [8], cascoding transistors [9] and combination of cascode and voltage regulation [10]. Although these circuits will result in high PSRR, they exhibit weakness such as requiring relatively high-power supply, making it unsuitable for low power applications [8] and also cannot obtain a reference voltage of lower than 1.2V [9] which is crucial for circuits that operate in sub-threshold or near-threshold. In [10], high PSRR can only be obtained at higher voltage references, at near-threshold and sub-threshold voltage the PSRR degrades because of the usage of BJT which consumes a lot of voltage headroom at supply voltage of 1.2V.

In this work, a bandgap circuit is presented that improvises the techniques in previous work, particularly the regulated cascode [10] so that a high PSRR can be achieved even at low voltage references. This paper will be organized as follows. Section 1 will discuss on the fundamentals of bandgap reference. In Section 2, the proposed work will be discussed. Section 3 will discuss on the results of the simulated circuit and lastly the work will be concluded in Section 4.

2. PROPOSED DESIGN
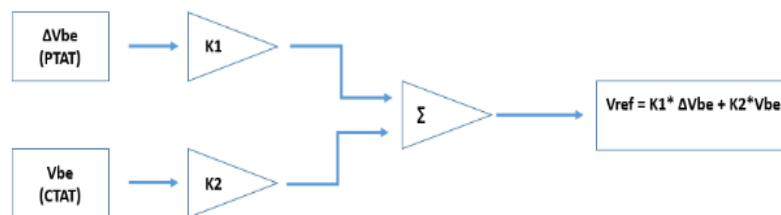By adding both PTAT and CTAT, a stable voltage can be obtained as depicted in Figure 2.

Figure 2. Basic operation of bandgap reference circuit obtained by summing PTAT and CTAT

In order to obtain a stable reference voltage over temperature variations, a circuit that produces PTAT and CTAT characteristics must be designed. PTAT (Proportional to Absolute Temperature) as its name implies, generates a voltage that is increasing somewhat linearly with respect to temperature.

As shows in 1 through 4, Vt is the thermal voltage, Ic is the collector current of BJT, Is is the reverse saturation bias current and VG0 is the bandgap voltage of silicon. As can be seen from 1 and 2, the term ΔVbe has a positive dependency, hence giving a positive slope when differentiated with respect to temperature. CTAT (Complementary to Absolute Temperature) on the other hand generates a voltage that is decreasing with temperature. This phenomenon is captured in 3 and 4 and when differentiated with respect to temperature has a negative slope. As such, the authors in [10] used a regulated cascode technique as can be seen in Figure 3(a), where the current mirror is cascoded to increase the output resistance (rds) of the transistor at the output stage.

$$\Delta V_{be} = V_t ln \left(\frac{I_{c1} I_{s2}}{I_{c2} I_{s1}} \right) = V_t ln(n) \tag{1}$$

$$\frac{\partial \Delta V_{be}}{\partial T} = \frac{k}{q} = +0.085 mV/°C \tag{2}$$

$$V_{be} = V_{G0} - \frac{kT}{q} ln \left(\frac{I_c}{I_s} \right) \tag{3}$$

$$\frac{\partial V_{be}}{\partial T} = -\frac{k}{q} ln \left(\frac{I_c}{I_s} \right) = -2 mV/°C \tag{4}$$
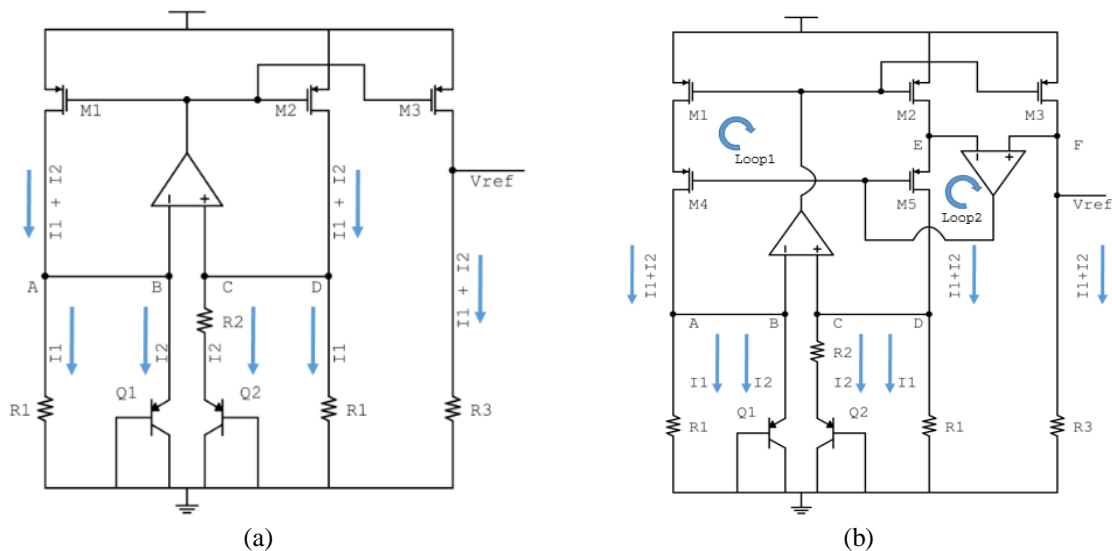

Figure 3. (a) Regulated cascode bandgap reference for increasing PSRR [10]
(b) Traditional sub 1-V bandgap reference [6]

The proposed architecture can be seen in Figure 4 where the BJTs in [10] is replaced by MOSFETs in diode connected configuration, whereby the gate source voltage is equal to the drain source voltage. The rest of circuit is similar to [10] in terms of functionality.
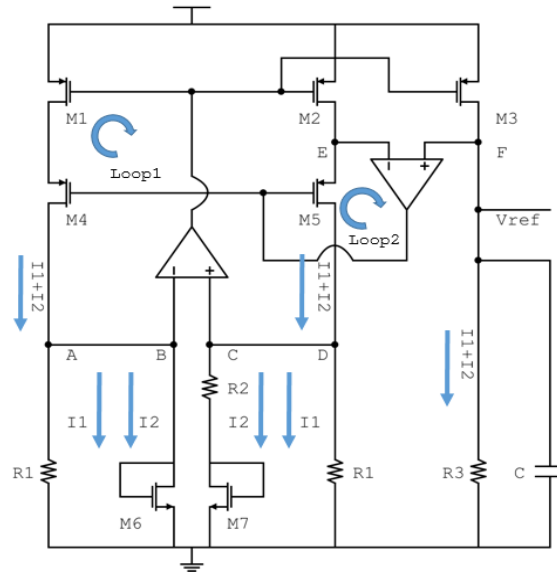
Figure 4. Proposed bandgap architecture with CMOS as PTAT and CTAT generator

The proposed design uses the conventional sub 1-V bandgap design by [6] to allow for lower reference voltage than 1.2V. Figure 3(b) shows the conventional [6] circuit. As can be seen the circuit is made up of BJTs Q1 and Q2. Q1 provides the CTAT property of the BJT as per 1. Q2 provides the PTAT property of the BJT as per 2. The op amp is used in a negative feedback configuration to set the voltage at nodes A, B, C and D to be the same. This is done so that the PTAT characteristics can be obtained from the difference of the Vbe1 and Vbe2 which is ΔVbe.

$$V_{ref} = \frac{R_3}{R_1}V_{be} + \frac{R_3}{R_2}\Delta V_{be} \tag{5}$$

The output of the op amp goes to the gate of a current mirror made up transistors M1 and M2. The op amp in negative feedback controls the gate voltage of M1 and M2 such that the voltage at nodes A, B, C and D are equal. The sum of the current in each branch is the then mirrored to the output via the current mirror M3. Since the current of I1 and I2 are known, Vref can be expressed as per 5.

Authors in [10] proposed a modification to the [6] architecture cascode in order to increase the PSRR of the bandgap. The effects of channel length modulation in smaller technology nodes causes the output resistance to be smaller.

$$\frac{V_{ref}}{V_{dd}} = (1 - PSRR_{A1})/(g_m.(r_{ds}||R_3).(1 + A_{v2})) \tag{6}$$

$$V_{ref} = V_{be} + V_{sd4} \tag{7}$$

Furthermore, the transistors M4 and M5 are regulated by op amp 2 in negative feedback configuration, further boosting the output impedance and therefore the PSRR as given by 6, where PSRR is the PSRR of the first op amp, gm is the transconductance of M3, rds is the output resistance of the of the M3 and Av2 is the gain of the second op amp. When in negative feedback configuration, the op amp will set nodes E and F to be equal, by increasing rds.

From the equation, it is apparent that when rds increases, the Vref over Vdd term, which indicates the presence of noise at the output becomes small, hence a better PSRR can be obtained. From the circuit perspective, the noise from power supply will be suppressed because it is travelling through a high impedance path set by the boosted output impedance, hence increasing the PSRR.

The problem with this architecture is that the second loop which contributes to the increase in PSRR, only works for a certain range of voltage references. The second loop only functions, as long as the condition in 7 holds true. The reason for this degradation of PSRR versus Vref is because of the usage of BJT for the PTAT and CTAT generation. This is because of the BJT contributing a voltage drop of approximately

0.7V, the loop will fail to increase the output impedance when a lower voltage reference than 0.7V is needed, especially in the case of powering low power devices

That operate at near-threshold or sub-threshold. For example, if a Vref of 0.4V is needed, the 0.7V of the BJT will result in a non-positive Vsd1 which is not possible, causing the loop to fail.

The proposed architecture adopts the same circuit as [10] but extracts the CTAT and PTAT behavior from MOSFETs instead of BJTs. This is because as previously mentioned, the BJT is contributing to a 0.7V voltage drop, consuming headroom for other transistors to saturate causing the second loop to fail. The aim is to extract the PTAT and CTAT behavior of MOSFETs which exhibit the same temperature dependency characteristics as the BJT. Unlike BJTs, the voltage drop across a MOSFET (Vds) in diode configuration can be controlled by sizing transistors to be in weak inversion region whereas the voltage drop across BJTs are somewhere around the order of 0.6V to 0.7V.

The CTAT is obtained through transistor M1 while PTAT is obtained through the difference of Vds across the resistor R2. In order to obtain the CTAT and PTAT behavior of MOSFETs, transistors M1 and M2 are sized to operate in weak inversion region.

$$V_{GS} = n.V_T.\ln\left(\left(\frac{I_{DS}}{I_{D0}}\right).\left(\frac{L}{W}\right)\right) \tag{8}$$

$$\Delta V_{GS} = n.V_T.\ln\left(\frac{I_{DS2}}{I_{DS1}}.\frac{L_2 W_1}{L_1 W_2}\right) \tag{9}$$

$$V_{ref} = \frac{R_3}{R_1}V_{DS} + \frac{R_3}{R_2}\Delta V_{DS} \tag{10}$$

$$V_{ref} = V_{DS1} + V_{SD4} \tag{11}$$

The equation for current through a transistor operating in weak inversion region is given in 8 and 9. Following the same derivations as the BJT, the CTAT and PTAT can be obtained. The Vref can then be expressed as per 10, where the Vds can be controlled to be in the range of 0.2 to 0.3V. By having lower Vds the second loop can be sustained even at lower Vref. As shows in 10 expresses the Vref in terms of PTAT, CTAT and resistive ratios whereas 11 shows how the second loop will react in response to the voltage drop of the MOSFET, in terms of Vref. A capacitor was added at the output to further suppress the noise coming from the power supply. Figure 5 shows the op amp used in the proposed bandgap circuit.
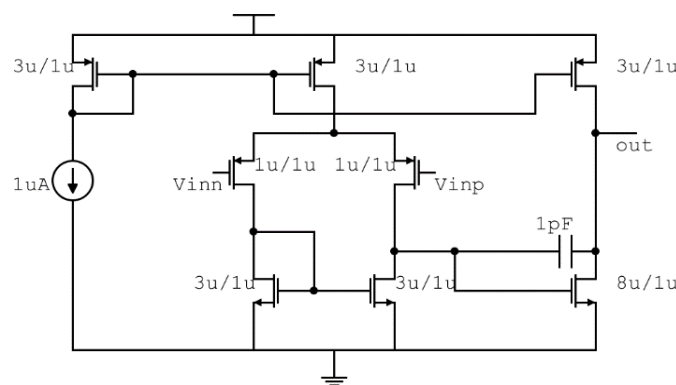

Figure 5. P-input 2-stage op amp for negative feedback loops in proposed bandgap circuit

It is a basic p-input 2-stage op amp with differential input stage and an output push pull stage. A p-input op amp was chosen because it has a low (input common-mode range) ICMR range than its n-input counterpart. Since the Vds of the CTAT transistor is chosen to be 0.2V a p-input op amp was used. In order to provide high gain to reduce error as per the Barkhausen criteria, a two-stage p-input op amp was used for both loops. Table 1 describes the values for the components in the proposed bandgap circuit shown in Figure 4.

Table 1. Device Values

Device	Values
M1	3u/1u
M2	3u/1u
M3	3u/1u
M4	10u/0.13u
M5	10u/0.13u
M6	30u/0.13u
M7	30u/0.13u (m=8)
R1	400kΩ
R2	80kΩ
R3	300kΩ
C1	8.5pF

For sizes of transistors M1-M3, in order to mitigate channel length modulation, a big length of 1u was chosen. The width 3u was chosen such that the current mirror transistors are in saturation for better current mirroring and high gain. Transistors M4 and M5 have an aspect ratio of 10u/0.13u to ensure the second loop is functioning correctly, hence operating in sub-threshold region. Transistors M6 and M7 were swept such that the voltage drop across the CTAT is low enough so that the second loop will function correctly, which is 0.2V and the value was found to be 30u and 240u respectively, with the multiplier of M7 as 8 for better layout matching purposes. These transistors also operate in sub-threshold region. The values of R1, R2 and R3 are calculated such that a Vref of 0.415V can be obtained, as per 8-10. An output filtering capacitor of 8.5pF was added to keep the PSRR under -10dB.

3. RESULTS AND ANALYSIS

Figure 6 shows the comparison between the PSRR of [10] and the proposed circuit at Vref = 0.415V. As can be seen, the PSRR of the proposed circuit is better than [10] by 40.7 % at DC which is -81dB as compared to -33dB of that in [10]. This is because as mentioned earlier, the second loop ensures that the voltage E and F are the same at 0.415V by increasing the impedance at output. The PSRR deteriorates and has low bandwidth because of the fundamental tradeoff between the high DC gain and bandwidth. In order to prevent the peak from deteriorating further at high frequencies, a capacitor was added at the output increasing the PSRR. Figure 7 shows the PTAT and CTAT nature of the MOSFET relative to temperature when swept from -40˚C to 85˚C
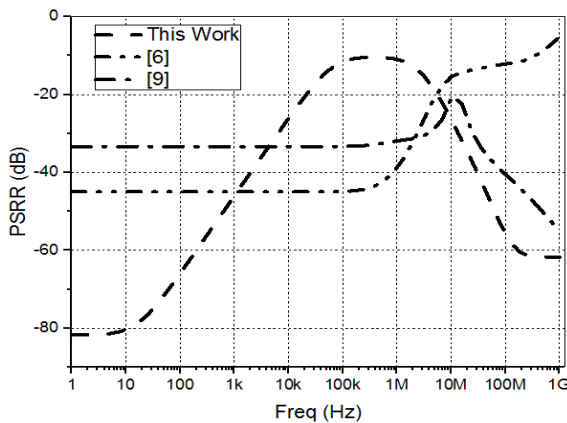

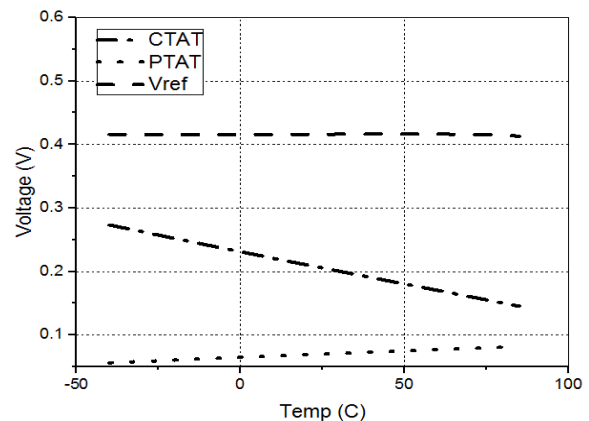Figure 6. PSRR performance of the proposed work and benchmark circuits with respect to frequency

Figure 7. CTAT, PTAT and output reference voltage across temperature from -40 to 85 ˚C

The summation of both PTAT and CTAT to get the reference voltage can also be seen in Figure 7. As can be seen, the proposed bandgap reference circuit exhibits a variation of only 3.261mV which translates to only 0.008%. Figure 8(a) and 8(b) shows the loop gain and stability for loop 1 and 2 respectively.
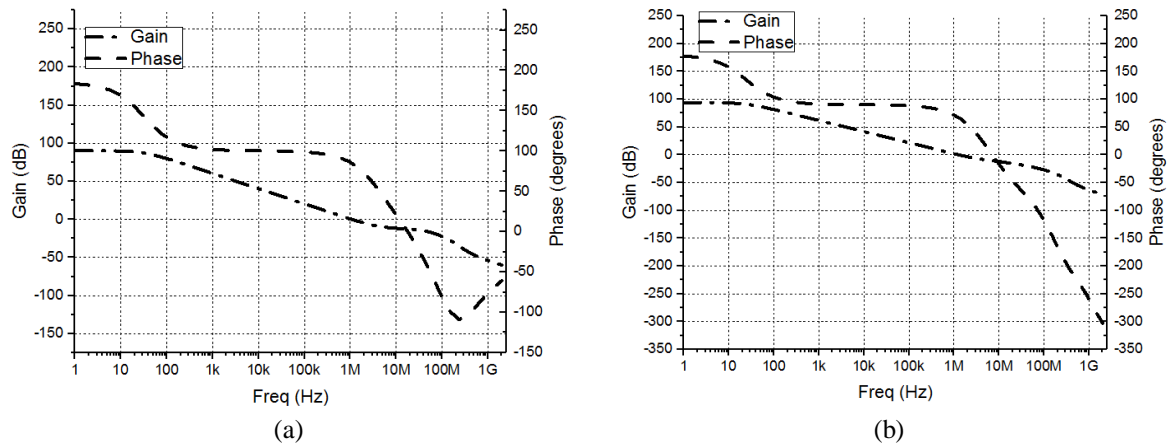
(a)   (b)

Figure 8. (a) Loop gain and phase for loop 1 with gain of 90dB and phase margin of 66.9˚ (b) Loop gain and phase for loop 2 with gain of 94dB and phase margin of 73.9 ˚

In order to make sure the voltage at nodes A, B, C, D for loop 1 and nodes E, F for loop 2 the same, the loop gain must be high. As can be seen, loop 1 has a gain of 90dB with 66.9˚ phase margin while loop 2 has a gain of 94dB and 73.9˚ phase margin. It can be concluded that both loops have high gain and are stable. Comparison between previous works as shown in Table 2.

Table 2. Comparison Between Previous Works

	This Work	[10]	[11]	[12]	[13]
Technology	130nm	130nm	180nm	180nm	180nm
Power Supply	1-1.2V	1.2 - 4V	0.45 – 1.8V	0.8-1.6V	0.9-2V
Vref	0.415V	0.85V	0.118V	0.477V	0.411V
Temperature Range	-40 – 85 ˚C	-40 – 125˚C	-40 – 125 ˚C	-20 – 120 ˚C	-40 – 125˚C
Temperature Coefficient	57.7ppm/ ˚C	10 ppm/ ˚C	63.6 ppm/ ˚C	51.2 ppm/ ˚C	33.7 ppm/ ˚C
PSRR	-81dB @ DC -11.7dB @100kHz	-130dB* @DC -110dB* @100kHz	-44.2dB @100Hz	-50dB @100Hz -19dB @1MHz	-61dB @ 10Hz -46dB @ 1MHz
Current/ Power Consumption	10.17uA	50uA	0.032uA	46.25nA	94.44nA

4.   CONCLUSION

A bandgap with MOS PTAT and CTAT extraction achieving a PSRR of -81dB at a Vref of 0.415V was designed on 130nm CMOS technology targeting IoT RFEH devices that operate at sub-threshold and near-threshold region that exhibits improvement over the base design. Future work involves designing a start-up circuit to ensure that the bandgap operates at its optimal DC operating point, a rectifier to convert RF signal to DC, a matching circuit for maximum power transfer and an LDO to regulate the voltage of the rectifier. A layout of the proposed circuit will be designed, and post-layout verification will be carried out as a proof of concept of the RFEH system.

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Fakhrul Zaman Rokhani received the B.S. degree in University of Technology Malaysia, and the M.S. and Ph.D. degree from the University of Minnesota, USA. He was with Intel Penang Design Center as visiting professor designing chipset for Intel Core i3/i5/i7 processor on 32nm Intel process technology, was with Huawei Technologies for CEO coaching program, visiting scholar at the ASIC & Systems State Key Lab in Fudan University, China, visiting assistant professor at Al-Neelain University, Sudan, visiting professor at Celal Bayar University, Turkey and engineer at MIMOS. His current research interests include designing smart systems and integrated circuits, and sensors for biological application. He has published more than 20 journals, 41 conference proceedings, 1 chapter in book and 1 patent pending. He has secured more than RM500k public grants and more than RM2 million private grants from industry including cash and in-kind, in which he leads as a principal investigator. His research work has been recognized with several awards locally and internationally. He serves as an Editor-in-Chief for IEEE CASS (M) newsletter and associate editor for IEEE CASS society newsletter, past chair for IEEE Consumer Electronics (M) Chapter, executive committee in the IEEE CASS (M) Chapter and was a Treasurer for the IEEE GOLD. He serves on the technical program committees and publication chair for many flagship IEEE conferences.

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