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Design of on-chip temperature-based digital signal processing for customized wireless microcontroller

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ABSTRACT

Dramatic rises in power density and die sizes inside system-on-chip (SoC) design have led to the thermal issue. High temperatures or uneven temperature distributions may result not only in reliability issues, also has become the biggest issue that can limit the system performance. This paper presents the design and simulation of a temperature-based digital signal processing unit for modern system-on-chip design using the Verilog HDL. This design provides continuous monitoring of temperature and reacts to specified conditions. The simulation of the system has been done on Synopsys Software. The result showed that temperature monitoring process is within the temperature range due to the incorporation of an interrupt-based system and with an advantage of minimum chip area required.

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1. INTRODUCTION

The thermal issue become one of an inevitable factor in contemporary system-on-chip (SoCs) due to the continuous increase in the integration density and power consumption of SoC devices. The dissipated power in SoC devices is manifested in the form of heat. Rise in heat density creating vast difficulties which can lead to the serious thermal problem even though in low power applications.

To describe the relationship between power consumption and junction temperature, a first-order expression can be expressed as:

$$T_j = T_a + P_{chip}\, x\, R_{ja} \tag{1}$$

Where Ta is the temperature of the ambient environment, Pchip is the total power consumption inside the chip, Rja is the junction to ambient thermal resistance and Tj is the derived junction temperature. Rja can be modeled as the series resistance from junction to ambient in different parts of the chip. Analogous to electrical resistance, thermal resistance can be defined as:

$$R = \frac{L}{k\, x\, A} \tag{2}$$

Where k is the material's thermal conductivity, L is the length and A is the cross-sectional area of the conducting path.

Substituting Equation (2) into Equation (1), we get:

$$T_j = T_a + P_{chip}\, x\, \frac{L}{k\, x\, A} \quad (3)$$

Therefore, Tj is related to the ratio between Pchip and A at which the power density of the chip is defined [1].

The temperature of the chip is also directly proportional to the voltage and clock frequency. The perpetual increase of the operating frequency increases the density of dissipated power [2]. As power consumption, P is directly proportional to the operational frequency, f by the following equation:

$$P = c.\ V2.\ f + Ps \quad (4)$$

Where c is scaling constant with the dimension of capacitance (F). V is an input voltage and Ps is the static power dissipation which is the power at a zero clock frequency [3].

From this equation, we can identify that if we want to decrease the frequency or voltage, the power into the chip also would decrease, as well as the power dissipated as heat. Meanwhile, by looking at the voltage into the chip, we can see it has a quadratic relationship to the power. Thus, any decreases in voltage have a greater effect on the power than the linear relationship of the clock.

Moreover, clock frequency has a linear relationship to the power consumed by the chip. By lowering the clock frequency, the processor runs slower, the processor executing fewer instructions in a given time period and therefore decreasing the power as needed.

Local overheating in one spot of a high-density circuit as in Figure 1 such as high-speed mixed-signal circuits, can cause a whole system to crash due to clock synchronization problems, parameter mismatches or other coefficient changes due to the uneven heat-up on a single chip [4,5].

Overheating can have effects on a microprocessor. When transistors heat up, more current will pass through the device. High currents will burn out transistors in a processor, ruining the device [6]. Furthermore, transistor performance will decay with increasing temperature as in the graph in Figure 2.

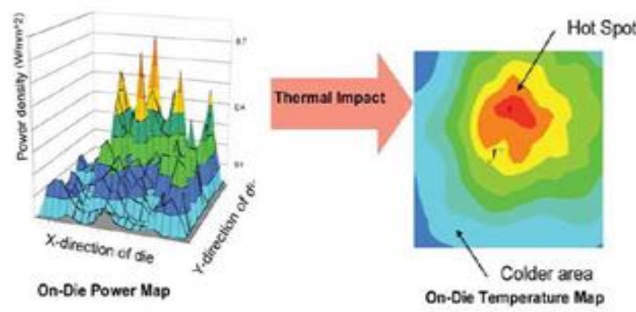

Figure 1. Hotspot of the high-density circuit[1]

The rapid increase in temperature can affect several aspects of the circuit design;

(1) The carrier mobility of a transistor decreases with increasing temperature at which can lower the drive current and leads to increased delays [7].
(2) Large spatial variations in power consumption caused the unevenly distributed heat at different locations can make performance analysis difficult. Increasing in temperature also critical to the design of mixed signal and analog ICs as they are more sensitive to temperature [1].
(3) Higher junction temperature reduces the mean time to failure (MTTF) for the devices, which has a large impact on the reliability of the overall system [8].

Consequently, thermal considerations should become one of the important parts of the design process. In this research, we are developing a temperature-based digital signal processing IP circuit (TDSP) that can provide continuous monitoring of temperature in SoC and reacts to a specified condition. Moreover, this research covers Verilog HDL and design of a temperature-based digital signal processing unit for an on-chip temperature monitoring system using Synopsys software. This circuit is optimized for architecture and circuit implementation to fit system-on-chip designs. Therefore, an interrupt-based system will be

implemented. Given the above considerations, an architecture based on the previous research [10] with significant architecture enhancements is proposed.

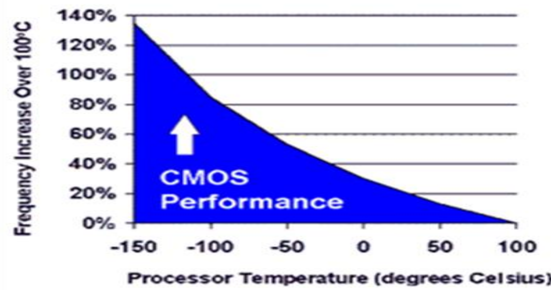

Figure 2. Frequency vs Temperature[9]

2. RESEARCH METHODOLOGY

From this research, the dynamic thermal management is the best option to be used in the development of the temperature-based digital signal processing unit. However, the system needs to be altered to meet the specification needed in a customized Intel wireless microcontroller. Based on the previous research [9], the simulation is done by using the Altera Quartus II software and successfully implemented on FPGA DE2-70 board. For this paper, the simulation is done using the Synopsys software and the Technology Library that will be used is Silterra CMOS 0.18 μm Technology Library. In summary, the process steps involved in the development of temperature-based digital signal processing unit is depicted in Figure 3.

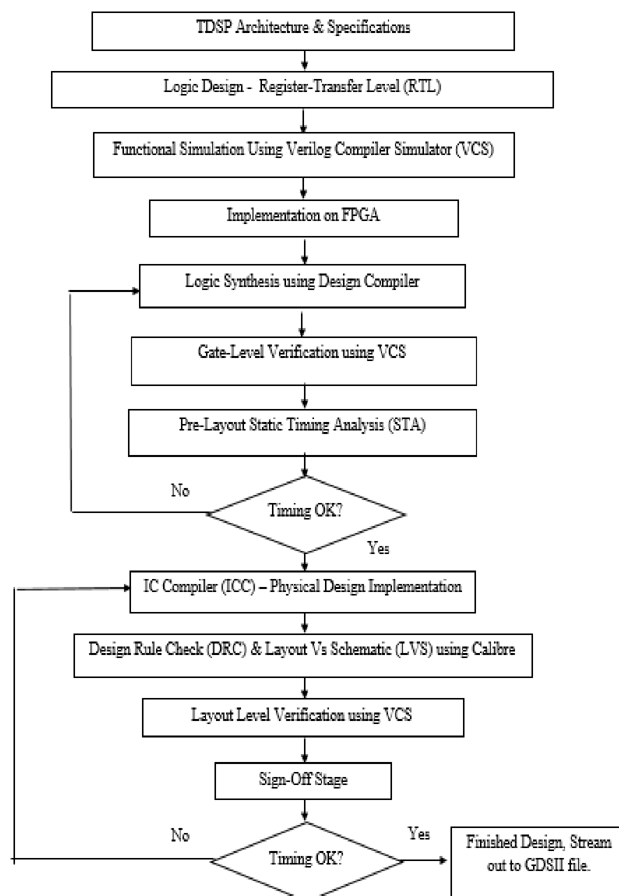

Figure 3. Design methodology

Firstly, after finished designing an architecture and source codes for TDSP, the functional simulation will be done using Synopsys Verilog Compiler Simulator (VCS). Later, to check the functionality and flexibility of the system, TDSP will be implemented to DE2-70 FPGA board. Next, the logic synthesis will be done using Synopsys Design Compiler. Gate level verification is done to check for any timing violation. If no timing violations, continue with physical design implementation using Synopsys IC Compiler. After finished with IC Compiler up until routing phase, proceed with DRC and LVS using Calibre to check for any errors. Lastly, proceed with Sign-Off Stage, consist of Layout Level Verification and Post Layout STA to check the timing violations. If no timing violations, the design is ready to tape-out.

3. PROPOSED ARCHITECTURE

In this section, the architecture of TDSP and its specification will be discussed.

3.1. Block Diagram of TDSP

The block diagram of the temperature-based digital signal processing circuit is shown in Figure 4. The block diagram consists of seven sub-modules

3.2. Function

The function of each sub-modules is described in details in this sub-section.

a. *Interface Register*: This unit control the input data received and providing an input interface synchronously to prevent an error in receiving data
b. *Counter*: This unit used to count to 8 clock cycles in order to receive an input from ADC.
c. *Voltage to Temperature Module*: This unit contains a look-up table to convert the input ADC which is in voltage value into the corresponding temperature value in Celsius (˚C).
d. *Programmable Watchdog Unit*: This unit used to monitor the temperature from the temperature sensor and react to specific temperature ranges.
e. *Interrupt Generator*: This unit provides data outputs that are read by the system CPU, like temperature value and interrupt types.
f. *Output Converter*: This unit convert the output into [31:0] bit form (including temperature value, interrupt low, interrupt high).
g. *Function Controller*: This unit controls the interaction between the system and the CPU.

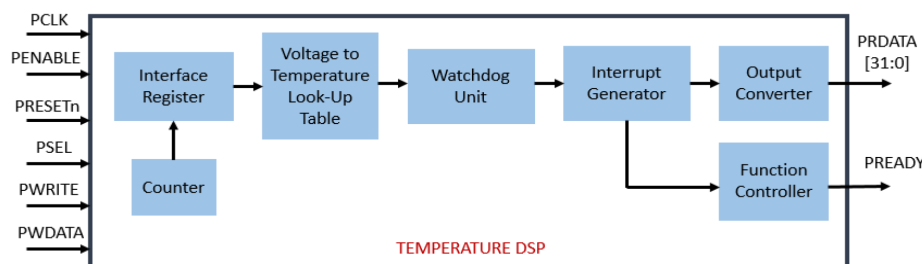

Figure 4. Block Diagram of TDSP

4. ARCHITECTURE ON AMBA BUS

The full chip integration for TDSP system is based on APB Bus Specification as in Figure 5. TDSP will use the AMBA bus protocol as their bus interface because the microcontroller will use the Advanced Microcontroller Bus Architecture (AMBA) bus protocol. The TDSP interface needs to match with Advanced Peripheral Bus (APB) specification, to easily interface the IP with the microcontroller. APB is part of the AMBA hierarchy of buses. It is optimized to reduce the complexity of interfacing and minimalize the power consumption.

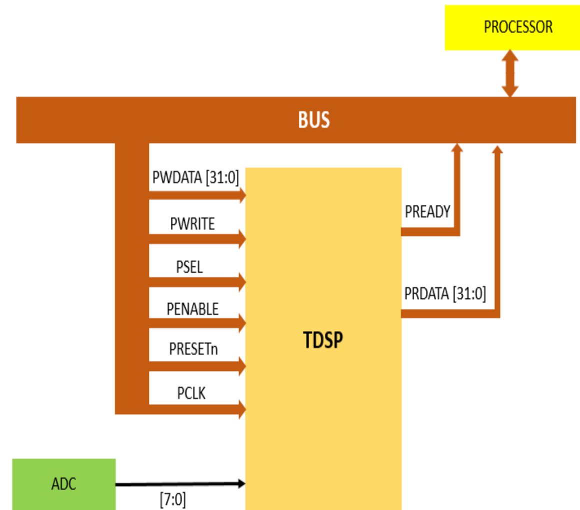

Figure 5. Full Chip Integration of TDSP

The ADC will convert a voltage from temperature sensor into equivalent 8-bit digital voltage. These 8-bit inputs are applied to TDSP where TDSP will monitor the input from ADC and also reference temperature from the host (if available) inside the system and implement the interrupt-based system if the condition needed. The programming in TDSP is done by Verilog HDL language and that builds TDSP system module.

5. RESULT & DISCUSSION

RTL level simulation is generated by Verilog Compiler Simulator (VCS) in Synopsys software. The RTL is the lowest level representation of circuitry from Synopsys software. The RTL generated for TDSP is shown in Figure 6. Meanwhile, the VCS simulator generates the output waveform corresponding to the input change of ADC or reference temperature on simulation to check the functionality of the system. This simulation is executed by random values chosen in inputs. The waveform simulation is shown in Figure 7.

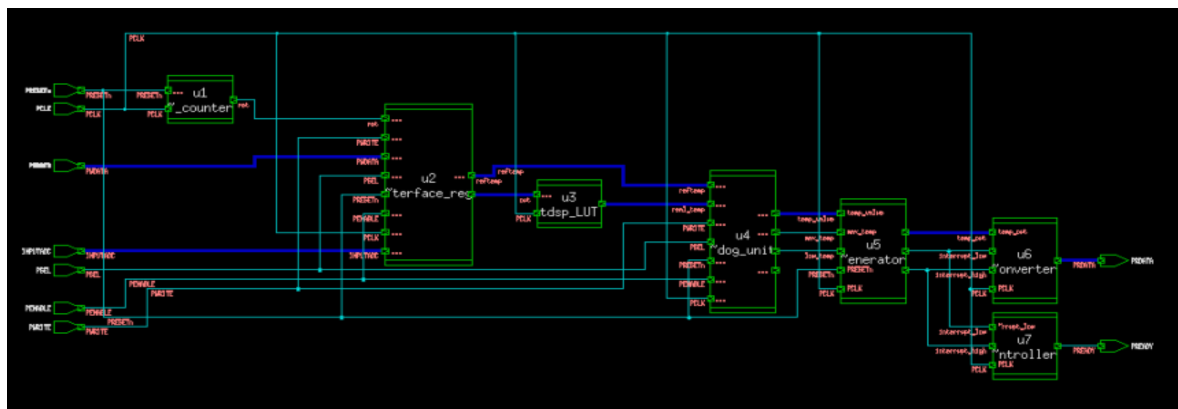

Figure 6. RTL Simulation of TDSP

Based on Figure 7, from 0 ns – 2000 ns, TDSP will receive 8-bit inputs from ADC, which is in decimal input ‘1’. After monitoring process, no interrupt is produced at PRDATA is 32’h0000_0000. This happens because the PRESETn is in active low mode.

Meanwhile, from 2000 ns – 2500 ns, there are slightly delay in the temperature monitoring to begin after the system has been reset. The real monitoring process starts from 2500 ns for the new input value from

the ADC. From 4300 ns – 6000 ns, TDSP received 8-bit inputs from ADC, in the decimal input of ‘37’. After monitor the real value in the look-up table, the temperature turns out to be in an average-temperature range. Thus, no interrupt is produced at PRDATA. TDSP will only send the current temperature value to CPU through the PRDATA output signals.

From 6000 ns – 8000 ns, TDSP received 8-bit inputs from ADC, in the decimal input of ‘43’. After monitor the real value in the look-up table, the temperature turns out to be in the high-temperature range. TDSP will trigger the 8 bits interrupt in PRDATA.

Lastly, from 8000 ns – 10000 ns, TDSP will receive an input, reference temperature from the host, through PWDATA signal. The inputs pin from the AMBA such as PENABLE, PWRITE, and PSEL will be triggered in order for TDSP to receive an input from PWDATA input signal. The reference temperature will be set by the host as the highest temperature. Thus, after the reference temperature is set, the reference temperature will be compared to the real temperature received from the ADC. TDSP can provide the continuous temperature monitoring process as long as the data received from ADC. Figure 8 shows the gate level schematic on one of the sub-modules in TDSP after verification of the gate is completed.

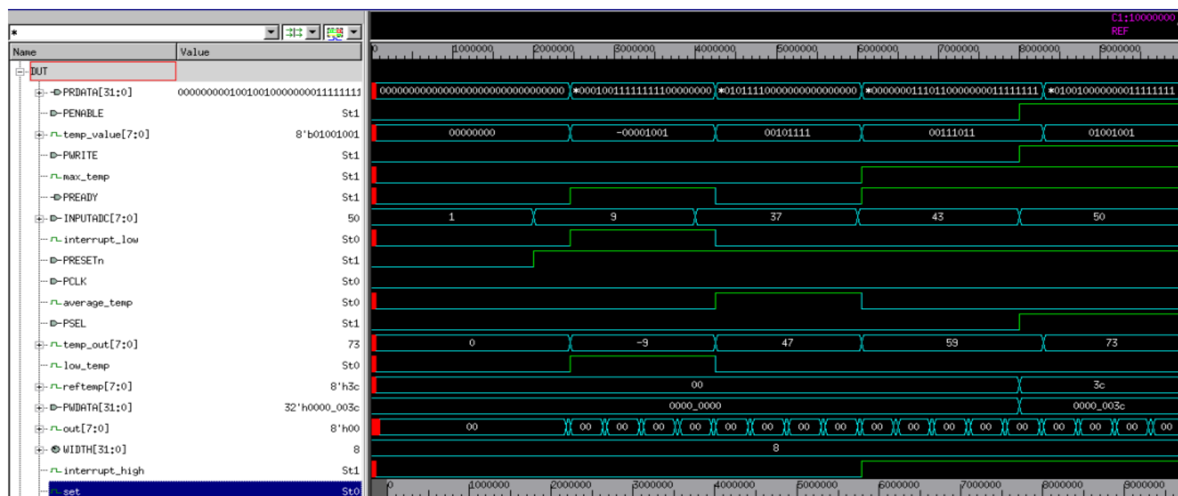

Figure 7. RTL Simulation of TDSP

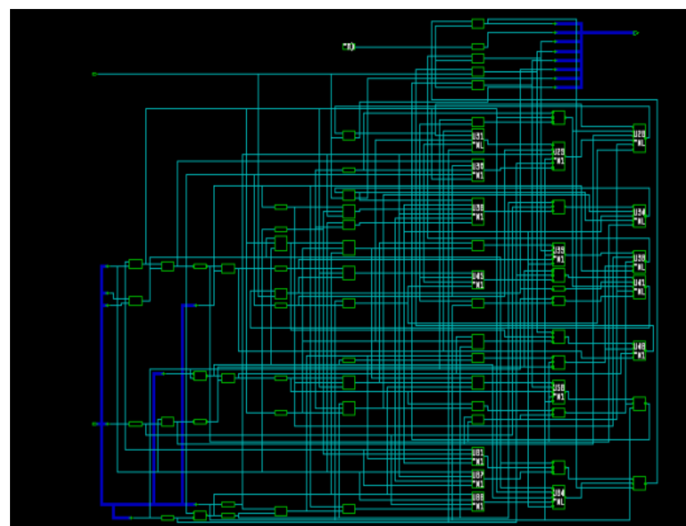

Figure 8. Gate Level Schematic Diagram for Look-Up Table Sub-Module.

Meanwhile, Figure 9 shows the final layout of TDSP after physical implementation in IC Compiler is completed. The process of physical implementation begins with floor planning, placement of standard cells, Clock Tree Synthesis (CTS) and lastly the routing. Table 1 shows the comparison of the specification of the layout on the latest architecture compared to previous architecture [9].

Based on Table 1, there are differences in terms of layout size. This is because both architectures using the difference technology library. Different foundry has different sizes of standard cells. Moreover, there are slightly different in terms of total power, the reason is, the layout of the latest architecture is optimized in terms of Power and Design for Test (DFT).

Table 1. Layout Specifications

Specifications	Latest Architecture	Previous Architecture [9]
Size of layout (Without IO Pad)	100µm(w) x 96µm(h)	300µm(w)x300µm(h)
Input Voltage (V)	1.8	1.8
Clock Frequency (MHz)	16	16
Total Power (mW)	1.446e-06	6.4916e-02
Technology Library	Silterra	TSMC

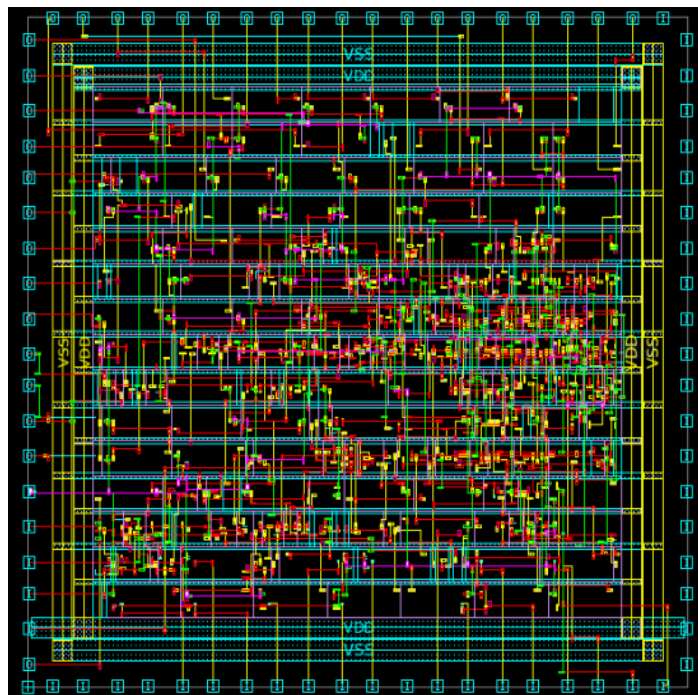

Figure 9. Final Layout of an 8-bit TDSP unit

6. CONCLUSION

A temperature-based digital signal processing simulation has been done using Verilog HDL code for the purpose of simulation in Synopsys. Such type of implementation can be used with different applications, such as temperature control and monitoring system. Thus, this design provides an intricate control and optimal thermal management on system-on-chip (SoC) devices, upon which a complete thermal management system for modern computer designs can be implemented with an advantage of minimum chip area required.

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