

FPGA-based embedded architecture for IoT home automation application

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ABSTRACT

An Internet of Things (IoT) FPGA-based home hub to automate control operations in a home environment was designed and built. The proposed system uses an FPGA home hub as its local analytic engine with an IoT platform to store the sensory data. The FPGA was programmed in Verilog HDL using Quartus II provided by Altera. The WiFi capability of the FPGA was extended through an ESP8266 chip to ease the interfacing with various sensors connected to it. The system can be configured and monitored through a web application coded in JavaScript. Various test cases were carried out on the implemented system at Multimedia University (MMU) Digital Home Lab. The results verified the functionality of the system in triggering real home appliances (i.e. air conditioning unit and lighting) based on multiple sensor nodes without conflicting each other. The ability to allow user to configure the control rules based on the sensory data via web interface hosted using ThingSpeak Plugins is also presented and demonstrated in this project. The base design is utilizing Altera Cyclone IV EP4CE22F17C6N FPGA with 153 I/O pins, which is highly scalable and adaptable to the requirements of home environments. This shows promising application of FPGA in supporting scalable IoT home automation system.

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1. INTRODUCTION

People are continually working towards enhancing the quality of life. As technology advances, the ambition of building a smart home with scheduled and automated home devices to create a more comfortable living environment becomes achievable. A survey conducted by TNS on behalf of Intel Corporation found that 68% of Americans believe that smart homes will be as popular as smartphones within 10 years [1], and Internet of Things (IoT) will be the core technology of these smart homes as well as smart city. [2,3,4]. IoT is an emerging technology trend in which objects such as sensors and actuators are given networking and computing capability, so that they can communicate and generate data among themselves with minimal human intervention [5]. The generated data can be analysed to provide valuable functions to the users. IHS predicts that by 2020, there will be more than 30 billion devices in the IoT market, impacting the areas of automation, integration and servitization (service-oriented business models) [6]. Currently available IoT platforms for home automation, however, are still limited [5], and the use of Field-programmable Gate Array (FPGA) is still relatively uncommon in these platforms. FPGAs have the potential to achieve higher performance than the more commonly-used embedded computers such as Raspberry Pi in many areas. [7,8,9]. The FPGA chips are well-suited for home automation for they have longer lifecycle, more than 100 general-purpose input and output (GPIO) pins (e.g. 150 GPIO for cyclone IV device). This project

designs and develops an embedded architecture to take advantage of the hardware parallelism in FPGAs to serve as a local analytic engine in IoT application for home automation using Verilog Hardware Description Language (HDL) and explores the potential of FPGA in IoT applications.

2. RELATED WORK

Debono and Abela reported a home automation system in which FPGA was used as the central controller with a Bluetooth module, various sensors and actuators interfaced to it [10]. The controlling and monitoring was realized by using the application in the mobile phone. However, the required Bluetooth connection between the module and the phone limits the operation range of the system. Sharma et. al. reported a similar FPGA-based monitoring system [11], both of these projects are controlling the home appliances based on single sensor mode, i.e., one sensory data to trigger one home appliance, without analyzing the status of multiple sensory data.

In contrast, Chinchansure and Kulkarni developed a home automation system that interfaced with a Global System for Mobile communication (GSM) modem that allows users to communicate with the system using Short Messaging Service (SMS) [12]. Although the operation range is greater than that of the Bluetooth, every control operation invoked by users via SMS incurs charges.

Kumar and Rao developed a secure home automation system that uses an FPGA to perform encryption and decryption to the data that are transmitted wirelessly between components of the system [13]. This project highlighted the advantages of FPGA in terms of scalability, configurability and security.

Rusu and Duka proposed and implemented a system in which FPGA boards are used to connect to and control household appliances [14]. A Raspberry Pi enables communication with the FPGA and a web application which can be accessed from a computer or mobile device. The system is designed to be flexible, scalable and adaptable to various communication protocol. The inclusion of a web technology provides for control of household appliances remotely through the Internet and also control of appliances in more than one home is reported in this paper. However, the embedded ARM Cortex M0 IP core of FPGA instead of Verilog HDL is used, which might not truly reflect the advantages of the FPGA in terms of configurability and scalability.

The IoT framework proposed by Laubhan consists of multiple sensor nodes which collect data from the sensors and sends them wirelessly to a regional hub which acts as a local analytic engine [15]. Raspberry Pi 2 was used as the regional hub. On top of that, a cloud portal is used to store the data from all regional hubs, provide user accessibility, and achieve more comprehensive analytical functions. The Wireless Sensors Network (WSN) applied in this platform is crucial to allow a wide distribution of sensors without the need of physical connections to the analytic engine. A similar IoT framework is adopted in this project with the FPGA functioning as the local controller hub with embedded analytic engine developed using Verilog HDL. To reduce the cost, open source IoT data platforms, Dweet.io and ThingSpeak, were utilized to allow the users to access the system.

3. SYSTEM DESIGN AND IMPLEMENTATION

An overview block diagram of the system is shown in Figure 1. The FPGA home hub acts as a local analytic engine based on the analytic rules configured by the users via web interface. Multiple sensor nodes are employed to provide the input data to the FPGA via Verilog-HDL based UART module developed in this project. The baud rate of the serial communication is set to 115200. Based on the sensory data received by the FPGA, users can configure the analytic rules in the form of “if-else” structure for home automation. The hardware prototype of the implemented system is shown in Figures 2a and 2b. It consists of an FPGA-based analytic engine that communicates with various sensor nodes via Wi-Fi connection and a web interface. Users can combine the status of the sensory data from various sensor nodes to define the control rules via the web interface hosted in remote cloud using ThingSpeak Plugins. These user-defined control rules are stored inside a Secure Digital (SD) card. In this design, users can define up to 10 rules. The output of the system is infrared (IR) profile signals for home appliances. The IR receiver module learns the IR profiles of home appliances and stores them in the SD card. This eliminates the need to hardcode any IR profiles in the system and provides the flexibility to control various brand and model of IR controlled home appliances.

4. LOCAL ANALYTIC ENGINES IN FPGA HOME HUB

The Verilog design entity of the local analytic engines is shown in Figure 3. The number of data sets and rules are pre-defined but can easily be re-defined using parameters named as “NUM_ESP” and “NUM_RULES”, during module instantiation as shown in Figure 4. (i.e., the parameter. NUM_RULES is

redefined to 10 instead of 2 as in Figure 3.) The rules applied on the data set are implemented using “if-else” structures defined in module “rule_subcore”, with the input values configured via web-page interface. In the operation mode, the result of entity “analytic core” will be used to match the IR profiles stored in the SD card. Then, the ESP8266-based sensor node will transmit the IR profile signal via UART transmitter for home automation tasks such as turning the air-conditioning and lighting on / off. A sample output of the UART transmitter, to trigger the LG air conditioning unit, is shown in Figure 5.

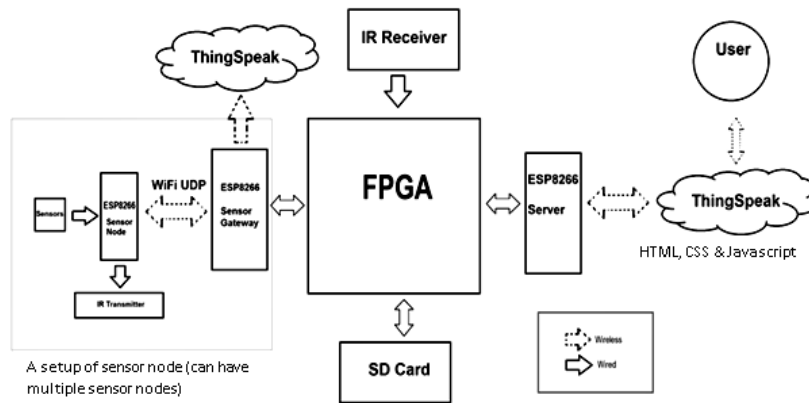


Figure 1. Overview block diagram

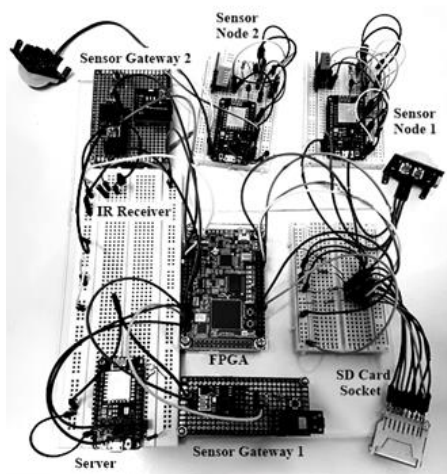


Figure 2a. Hardware prototype



Figure 2b. Web user interface

5. MULTIPLE SENSOR NODES TO FPGA HOME HUB

Two ESP-12-E-based sensor nodes and a single FPGA home hub are constructed and tested in this project. Each node consists of an ESP-12-E with sensors (i.e., temperature, humidity, and motion) and an IR transmitter, TSOP38238. This structure emulates the function of a WSN. Signals from the sensor are transmitted to the FPGA home hub wirelessly via internal home network. This demonstrates the ability of the FPGA home hub to serve as a local analytic engine for scalable distributed sensors nodes.

All the sensor signals are collected and analyzed by the FPGA home hub for immediate action, as well as being displayed on IoT dashboard for remote notification and action. The IR profiles learned and stored in the FPGA home hub's SD-Card are retrieved and transmitted via home network to the sensor nodes. The sensor nodes which contain IR transmitters then transmit the IR signal based on the received IR profile received to turn ON/OFF the home appliances. The schematic diagram of the sensor node which consist of ESP8266 by Espressif is shown in Figure 6.

```

module analytic_core #(
    parameter NUM_ESP = 2,
    parameter NUM_RULES = 2
) (
    input clk,
    input [8*NUM_ESP-1:0] temperature, //unsigned 8-bit
    input [8*NUM_ESP-1:0] humidity,
    input [8*NUM_ESP-1:0] motion,
    input [47:0] conf_data, //47:0 data for lower and upper boundary
    input [15*NUM_RULES-1:0] conf_sel,
    input conf_sig_in,
    //output reg conf_sig_out,
    output [NUM_RULES-1:0] result,
    input [7:0] count_rules,
    output reg busy
);
    
```

Figure 3. Design of entity analytic_core

```

analytic_core #(
    .NUM_ESP(2),
    .NUM_RULES(10)
) a1(
    .clk(clk),
    .temperature(temperature),
    .humidity(humidity),
    .motion(motion),
    .conf_data(conf_data),
    .conf_sel(conf_sel),
    .conf_sig_in(conf_sig_in),
    .result(result_rule),
    .count_rules(count_rules),
    .busy(analytic_busy)
);
    
```

Figure 4. Module analytic core instantiation with 10 rules

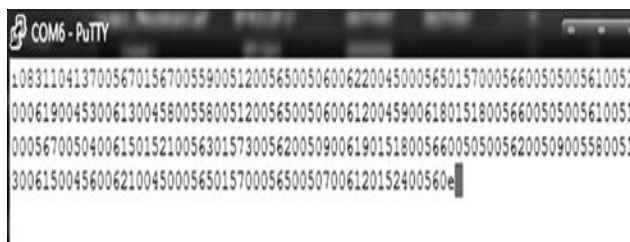


Figure 5. IR profile sent from uart transmitter to trigger an air conditioning unit

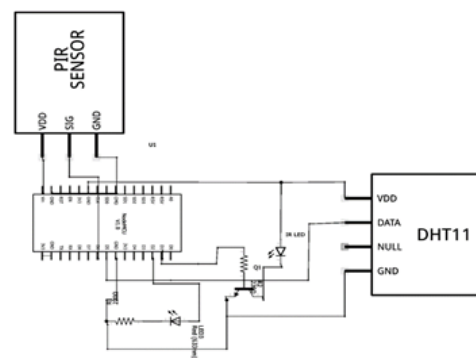


Figure 6. Schematic diagram of the sensor node

6. PERFORMANCE RESULTS

A physical field test was conducted at Digital home and lifestyle Lab in Multimedia University (MMU) to ensure the analytic rule is triggered correctly according to its configuration and subsequent pre-set action is performed according to the triggered rules. One of the rules tested is shown in Figure 7. Two parameters, room temperature (between 00C to 300C) and motion, were used in this rule in order to trigger the air conditioner unit via IR signal transmitted from sensor node 2. The test has verified the functionality of the FPGA home hub and its ability to control a home appliance (the air conditioner unit) based on the status of the sensory data and its configured rule. The functionality of the analytic core was verified using a Verilog HDL test bench. Figure 8 shows the result waveform of the test bench and Table 3 shows the comparison of expected result and the actual result obtained.

Home Automation System				
Parameter 1	Parameter 2	Parameter 3	Action	
1	0stemperature_2<=30	None	motion_2=1	Send IR 2 to Unit 2
2	Deactivated			
3	Deactivated			
4	Deactivated			
5	Deactivated			
6	Deactivated			

Figure 7. Home automation system test rule

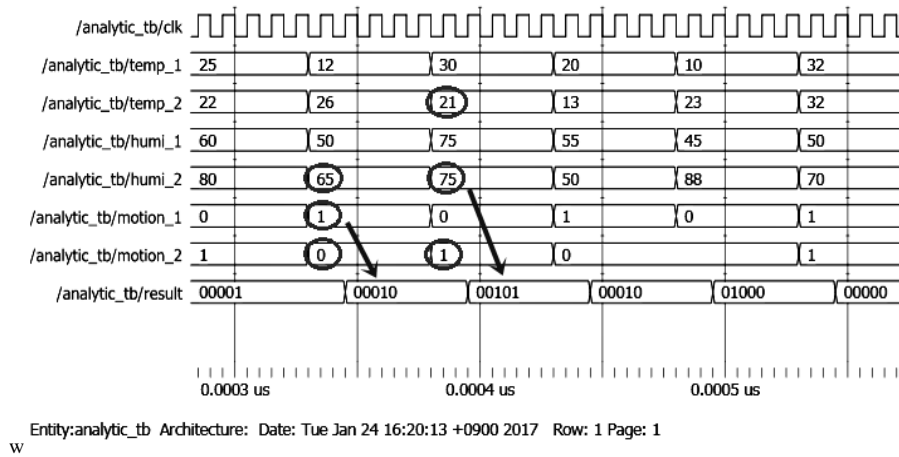


Figure 8. Result waveform of the test bench

Five rules were configured and eight sets of data with different parameters were fed into the analytic engine. Table 1 shows the list of configured rules and Table 2 shows the list of sensory data that fed into the analytic engine. The analytic core was instantiated to accommodate two sensor nodes. As highlighted in Figure 8, rule 2 (“0010”) is generated when the sensory data comply with the rule no 2 as in Table 1 (i.e., $humi_2 \geq 50$, $motion_1 = 1$, and $motion_2 = 0$). Similarly, rule 5 (“0101”) is generated when the data comply to rule 5 in Table 1 (i.e., $temp_2 \geq 20$, $humi_2 \geq 70$, and $motion_2 = 1$). Hence, the Verilog-HDL test bench results verified the analytic engine's functionality.

Table 1. List of Configured Rules Tested in the Test Bench

Rule No.	Parameter 1	Parameter 2	Parameter 3
1	$15 \leq temp_1 \leq 30$	$20 \leq temp_2 \leq 26$	$motion_2 = 1$
2	$50 \leq humi_2 \leq 70$	$motion_1 = 1$	$motion_2 = 0$
3	$70 \leq humi_1 \leq 80$	$60 \leq humi_2 \leq 75$	$20 \leq temp_2 \leq 23$
4	$motion_1 = 0$	$10 \leq temp_1 \leq 15$	$30 \leq humi_1 \leq 50$
5	$20 \leq temp_2 \leq 25$	$70 \leq humi_2 \leq 90$	$motion_2 = 1$

Table 2. List of Data Fed into the Analytic_Core in the Test Bench

Data	temp_1	humi_1	motion_1	temp_2	humi_2	motion_2
1	25	60	0	22	80	1
2	12	50	1	26	65	0
3	30	75	0	21	75	1
4	20	55	1	13	50	0
5	10	45	0	23	88	0
6	32	50	1	32	70	1
7	24	70	0	20	70	0
8	28	65	1	21	60	1

Table 3. List of Data Fed into the Analytic_Core in the Test Bench

Data	Expected Result	Obtained Result	Expected matches obtained results
1	00001	00001	✓
2	00010	00010	✓
3	00101	00101	✓
4	00010	00010	✓
5	01000	01000	✓
6	00000	00000	✓
7	00100	00100	✓
8	00001	00001	✓

7. CONCLUSION

An FPGA-based home hub featuring a local analytic engine has been implemented and tested with several test cases in an actual home environment setup at Digital Home and lifestyle Lab in MMU. An Verilog-HDL Test bench results were also included to verify the functionality of the analytic core developed in this project. The FPGA home hub successfully demonstrated the ability of FPGA being used in an IoT platform and its internal architecture in handling multiple sensor nodes. This shows the potential of FPGA in handling multiple sensor nodes simultaneously without any software delay as in most sequential programming microcontroller based system. New sensor node units can be added to the system easily without conflicts. The prototype implementation of the system included two sensor nodes to demonstrate this. From that, it can be concluded that as long as the firmware code is well-written with scalability in consideration, FPGA-based design can be scaled up with minimum effort.

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