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Electronic controlled CMOS inductor with patterned metal ground shields for fine inductance tuning application

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ABSTRACT

This paper is on an inductance fine tuning technique which benefits from the idea of varying the number of metal plates of an inductor's pattern ground shield (PGS) shorted to ground to change its magnetic fields. This technique is unique because the geometry and physical shape of the inductor remains untouched from its form in the process design kit (PDK) while the inductance is being tuned. The number of metal shields shorted to ground was controlled by an electronic circuit which consists of analog-to-digital converters and active switches. Both Sonnet EM simulator and Cadence Virtuoso were used for the inductor and circuit simulations. From the simulation, it was found that the inductance increased while the Q-factor decreased as more metal shields were shorted to ground. For instance, at 1.6 GHz, the simulated inductance was 8.8 nH when all metals were floated and 9.4 nH when all metals were shorted to ground. On the other hand, the simulated Q-factor was 10.4 when all metals were floated and 9.8 when all metals were shorted to ground. From both simulation and measured results, both inductance and inductance tuning range increased with frequency. From the measured results too, the inductance observed was 9.4 nH at 1.6 GHz, 10.8 nH at 2 GHz, and 13.5 nH at 2.5 GHz when all the metal shields were shorted to ground. The inductance tuning range was 6.2% at 1.6 GHz, 12.5% at 2 GHz, and 20% at 2.5 GHz. The measured results showed good correlation with the simulated results trend, but with smaller value of inductance, inductance tuning range and Q-factor.

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1. INTRODUCTION

Recently, researchers are interested in developing on-chips tunable inductors. The demand of the on-chips tunable inductors increases especially in radio frequency (RF) and microwave applications. This is because inductance variation due to process variation and unpredicted parasitic is unavoidable after fabrication. The effects of inductance variation are crucial especially for frequency sensitive circuits such as oscillators. Hence, it is useful to have flexibility for inductance fine tuning after fabrication as re-fabrication is costly.

In this paper, a suitable inductance fine tuning technique is presented which is suitable to any available PDK monolithic on-chip inductor. In general, this technique utilized the idea of changing the magnetic field of the planar inductor by shorting the metal shields of the PGS in turn to the ground. Previously, PGS were solely used to isolate the inductor form the substrate without tuning capability consideration [1], [2]. However, in this research, PGS were utilized to tune the inductance value, by shorting the metal fingers of the shield one by one to the ground. To the best of our knowledge, this is the first time such technique is implemented in standard CMOS process in order to tune the inductance value. The work in this paper was focusing on the effect of magnetic field variation on the inductance tuning range. This paper also discussed on the impact of ths patterned grounding towards the quality factor or simply known as Q-factor.

Passive components such as inductors, capacitors, and resistors are important elements in RF circuit design. Nevertheless, these passive components are also the limitation factors in terms of performance and cost in RF circuit design. Especially in integrated circuit (IC) design, the inductor consumes a large layout area and having many inductors in a circuit means a higher cost for fabrication. In IC design too, the semiconductor parasitic affects the overall value of the inductance and capacitance.

Previously, researchers were focusing on the Q-factor and the substrate losses when designing an inductor for high frequency applications. These two factors determine the performance of the inductor [3]. A good performance inductor should have high Q-factor and low substrate losses. Supposedly, at high frequency, the Q-factor should be high but unfortunately it is not due to the substrate losses. The inductor equivalent circuit for the Q-factor modeling is shown in Figure 1. From that, the inductor's Q-factor can be derived as [3]:

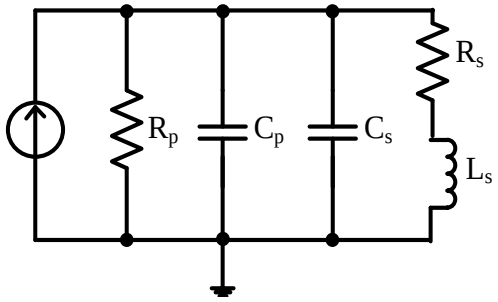

Figure 1. The inductor equivalent circuit for the Q-factor modeling [3]

$$Q = \frac{\omega L_s}{R_s} \cdot \frac{R_p}{R_p + \left[\left(\omega L_s / R_s\right)^2 + 1\right] R_s} \cdot \left[1 - \frac{R_s{}^2 (C_s + C_p)}{L_s} - \omega^2 L_s \left(C_s + C_p\right)\right] \quad (1)$$

$$Q = \frac{\omega L_s}{R_s} \cdot Substrate\ Loss\ Factor \cdot Self - resonance\ Frequency \quad (2)$$

where ω is defined as the radian frequency, L_s is the series inductance, R_s is the series resistance, R_p is the coupling resistance, C_p is the coupling capacitance, and C_s is the series capacitance between metal lines.

From the first term in (1), it is clear that Q is proportional with L_s but inversely proportional with R_s. As shown in(1) can be further defined as in (2). The first term denotes the magnetic energy stored in the inductor and the ohmic loss in the series resistance. For the second term in the same equation, substrate loss is due to the capacitive and inductive coupling. The capacitive coupling from the metal layer to the substrate induces the displacement current due to the variation in the substrate potential.

On the other hand, an inductive coupling happens when the magnetic field from the metal penetrates the substrate and induces an eddy current. Both displacement and eddy currents cause the substrate loss which consequently reduces the inductor's performance [3].

In order to cater for the substrate loss, researchers in [3]–[5] use metal ground shields to isolate the metal layer from the silicon substrate. The metal ground shields can be either solid or patterned. However, a solid ground shield reduced performance of the inductor as it induced an eddy current. This corresponding current produced the magnetic fields which negatively coupled with the magnetic flux from the spiral inductor. This causes the inductance to drop. The PGS, on the contrary, restricts formation of the induced current. Thus, the inductance in the inductor remains unchanged.

Many methods were introduced by researchers to enhance the Q-factor of the inductor. As an example, Forbes in [6] used a field effect transistor and two inductors arranged in a feedback loop. The first inductor was connected to the gate while the second inductor was connected to the source. The best Q-factor was achieved when both inductors were spiral-shaped, and the first inductor was larger that the second inductor. Though improvements in the substrate loss and Q-factor contributed to good inductor characteristics, they do not fulfil the purpose if inductance tunability was the requirement.

At present, researchers are interested in developing a tunable inductor. There are a few frequency tuning techniques available. One of the techniques is the counteractive magnetic field induction. It controls the magnetic flux of the inductors by partially or fully shielding it. According to Lenz's law, as the magnetic flux of the spiral inductor passes through the metal plate, an eddy current starts to move in the metal plate and subsequently induces a counteractive magnetic field.

In [7], the authors introduced a parallel moving metal on top of the planar spiral inductor to shield magnetic flux which penetrated the inductor. When the capacitance between the electrodes of inductors as well as the metal shield increased, it caused inductance variation due to permittivity variation.

Researchers in [8] utilized ferrofluid actuation to vary the permeability distribution on the planar spiral inductor, which resulted in inductance variation. To enable ferrofluid actuation, an external biasing field was needed to allow repelling of the fluid from the inductor. In addition, an actuation planar coil was required to generate magnetic field.

Next, researchers in [9] used pizomagnetic core to control the inductance of the MEMS inductor. The proposed inductor was made up of the PZT bridge between the two electrodes. When a DC voltage typically from 1 V to 10 V was applied to each pair of the sided-electrodes, it shorted or extended the central part of the PZT bridge. The uniaxial tensile or compressive planar stress was transferred to the ferromagnetic core, changing its permeability and incductance due to the magnetostatic effect.

Previous work in [10] showed that an electrically tunable RF inductor, based on a planar solenoid with a thin-film ferromagnetic (FM) core (NiFe), could be achieved. However, this design required an extra DC current through the same device to vary the effective permeability of the FM core that caused the inductance value to vary.

Sato el al., in [11] used the circumferential wiring together with a switch to tune the inductance value of the inductor. This wiring, which was known as a loop conductor, placed around the spiral inductor with a switch at one end. When the switch was opened, no current was induced in the loop conductor. Subsequently, when the switch was shorted, the loop conductor became a closed loop. The magnetic flux from the spiral inductor passed through the loop and induced an eddy current which caused the inductance value to change, similar to explanation given in [1], [3], [4].

Loke et al. [12] used transistors to vary the magnetic flux of the inductor. The transistors were arranged so that their gate structures were orthogonal to the turns of the inductor. The transistors resembled the solid ground shield (SGS) when they were on. This happened due to the current that was induced which changed the magnetic flux in the inductor. Consequently, the inductance value dropped. On the other hand, the transistors resembled PGS when they were off. This is because the inductance remained unchanged since the PGS restrained the formation of the eddy current.

In [13], researchers adopted different configurations to tune the inductance value and to varye the Q-factor in a voltage-control oscillator. The design was made up of a pair of inductors, and the resistance of switch. To vary the inductance, the second inductor has to be included or excluded in the circuit. A series configuration allowed higher tuning range but reduced the Q-factor. This happened as the resistance of the switch was added in series with the first inductor, when the second inductor was shorted to ground. In contrast, a parallel configuration was able to demonstrate better Q-factor as the resistance of the switch was added in parallel with the first inductor.

Unfortunately, the aforementioned works were impractical to integrate with CMOS and not suitable for mass production. In addition, some of the techniques might only be realized when changes were made to the existing fabrication process of the inductor. Hence, a method to enable the inductance fine tuning without changing the physical shape and geometry of any available PDK on-chip inductor will definitely benefit the RF integrated circuit (RFIC) designers to enable first tape-out success.

This work was conducted to demonstrate a fine-tuning technique to vary the inductance of a monolithic on-chip inductor. This technique did not change the physical shape and geometry of the available inductor. It can be added to any available PDK inductor without changing its fabrication processes. This proposed tunable inductor is suitable to be used in RF application circuitries, especially in frequency sensitive circuits like the oscillator.

2. RESEARCH METHOD

This paper presents a new approach to achieve a fine-tuning range of the inductor without changing its physical shape and geometry. The change in magnetic field was achieved by shorting the metal shields in turn to the ground. The metal shields were detached from each other. This allowed a fine-tuning range of the inductor by shorting the metal shields one by one to the ground. The inductor showed the maximum inductance value when all the metal shields were grounded. Simulation on the inductor was performed using Sonnet EM simulator while the electronic circuit controlling the grounding of each metal shield was verified using Cadence Virtuoso.

2.1. Design of The Tunable Inductor

All design processes were conducted in Cadence Virtuoso and Sonnet EM. Figures 2 to 4 show the 2D, 3D and overall layout views of the proposed inductor.

(a) (b)

Figure 2. Sonnet 2D view of the (a) tunable inductor and (b) switches modeled as resistors

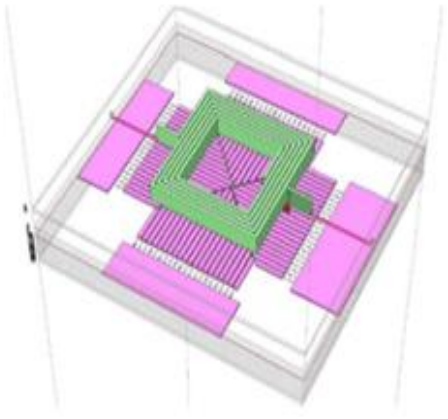

Figure 3. Sonnet 3D view of the proposed variable inductor with metal shields and switches to the ground (modeled as resistors)

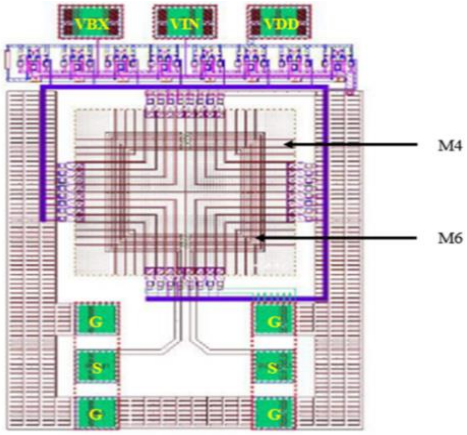

Figure 4. Layout of the proposed tunable inductor in cadence virtuoso

2.2. Mechanism of Shorting and Floating the PGS Metal Shields of the Tunable Inductor

Switches were used to ground the metal shields. There were 32 switches in total. Each two of them were connected through one plate of the metal shield. Hence, the total number of metal shields was 16. Figure 5(a) shows the proposed inductor when all the switches were OFF. This state indicated that all the metal shields were floated. Figure 5(b) shows when state 1 was chosen which made four switches were shorted so that two metal shields were grounded. In Figure 5(c), another four switches were turned ON, this made four metal shields in total were grounded. When all the switches were ON as shown in Figure 5(d), this implied that all the 16 metal shields were grounded. By increasing or decreasing the number of metal shields shorted to the ground, the magnetic fields of the inductor are actually being changed, hence resulting in inductance tuning.

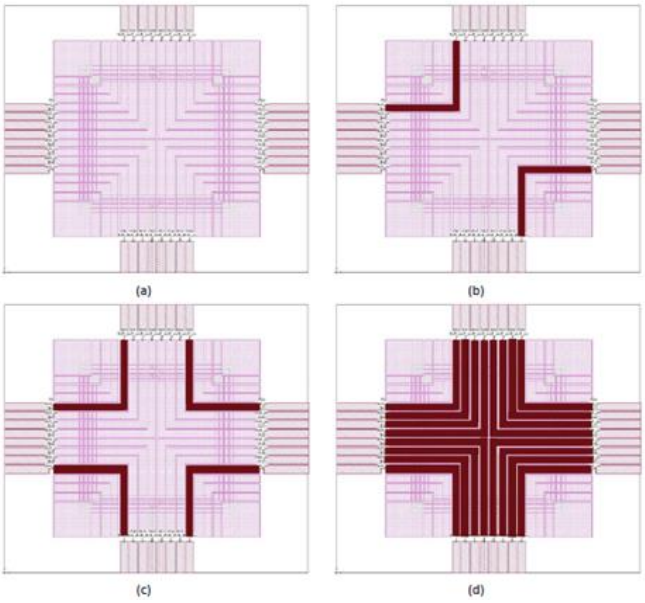

Figure 5. 2D view of the tunable inductor (a) when all switches are OFF, (b) when four switches are short to make two metal plates grounded, (c) when eight switches are short to make four metal plates grounded, and (d) when all the 32 switches are ON to make all the 16 metal plates grounded

Figure 6 shows the basic concept of an analog-to-digital converter circuit. This circuit was applied to tune the inductor by using one pad only (i.e. the Vin pad). The control voltage, Vin, was varied from 0 to VDD. Vref was fixed at VDD.

Figure 7 shows the schematic of the control circuit. It includes a half analog-to-digital converter to convert a dc voltage range from 0 to 1.2V into a digital stream of 00000000 to 11111111. The top most op-amp for the circuits in Figures 6 and 7 was used to generate the most significant bit (MSB). Table 1 shows the conversion denoted by this circuit.

The op-amps in the half A/D converters shown in Figure 7 were simple single-stage amplifiers with current tail, followed by a common source stage to improve the linearity and output voltage swing properties. This circuit is shown in Figure 8. VBX was the biasing voltage just above the threshold voltage of the NMOS.

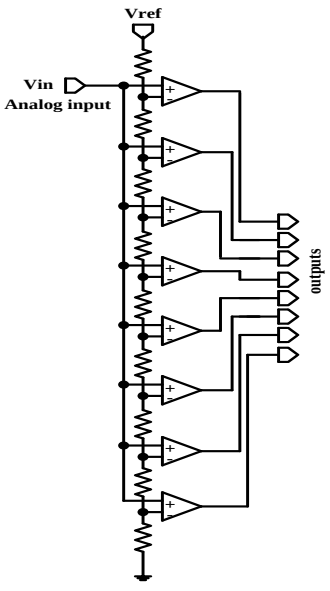

Figure 6. Basic concept of an analog-to-digital converter circuit

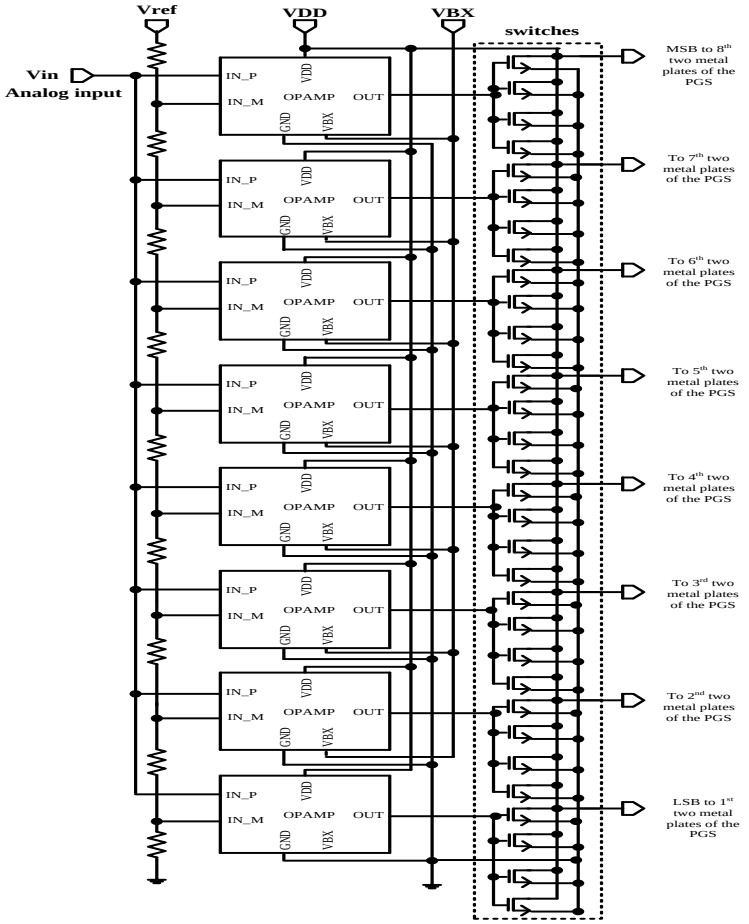

Figure 7. The schematic of the control circuit

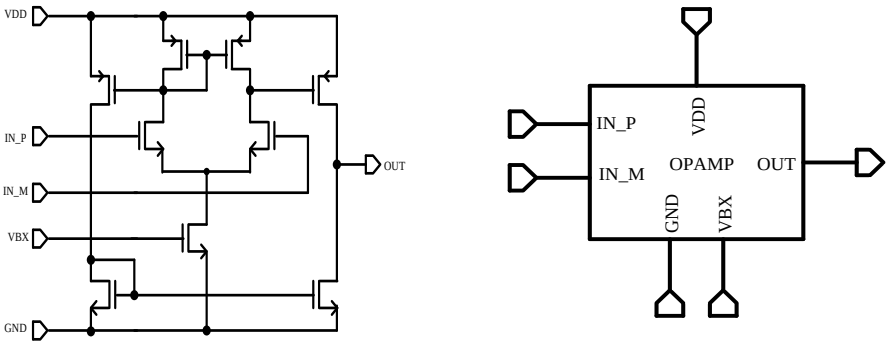

Figure 8. Op-amp in a half A/D converter circuit (a) schematic,(b) symbol

Table 1. Different States in Terms of the Voltage Control

State	Vin (mV)	Half A/D output
0	0 – 93.75	00000000
1	93.75 – 187.5	00000001
2	187.5 – 281.25	00000011
3	281.25 – 375	00000111
4	375 – 468.75	00001111
5	468.75 – 562.5	00011111
6	562.5 – 656.25	00111111
7	656.25 – 750	01111111
8	750 – 1200	11111111

2.3. Simulation of The Tunable Inductor

The proposed inductor was Sonnet EM simulated for state 0 (OFF) and state 8 (ON). The CMOS switches were modeled as resistors which are 1 MΩ when OFF-state and 10 Ω when ON-state. The Sonnet model of this proposed inductor is shown in Figures 2 and 3.

3. RESULTS AND ANALYSIS

This section discussed about the simulation as well as the measured results of the tunable inductor in section 3.1 and 3.2, respectively.

3.1. The Tunable Inductor Simulation Results

Figure 9 shows the simulation results of the tunable inductor using Sonnet EM simulator. As can be seen from this figure, the inductance changes with frequency. As frequency increases, inductance will also increase. The inductance tuning range also increases with frequency. As an example, at 1.6 GHz, the inductance changes from 8.85 nH (when all switches are OFF, i.e. the metal shields are all floating) to 9.44 nH (when all switches are ON, i.e. the metal shields are all grounded). This shows a 6.2% of inductance tuning range. Meanwhile, at 2.0 GHz, the inductance varies from 9.45 nH to 10.8 nH, which is 12.5% of inductance tuning range. A final example is at 2.5 GHz, where the inductance now can vary from 10.8 nH to 13.5 nH, which contributes to 20% of inductance tuning range.

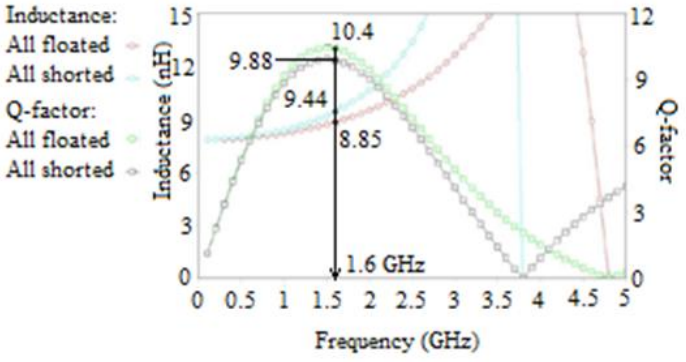

Figure 9. The Sonnet simulation results of the proposed inductor

3.2. The Fabricated Tunable Inductor Measurement Results

Figure 10 shows the micrograph of the fabricated tunable inductor while Figure 11 shows its measured inductance values when the PGS was shorted to ground one by one. Again, the results indicated that the inductance increased with the frequency. The inductance tuning range is also proportional to the frequency. At 2.0 GHz, the inductance tuned from 7.9 nH to 8.1 nH. The tuning range was about 2.47%. At 2.5 GHz, the inductance tuned from 9.5 nH to 10.1 nH, a tuning range of 5.94%. Both simulated and fabricated inductors showed correlation in terms of the tuning range trend. This verified the concept of the proposed technique for inductance tuning. Nevertheless, the measured results portray smaller inductance tuning range as compared to the ones obtained from simulation.

Figure 12 shows the relationship between Vin and inductance at different frequencies. From the mentioned figure, when all the metal shields were grounded (indicated by Vin = 0.8V), the inductance was at its highest value for each frequency. In contrast, when the metals were left floated (at Vin = 0V), the inductance was at its lowest value for each frequency. This observation confirmed that PGS helped to vary the inductance value, hence able to be used as a fine-tuning method for the inductor. Based on Figures 11 and 12 also, it is seen that as the frequency goes higher, the inductance tuning range also becomes larger.

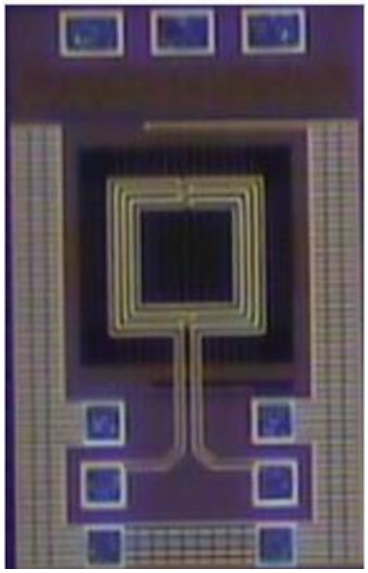

Figure 10. The fabricated tunable inductor

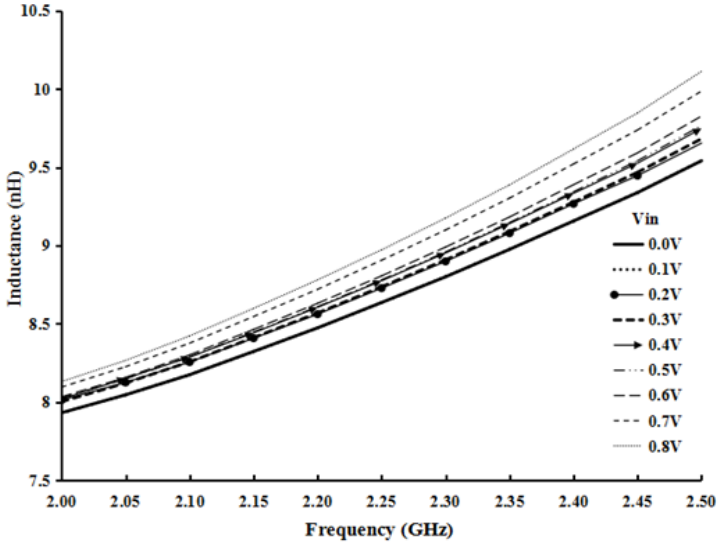

Figure 11. The measured inductance versus frequency of the tunable inductor. V_{in} = 0.0 V was when all PGS metals were floated while V_{in} = 0.8 V was when all PGS metals were grounded

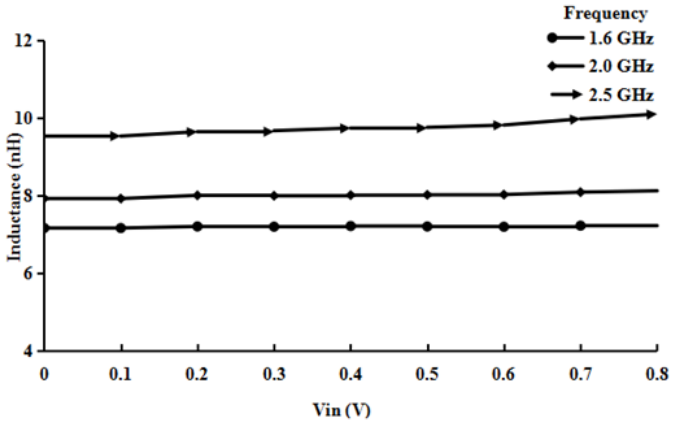

Figure 12. The measured inductance versus V_{in} at different frequencies

The second term (i.e. substrate loss factor) in (1) described in Section 2 indicates that the number of metal shield floating or shorted to ground will affect the Q-factor of the inductor. The maximum Q-factor can be realized when the term for substrate loss factor becomes unity. To achieve that, Rp should be very large (i.e. Rp approaches infinity). It can be done by inserting metal shields to the ground. However, in Figure 13, the Q-factor decreases as more patterned shields were grounded. As an example, at 2 GHz, the Q-factor drops from 7.5 to 5.8 when all metal shields were floated and shorted to ground, respectively. This is because PGS increases the capacitance to the ground. This parasitic capacitance reduces the inductance, hence decreasing the Q-factor [3].

Another observation from Figure 13 is that the Q-factor at first increases with frequency until it reaches its peak between 1.3 GHz to 1.5 GHz. Beyond this frequency, the Q-factor starts to decrease with further increment in frequency. This can be explained by looking at (1), whereby Q-factor will increase at first due to increment in the first term, but then will later decrease due to the second and third terms becoming more dominant. As an example, at 2.5 GHz, the Q-factor when all metal shields were floated is 5.94 as compared to the 7.5 obtained at 2 GHz under the same condition.

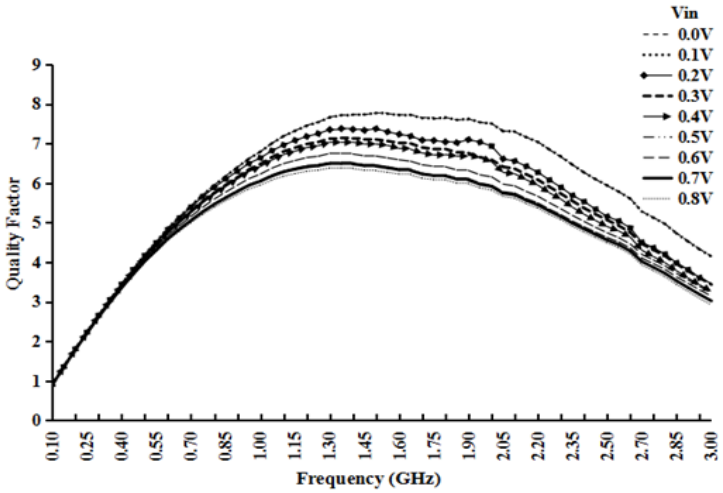

Figure 13. The measured Q-factor versus frequency at different Vin

Finally, Figure 14 shows the Vin effect on the Q-factor. As Vin increases, more switches will be turned on resulting in more metal shields being shorted to ground. Figure 14 shows that when Vin increases, the Q-factor deteriorates. In terms of Q-factor dependence on frequency, the Q-factor deteriorates with the increment of frequency. This is consistent with the observation made for Figure 13 and therefore the reason for the mentioned trend follows the one given for the previous figure.

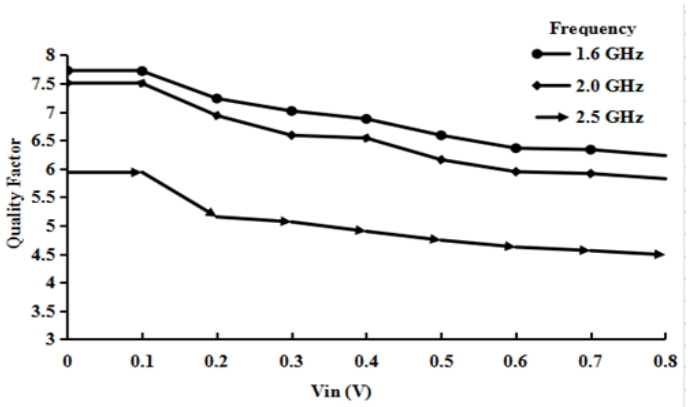

Figure 14. The measured Q-factor versus V_{in} at different frequencies

The performance summary and comparison with other works are tabulated in Table 2. At frequency less than 0.1 GHz, the inductor has larger tuning range [8], [10]. However, lower frequency range has become saturated, hence there is an urge to exploit higher frequency range. Researchers in [7], [9] utilized MEMS technology in their designs. Even though their works showed higher inductance tuning range and Q-factor, nevertheless MEMS technology is currently not suitable for mass production and expensive. This work achieved the highest application frequency, up to 2.5 GHz and suitable for fine-tuning applications. Besides, this tunable inductor design is readily to be integrated with available CMOS technology process.

Table 2. Performance Comparison of the Tunable Inductors

	[8]	[10]	[7]	[9]	This work
Frequency (GHz)	0.06	0.1	2.0	2.1	2.5
Inductance Tuning Range (%)	16	< 50	29.82	42.13	5.94
Q-factor	23	< 2	< 6.0	11.9	5.94
Application	-	-	LNA	VCO	-

4. CONCLUSION

In this paper, a monolithic inductor with fine tuning capability is proposed. The fine tuning was achieved by controlling the magnetic flux between the inductor and substrate through varying the number of PGS metals shorted to the ground via the use of analog to digital converters and active switches.

Verification of the tuning concept was realized first through simulation using Sonnet EM and Cadence Virtuoso. The tunable inductor was then fabricated and measured. Results from the simulation and measurement were then compared for consistency.

From the simulation and measured results, it is found that as more metal shields were grounded, the inductance and inductance tuning range increase. The tradeoff, however, is the deterioration of the Q-factor when the same condition was imposed.

The advantage of this fine tuning technique is that the main structure of the inductor maintains as it is in its PDK form. This is interesting to the foundry and PDK providers as the inductance can be tuned without changing the existing inductor fabrication process.

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