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Design of low power 8-bit Gate-diffusion input (GDI) full adder using variable body bias (VBB) technique in 90nm technology

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ABSTRACT

In digital system, the full adders are fundamental circuits that are used for arithmetic operations. Adder operation can be used to implement and perform calculation of the multipliers, subtraction, comparators, and address operation in an Arithmetic Logic Unit (ALU). The subthreshold leakage current increasing as proportional with the scaling down of oxide thickness and transistor in short channel sizes. In this paper, a Gate-diffusion Input (GDI) circuit design technique allow minimization the number of transistor while maintaining low complexity of logic design and low power realization of Variable Body Biasing (VBB) technique to reduce the static power consumption. The Silterra 90nm process design kit (PDK) was used to design 8-bit full adder with VBB technique in full custom methodology by using Synopsys Electronic Design Automation (EDA) tools. The simulation of 8-bit full adder was compared within a conventional bias technique and VBB technique with operating voltage of V_DD=0.2V supply. The result showed the reduction of VBB technique in term of peak power, P_peak=39% and average power, P_avg=30% compare with conventional bias technique. Moreover, the Power Delay Product (PDP) showed 1.29pJ in VBB technique compare with conventional bias mode 1.67pJ. The area size of 8-Bit full adder was 10μm×23μm.

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1. INTRODUCTION

In recent technologies, Very Large Scale Integration (VLSI) applications were grow advanced rapidly, such as image processing, video processing, Digital Signal Processing (DSP) and microprocessors that mostly used arithmetic operation. The full adder are fundamental circuits used for performing arithmetic operation. The designing of low power and high speed VLSI system has emerged as highly popular due to the fast growing technologies in mobile as well as other battery power applications.

The power consumptions were exponentially increased as the size of transistors was scaling down to sub-nanometer (nm) for higher density number of transistor in complex achievement and high performance circuit in a low area. The scaling down in MOSFET channel size is a big challenge for the Integrated Circuit (IC) designers as it doubles the density of transistor integration almost every two years based on Moore's law theorem.

When the MOSFET channel size been scaling, the subthreshold leakage current increases exponentially as threshold voltage (V_{th}) reduces. In a short channel transistor, the shorter channel length of transistor will be resulting in sub-threshold leakage current through at transistor when in the gate was not in switching mode. Low threshold voltage also results in increased sub-threshold leakage current because

transistors not able to turned OFF completely. Thus, the static power consumption will occur due to the leakage current when the transistor is under standby mode. As a result, it will consume leakage current dissipation, and these leakage current will dissipate in standby mode called static power. It was become a significant issues in the advance sizing technology of a transistor.

In a shorter channel length between Source and Drain of a MOSFET, it will reduce the transistor threshold voltage (V_{th}) to maintain a reasonable gate over drive. In the MOSFET V_{th} reduction, will result in an exponential increasing in the subthreshold current. Moreover, to control and minimize the Short Channel Effects (SCEs) and to maintain the transistor drive strength at low supply voltage, the oxide thickness is required to scale down. The aggressive scaling of oxide thickness will result in a high tunneling current through the transistor gate insulator.

2. LITERATURE REVIEW

In this section will review the previous work in design of 8-bit full adder with GDI circuit design technique and VBB low power design technique. The GDI circuit design implementation able to minimize the usage of transistor in designing full adder. Meanwhile, the VBB low power technique able to reduce the static power consumption by apply an external potential difference at the MOSFET body connection

2.1. Gate-diffusion Input (GDI) Technique

The GDI technique able to apply for low power digital circuit design which allows minimum chip area, delay and low power consumption to reduce the usage of transistor. GDI method is based on the use of a simple cell as illustrate in Figure 1. The GDI technique allows implementation of complex logic functions using only two transistors over a wide range application. The GDI standard cell is almost similar CMOS inverter. For instances, the standard cell connected to the two terminal namely N and P, so it can be randomly biased at contrast with CMOS inverter.

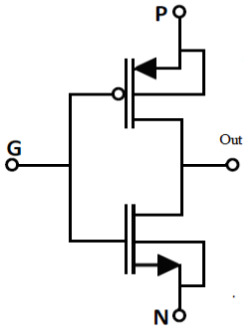

Figure 1. Schematic of GDI cell

The GDI design is more flexible as compared to the CMOS design. GDI cell consists of three inputs. The G indicate the gate input of NMOS and PMOS transistors where is the input switching signal been applied, second input P was connected to the source/drain of PMOS transistor and the last input N is connected to the source/drain of NMOS transistor. Body of NMOS transistor is connected to the input terminal N and body of PMOS transistor is connected to the input terminal P.

2.2. Variable Body Biasing (VBB) Technique

In MOSFET, the subthreshold leakage current occurs as the channel length become shorter, this scenario is different and causes Drain Induced Barrier Lowering (DIBL). The general equation for subthreshold leakage is:

$$I_{sub} = I_0 e^{(V_{GS}-V_T)/nV_{th}} \quad (1)$$

where $I_0 = \mu_0 c_{ox} \frac{W}{L} (n-1) {V_{th}}^2$, V_{GS} stands for gate-source voltage, V_T stands for thermal voltage (KT/q), n stands for subthreshold swing coefficient, V_{th} stands for threshold voltage, μ_0 stands for carrier mobility at zero bias, c_{ox} is the gate oxide capacitance, W and L are the effective width and length of transistor.

Typically, the bulk or body of a transistor can be control the threshold voltage based on the potential different been applied to the body. Thus, it can make a variation of threshold voltage as desired. The basic equation which shows how body bias impacts on threshold voltage V_{th} is:

$$V_{th} = V_{th0} + \gamma\left(\sqrt{2\emptyset_B - V_{SB}} - \sqrt{2\emptyset_B}\right) \quad (2)$$

In which the V_{th} is the threshold voltage, the $\emptyset_B$ stands for flat band voltage, γ stands for body effect coefficient, V_{th0} is the threshold voltage with zero substrate bias and V_{SB} is the source to body bias voltage. Based on (2), the V_{th0}, γ and $\emptyset$ are the constant element at which setting by the technology's parameter. Therefore, based on (2) the threshold voltage, V_{th} is directly proportional with the source to body bias voltage,V_{SB}, ($V_{TH} \propto V_{SB}$). Therefore, the body terminal of a MOSFET able to control the threshold voltage V_{TH}. In Figure 2 illustrate the conventional static CMOS connection and VBB technique connection logic design.

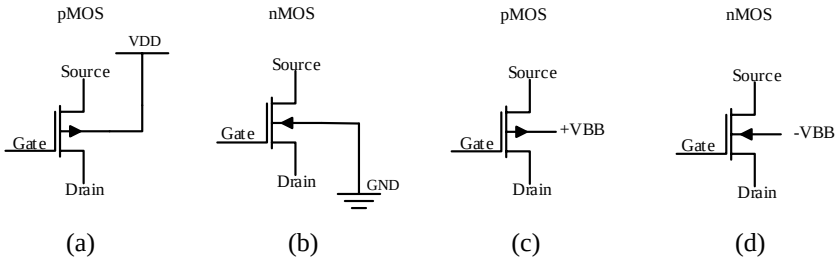

Figure 2. Body connection of logic design (a), (b) in conventional bias, (c), (d) in VBB technique

Nowadays, there are many IC design techniques to reduce power consumption such as power gating and so on. However, each technique provides an efficient way to reduce leakage power, but the drawback of each technique will affect the performance of a system. Therefore, this paper presents an idea Variable Body Bias (VBB) technique to reduce static power consumption in VLSI design.

3. OBJECTIVES

The main objective of this paper presents is to design a low power 8-bit Gate Diffusion Input (GDI) full adder by using Variable Body Biasing (VBB) technique. Thus, the sub-objectives are:

a) To design the low power 8-Bit full adder using VBB technique design in 90nm CMOS technology with two inputs are denoted by A and B with a carry in from previous lower significant figure, C_{in} and produce two outputs denoted by summation of two inputs, SUM and carry out, C_{out}.
b) Implement a low power full adder VBB technique and analyses by using Synopsys EDA tools for schematics entry simulation and layout design verification.
c) Simulate the 8-bit full adder VBB technique design with operating voltage, V_{DD}=0.2V in order to achieve the reduction of static power dissipation less than 1nW, propagation delay less than 30ns and minimize the size of layout in 90nm CMOS technology compare with other low power techniques.

4. METHODOLOGY

In this paper, the propose circuit design by using VBB technique can reduce the static power in an efficiently way. Basically, the body terminal for pMOS will to a voltage higher than V_{DD}, while in nMOS to a voltage lower than V_{SS} in order to reduce the leakage current. To be more understanding of VBB technique, a schematics of CMOS inverter with VBB technique circuit was carried out. Figure 3 illustrate an inverter design with VBB technique.

Figure 3 showing an inverter with the body terminal connected with an external potential supply source. Directly proportional increasing the potential different will make increasing of threshold voltage and affect performance. However, the VBB technique allows the bias to be applied dynamically by applied to potential difference at the body terminal. So during an active mode of operation the reverse bias is small, while in standby the reverse bias is stronger. Therefore, sub-threshold leakage current is able to reduce and thus reducing in static power dissipation.

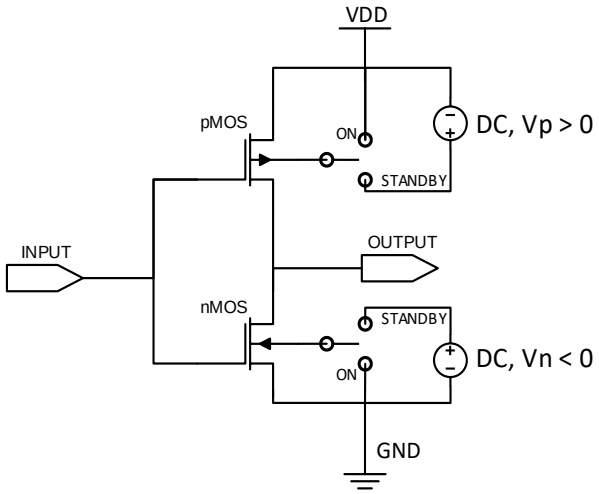

Figure 3. An inverter with VBB technique

Next, the implementation of VBB technique will be design in 1-bit GDI full adder before duplicate into 8-bit full adder. Typically, a full adder consists three input terminals and two output terminals. The 3 inputs are namely by A, B and a carry in, C_{in} will resulting 2 output namely as summation, SUM and carry out, C_{out}. The truth table of a full adder is shown in Table 1.

Table 1. Truth Table of a Full Adder

INPUT			OUTPUT	
A	B	C_{in}	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

From the truth table of full adder, the Boolean equation for SUM and C_{out} can be generated and solving with Karnaugh map to simplifier the equation efficiently. The equation for full adder is shown as below:

$$\begin{aligned} SUM &= A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC \\ &= (A \oplus B) \oplus C \end{aligned} \tag{3}$$

$$\begin{aligned} C_{out} &= AB + AC + BC \\ &= AB + C(A + B) \\ &= \overline{(\bar{A}+\bar{B})(\bar{C} + \bar{A}\bar{B})} \\ &= \overline{\bar{A}\bar{B} + \bar{C}(\bar{A} + \bar{B})} \end{aligned} \tag{4}$$

The number of transistors need to be reduce in order to achieve a low power consumption in a digital system. Conventionally, the number of pMOS pull-up network (PUN) and nMOS pull-down network (PDN) for a static CMOS full adder design must be equivalent. Based on (3) and (4), the static CMOS 1-bit full adder can be design in 28T (Transistor) based on the equation which is obtained by rearranging the SUM as show in (5):

$$SUM = ABC + (A + B + C)C_{out} \tag{5}$$

Furthermore, the pMOS PUN in the adder circuit is identical to the nMOS network according (5). The schematics of the static CMOS 1- bit full adder using 28T shown in Figure 4.

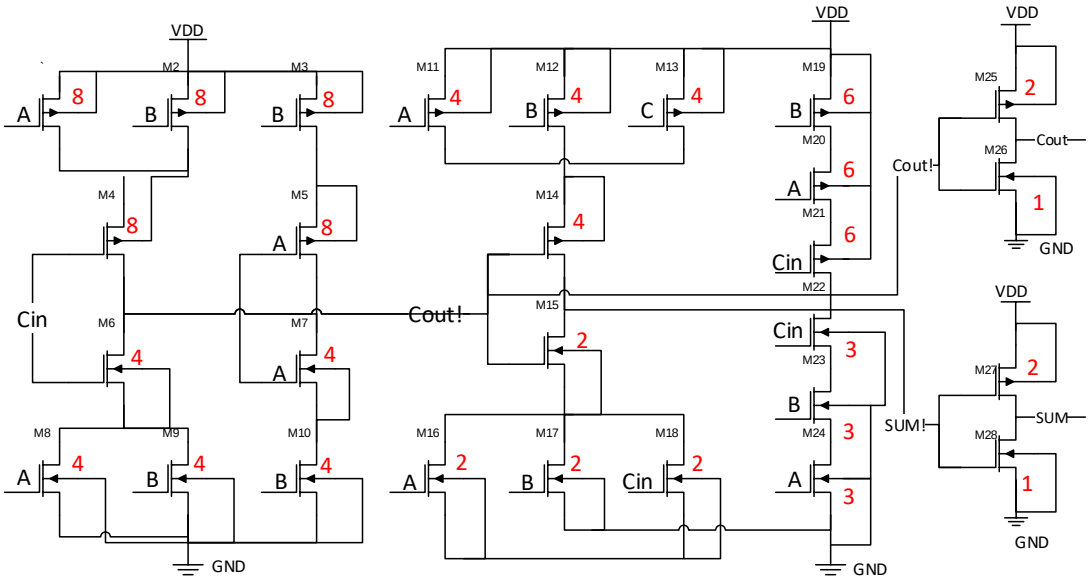

Figure 4. Static CMOS 28T 1- bit full adder

With the intention of further optimize and reduce the static power consumption, the GDI full adder was implement. This GDI full adder only using 8 Transistors (8T) to design, thus it can maintain the low complexity of full adder and reduce size of physical design.

The GDI 8T 1-bit full adder implement by using the two XOR logic gates and one MUX logic. In the existing system the XOR gates can be implemented with the help of three transistors. The three transistor XOR gate can be implemented with 2 units pMOS and 1 unit nMOS using the modified GDI technique. In the Figure 5 shows the 1-bit GDI full adder are used 8 transistors to design the schematic transistor level in conventional bias.

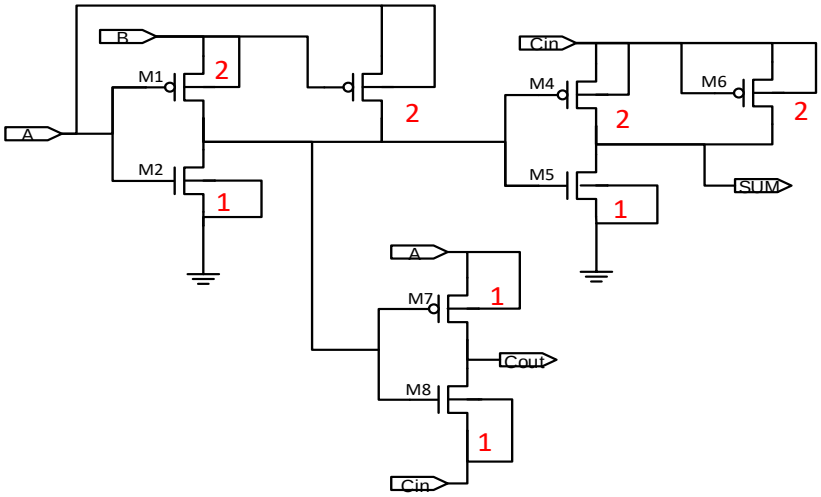

Figure 5. GDI 8T 1-bit full adder

According to the Figure 5 illustrate the 3T first XOR gate output is (A⊕B) at the top left and right. The output of first XOR gate is connected to the input of next XOR gate. The output of second XOR gate generates the SUM signal of full adder ($A \oplus B \oplus C_{in}$). The carry signal output C_{out} is equal to the input A when first XOR gate output is equal to the zero and carry signal output C_{out} is equal to the input C_{in} when first XOR gate output is equal to the one.

The MOSFET width in designing the full adder size in term of (W/L) ratio were carried out based on the logical effort calculation to optimize the propagation delay. Table 2 shown the logical effort of basic common gate that will be used for design the full adder.

Table 2. Logical Effort of Basic Common Gates

Gate type	Number of inputs					
	1	2	3	4	5	n
Inverter	1					
NAND		4/3	5/3	6/3	7/3	(n + 2)/3
NOR		5/3	7/3	9/3	11/3	(2n + 1)/3

Conventionally in the 1-bit GDI full adder, the pMOS is connected to VDD and nMOS connected to ground. The logical effort was being calculate in achieve a minimum propagation delay for the design of GDI 8T 1-bit full adder as shown in Figure 5. The sizing in (W/L) ratio of transistors were illustrated in number in red font.

In this paper, the GDI full adder was applied with VBB technique whereby the body of pMOS and nMOS will be connected to an external source supply in order to provide a reverse bias in standby mode to reduce the sub-threshold leakage current. Figure 5 illustrated the schematics of 1-bit GDI full adder with VBB technique. 1-bit GDI full adder with VBB technique as shown in Figure 6.

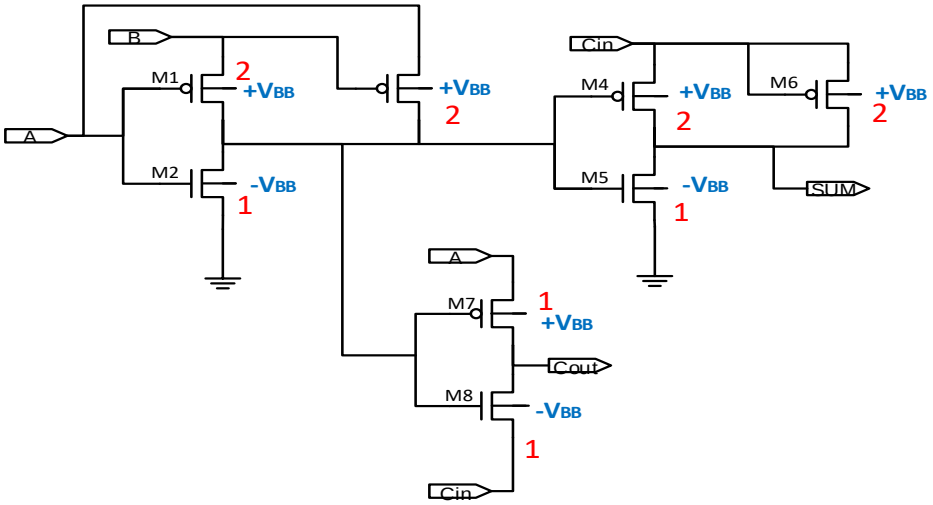

Figure 6. 1-bit GDI full adder with VBB technique

In the transistor level circuit design, the high threshold voltage MOSFET was been used to design the circuit. This is because the higher threshold voltages able to apply high bias voltages to the body terminal of the MOSFET. Therefore, when it was in standby mode, the static power will be reducing. During fabricate the high threshold MOSFETs methods involve adjusting the gate oxide thickness, gate oxide dielectric constant, or dopant concentration of the substrate in between the gate oxide and the polysilicon.

Next, the physical design was being drawn by using Synopsys EDA tools based on the stick diagram obtained from the Euler path. The design rule was strictly follow in order to achieve smaller size in physical area. The number of body connection indicate the total number of transistor being used. There are 5 pMOS and 3 nMOS in the circuit design. In the physical design the body was connected to the external source to achieve VBB technique bias. The metal layer used up to metal 2 which indicated by pink in color to minimize the size of layout. The Figure 7 illustrate the physical design of GDI 8T 1-Bit full adder.

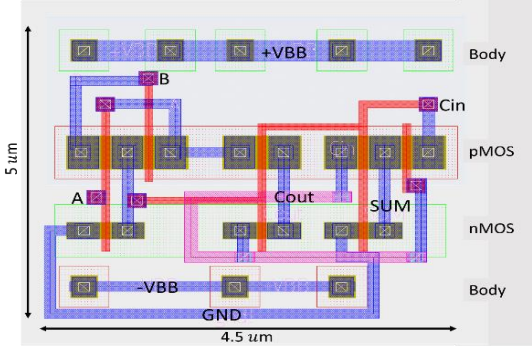

Figure 7. 1-bit GDI full adder

Next, the design will proceed with 8-Bit GDI full adder. The 1-Bit full adder will be used to duplicate in designing the 8-Bit full adder. For the 8-bit full adder will be designed in 4×2 array in order to minimize the size of area for layout interconnection and in the shape of square size. The Figure 8 illustrates the physical design of GDI 8T 8-Bit full adder.

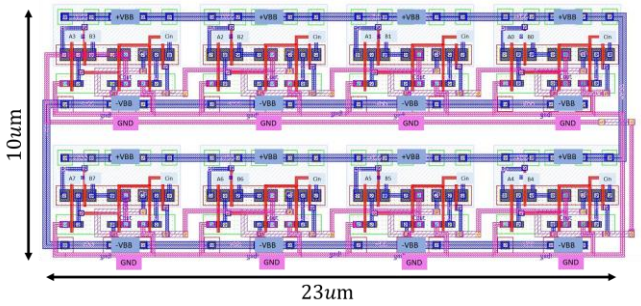

Figure 8. 8-bit GDI full adder

The physical design was continued with DRC and LVS verification to ensure the functionality of designed same as schematic design. Next, the parasitic extraction layout will be proceeding to observe the formation of parasitic capacitance and parasitic resistance in between different layer of interconnection.

5. RESULT AND DISCUSSION

The 1-bit GDI full adder and 8-bit GDI full adder was designed and simulated in Synopsis CMOS 90nm technology tools with the standardize operating voltage of $V_{DD} = 0.2V$. The functionality of designed 1-bit full adder was verified compared with truth table.

From the analysis results of 1-bit GDI full adder designed, the power consumption was reducing gradually with the decreasing usage of transistor. Besides that, in approach the VBB technique in the 1-bit GDI full adder design was successfully reducing the power consumption. However, there was increasing in delay due to less output driving capability because of the increase in threshold voltage V_{th} of the pMOS and nMOS.

The power performance of the 1-bit full adder was being analyses in term of propagation delay and power delay product (PDP) by compare with conventional bias technique and VBB technique. Table 3 shown the simulation result of 1-bit GDI full adder with standardize operating voltage of $V_{DD} = 0.2V$.

Table 3. Measurement Data of 1-bit GDI Full Adder

Measurement	Conventional Bias	VBB Bias
Peak Power (nW)	7.509	8.842
Average Power (nW)	1.321	0.5024
RMS Power (nW)	2.044	0.7414
Delay (ns)	7.42	10.2
PDP (pJ)	9.80182	5.12448

From the Table 3 result, the VBB technique was achieved 28% on reduction of average power consumption while there are increasing of delay. However, the PDP of VBB technique was achieved in least measurement value. Therefore, the applied of VBB technique able to reduce the static power consumption efficiently. For the GDI 1-bit full adder the size of layout is $5\mu m \times 4.5\mu m$.

Next the comparison of 8-bit GDI full adder was compare in between conventional bias and VBB technique bias. The Table 4 show the measurement comparison of 8-bit GDI full adder.

Table 4. Measurement Data of 8-bit GDI Full Adder

Measurement	Conventional Bias	VBB Bias
Peak Power (μW)	0.1851	0.1178
Average Power (nW)	58.39	25.15
RMS Power (nW)	66.32	28.17
Delay (ns)	28.6	51.3
PDP (pJ)	1.67	1.29

The analysis shown that the 8-bit GDI full adder using VBB technique bias was achieved reduction about 30% in the average power consumption. However, the delay was increasing in using VBB technique but the power delay product shown the least value compare with conventional bias. Thus, it shows that VBB technique can be reduce static power consumption by applied external potential different at the body terminal. The physical design of the 8-Bits GDI full adder with the size of $23\mu m \times 10\mu m (230\mu m^2)$ was completed.

6. CONCLUSION

In this paper, the design of low power 8-bit GDI full adder with variable body biasing (VBB) technique had been implemented in Synopsys EDA tools 90nm technology successfully. The VBB technique is one of the low power technique in VLSI design and able to reduce static power consumption efficiently.

The proposed full adder circuit design was implemented on conventional bias mode and VBB technique mode and comparison result in term of power consumption and proportional delay were carried out. The VBB technique shows the result achieved the reduction in term of peak power, $P_{peak} = 39\%$ and average power, $P_{avg} = 30\%$ in compare with conventional bias and VBB technique. However, in the VBB technique was increasing of propagation delay with 64% however in the power delay product (PDP) shows 1.29pJ compare with conventional bias mode 1.67pJ. The area size of 8-Bit full adder was $10\mu m \times 23\mu m$. Hence, from the comparisons, the proposed VBB technique is one of the best alternatives to achieve low static power consumption in VLSI design

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