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Influence of optimization of control factors on threshold voltage of 18 nm HfO2/TiSi2 NMOS

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ABSTRACT

This paper presents the influence of control factors as the process in development of 18 nm gate length NMOS transistor. The threshold voltage (VTH) can be minimized by optimal the control factors. Five control factors were selected through experiments. They are Adjustment VTH Implantation, Compensation Implantation, Compensation Energy Implantation, Source/Drain Implantation and Halo Implantation. While the two noise factors were introduced which are Phosphor Silicate Glass (PSG) temperature and Boron Phosphor Silicate Glass (BPSG) temperature to complete the combination with five control factors in process of Taguchi method L27 orthogonal array. The purpose of this research is to find the best value of interaction between combination controls factors and noise factors to achieve the best point of threshold voltage. In CMOS design, the threshold voltage is the benchmarking of physical parameter for determining the functional of transistor. The Virtual Wafer Fabrication SILVACO software was used to fabricate the 18 nm NMOS device. Hafnium Oxide (HfO2) and Titanium dioxide (TiO2) were utilized as the high-K materials and the Titanium Silicide (TiSi2) was utilized as metal gate. The statistics data are from the signal noise ratio (SNR) with nominal-the best (NTB) and the analysis of variance (ANOVA) of L27 orthogonal array are executed to minimize the variance of threshold voltage. The results show that the optimization and interaction method is achieved to perform the threshold voltage value with least variance is 0.3055 volts while the target value that is 0.302 ± 12.7% volts from value recommendation by the International Roadmap for Semiconductor prediction 2012.

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1. INTRODUCTION

Electronics would not be exist without semiconductor devices. Semiconductor device mark it possible to achieve the basic occupations of switching and amplification of signal. Bipolar junction transistor and the field effect transistor are two of the most significant semiconductor devices. The goal of MOSFET technology is to create smaller devices in order to put more devices to be fabricated on a single chip and it's also tends to be the essential of digital integrated circuit (IC). Through this, it makes great improvement of operation and performance of MOSFET. This situation can give a big advantage for operation of transistor especially it can save the time, energy and power consumption because the digital switching speed of transistor can be switched faster. The reduction size of MOSFET that required not only effected to all device dimensions to reduce proportionally, in term of the channel length, channel width and oxide thickness but it

also gives effect to the doping of the transistor. The researcher counter challenging to develop the smaller size transistor. The researcher are facing lots of problem that need to be taking a count in the scaling down of MOSFET such as carrier mobility dilapidation because of adulteration, severe gate tunneling effect with shrinking oxide thickness, the channel is getting shallower cause the p-n junction leakage current become higher and hot channel carrier [1]. More time, concentration and consistence need to be spend to make the transistor is function successfully. The threshold voltage (VTH) is one of the main difficulties in producing a nanoscale transistor is to control. If the VTH value is not achieved, it will affect the whole system of the device and worst case, the device will not function at all. It is caused the doping fluctuations [2]

Based on previous research, there are two ways to solve the problems above with the good combination between high-k dielectric and metal gate that is between HfO2 and TiSi2 [3]. Another solution is the optimization on process parameter using L27 Taguchi method. This paper is the continuation from the previous work where the 18 nm device design is optimized using the Taguchi method L27 orthogonal array for PMOS threshold voltage, VTH where the result shows that a 18 nm gate length PMOS transistor with VTH value of -0.302V that is well within ITRS 2011 prediction can be produced numerically [4].

In this work, to examine NMOS functionality and electrical characteristics 18nm NMOS with high-k materials and metal gate transistor was modeled and simulated. The NMOS fabrication process was executed by using SILVACO, ATHENA module whereas to verify the NMOS electrical characteristics device were performed by using ATLAS module simulator. In this work, the optimization process by using orthogonal array L27 Taguchi method needs only five important process parameters to be considered in the design of experiments with interaction. In the previous experiment, which studies the process by using the Taguchi L9 orthogonal array it can be concluded that the Halo Implantation was selected as dominant factor (factor E). This research was studying the effects of interactions (EXA), (EXB), (EXC) and (EXD) in determination of the optimal combination of control factors. The five parameters that desired to take as attention are Adjustment VTH Implantation, Compensation Implantation, Compensation Energy Implantation, Source/Drain Implantation and Halo Implantation as they get into do affect threshold voltage (VTH), in the fabrication of 18nm NMOS device. The Taguchi method involving analysis of control factor in which of the factors should be manipulated and finely adjusted to produce an improvement of results. By using an L27 orthogonal array, these could help to find out multiple manipulated factors on each characteristic and faster variation in a more economical way and save time [5].

2. RESEARCH METHOD

The fabrication process steps of 18 nm NMOS in Athena module from VWF are as follows. The first step in fabrication is a creating the initial substrate from a Silicon p-type (boron doped) with a doping $7x10^{14}$ atoms/cm^3 and orientation <100>. Next is to generate retrograde P-well by growing a dry oxygen 200 Å on the top of the substrate for 20 minutes with 970^{o}C and doped with Boron. The dose is $3.75x10^{12}$ atoms/cm^3 and energy implantation is 100KeV. This wafer has undergone the annealing process at 900^{o}C and it needs 36 minutes in Nitrogen and also 36 minutes in dry Oxygen. Next, the etched process was remove the masking oxide and create the Shallow Trench Isolation (STI) of 130-Å thickness in annealing process with dry Oxygen in 25 minutes at 900^{o}C. Then followed by a Low Pressure Chemical Vapor Deposition process (LPCVD) and Reactive Ion Etching (RIE) process. The Phosphor Silicate Glass (PSG) was developed on top of substrate after wafer is undergoing the annealing process at 850^{o}C for 15 minutes. After complete the process of growing and annealed 1.1 nm Gate Oxide Thickness (TOX), the Boron Di-fluoride (BF2) with $1.67577x10^7$ atoms/cm^3 Boron and the energy 5KeV with a tilt angle of 7^o was implanted at the N-well active. Followed by deposition process of insulator that is Hafnium dioxide (dielectric permittivity HfO2, □opt = 22) on top of bulk Silicon. In this research the length of HfO2 material was 18 nm and on the top of the insulator was the deposition process of gate material, Titanium Silicide (TiSi2). The NMOS device, Indium with dose $13.300x10^{13}$ atoms/cm^3 at 30° angle and energy, 290KeV was used in Halo Implantation process. By using chemical vapor deposition process, the side wall spacer was develop with a 0.047μm Silicon Nitride layer. Again, arsenic with a dosage of $4.0x10^{12}$ atoms/cm^3 was used in Source/Drain Implantation process followed by phosphorous with a dosage of $1.75x10^{12}$ atoms/cm^3. Next process is to develop a 0.3 □m layer of Boron Phosphor Silicate Glass (BPSG) and followed by the annealing process of structure at 850^{o}C. The last implantation process is Compensation Implantation with Phosphorous dose of $2.5x10^{13}$ atoms/cm^3. Last but not least, the process of deposition the Aluminum material on top of the structure and etching accordingly to form metal contacts for Source and Drain [6-7]. Then, the transistor undergoes the ATLAS module to measure the electrical characteristic in order to study the threshold voltage, VTH of the device with reference to ITRS 2011 [8]. The complete diagram of 18 nm gate length structure as shown in Figure 1.

In this section, Taguchi method L27 orthogonal array is used to study and modeling of variability of

18 nm NMOS device performance with five relevant process parameters with different levels as shown in Table 1. Meanwhile, the two noise factors are Phosphor Silicate Glass (PSG) temperature and Boron Phosphor Silicate Glass (BPSG) temperature were varied with 2 levels are listed in Table 2. Based on the Taguchi L27 orthogonal array that is the 27 experiments were generated from the combination between five process parameters with two noise factors to get the four readings of threshold voltage (VTH) for every row of experiment.

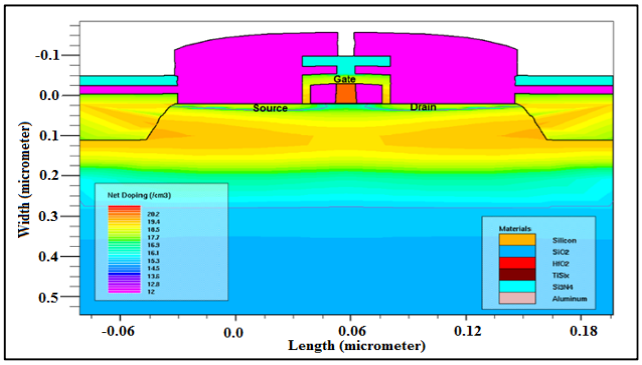

Figure 1. A doping profile of the NMOS 18 nm gate length

Table 1. Control Factors and their Ranges

Symbol	Control Factor	Unit	Level 1	Level 2	Level 3
A	Adjustment VTH Implantation	atom/cm^3	2.00x10^{10} [A1]	10.00x10^{10} [A2]	18.0x10^{10} [A3]
B	Compensation Implantation	atom/cm^3	4.50x10^{12} [B1]	6.00x10^{12} [B2]	8.50x10^{12} [B3]
C	Compensation Energy Implantation	KeV	30 [C1]	40 [C2]	50 [C3]
D	Source-Drain Implantation	atom/cm^3	4.00x10^{12} [D1]	12.00x10^{12} [D2]	20.00x10^{12} [D3]
E	Halo Implantation	atom/cm^3	15.00x10^{12} [E1]	15.60x10^{12} [E2]	16.20x10^{12} [E3]

Table 2. Noise Factor and its Ranges

Symbol	Noise factor	unit	Level 1	Level 2
X	PSG Temperature	°C	845 [X1]	850 [X2]
Y	BPSG Temperature	°C	850 [Y1]	855 [Y2]

3. RESULTS AND ANALYSIS

The results of VTH were analyzed and processed using the Taguchi L27 orthogonal array method with two combinations of main factors to get the optimal design. Then, the optimized results were simulated again using ANOVA analysis and the last confirmation stage from Taguchi method in order to verify the predicted optimal and finally to get the accurate result. Below are the process of optimization process parameters using Taguchi L27 orthogonal array.

By using the specified Taguchi's L27 orthogonal array table, there were twenty-seven experiments were performed with the combination design parameters in Table 1 and Table 2 respectively. Four specimens were simulated for each of the parameter combinations to produce the completed response for VTH and the data is listed in Table 3. The next step was to determine the significant control factors that gives more effectiveness to the device characteristics. Therefore, the best solution is using the Signal-to-Noise ratio, (SNR) to find out the optimal process parameters and analyze the experimental data. Hence, the larger SNR corresponds to present the better performance characteristic [9]. As a result, the optimal level of the process parameter is the level with the highest SNR [10-11]. VTH values in Table 3, the data of mean (μ), variance (σ2) and Signal-to-Noise (SNR) Nominal-the-Better (NTB), □ can be calculated by using the formulas below [12]:

$$\text{SNR (NTB)}, \square_{NTB} = 10\ \text{Log}_{10}\left[\frac{\mu^2}{\sigma^2}\right] \quad (1)$$

$$\text{Where: Mean}, \mu = \frac{Y_i + \ldots\ldots + Y_n}{n} \quad (2)$$

$$\text{Variance}, \square\square \frac{\sum_{i=1}^{n}(Y_i - \mu)^2}{n-1} \quad (3)$$

Based on the (1), (2) and (3), n is the number of tests, Y is the experimental value of the VTH. As shown in (1) and (2) are the formulas to calculate mean values and variance values respectively. By applying the both formulas, the SNR (NTB), □ for the NMOS device was calculated and the results were listed in Table 3. In this work, the threshold voltage of the 18 nm device belongs to the Nominal-the-Better quality characteristics.

Table 3. 18 nm NMOS Statistical Result-Taguchi L27 Orthogonal Array

Exp.No	Threshold voltage				Mean	Variance	SNR (Nominal-the Better),□□□dB
	X_1Y_1	X_1Y_2	X_2Y_1	X_2Y_2			
1	0.259553	0.246368	0.254636	0.245685	0.251561	4.494E-5	31.49
2	0.257864	0.245786	0.257864	0.245786	0.251825	4.863E-5	31.15
3	0.277843	0.267783	0.277913	0.267791	0.2728325	3.394E-5	33.41
4	0.263242	0.256632	0.263242	0.256324	0.259860	1.511E-5	36.46
5	0.263268	0.256326	0.268162	0.256815	0.2611428	3.191E-5	33.30
6	0.232432	0.213123	0.232432	0.213123	0.2227775	1.243E-4	26.01
7	0.326326	0.312531	0.326326	0.312531	0.3194285	6.343E-5	32.06
8	0.326437	0.312537	0.326437	0.312537	0.319487	6.441E-5	32.00
9	0.265348	0.253485	0.265349	0.253492	0.2594185	4.689E-5	31.57
10	0.258441	0.247844	0.253847	0.235478	0.2489025	9.892E-5	27.97
11	0.248327	0.232732	0.248327	0.232732	0.2405295	8.107E-5	28.53
12	0.243749	0.237493	0.243749	0.237494	0.2406213	1.304E-5	36.47
13	0.323269	0.312326	0.323269	0.321326	0.3200475	2.734E-5	35.74
14	0.258683	0.245868	0.258691	0.245869	0.2522778	5.477E-5	30.65
15	0.380273	0.372926	0.380273	0.372967	0.3766098	1.789E-5	38.99
16	0.367527	0.356752	0.367527	0.356752	0.3621395	3.87E-5	35.30
17	0.374023	0.363402	0.374023	0.363402	0.3687125	3.76E-5	35.58
18	0.382498	0.378249	0.382498	0.378249	0.3803735	6.018E-6	43.81
19	0.326329	0.312563	0.326832	0.312563	0.3195718	6.673E-5	31.93
20	0.328702	0.312872	0.328711	0.312871	0.320789	8.358E-5	30.90
21	0.243253	0.232532	0.243253	0.232532	0.2378925	3.831E-5	31.69
22	0.328314	0.312831	0.328314	0.312831	0.3205725	7.993E-5	31.09
23	0.265299	0.252995	0.265290	0.259959	0.2608858	3.399E-5	33.01
24	0.268107	0.256811	0.268114	0.256811	0.2624608	1.28E-4	32.09
25	0.332932	0.321582	0.332179	0.321742	0.3271088	3.966E-5	34.31
26	0.296322	0.286932	0.293241	0.286932	0.2908568	2.245E-5	35.83
27	0.327323	0.312302	0.327323	0.312302	0.3198125	7.521E-5	31.34

The SNR (Nominal-the-Better), □□data from Table 3 is computed based on the SNR analysis to determine which the level of the proses parameters that influence to the changing of the characteristics of the device. The calculation data is shows in Table 4.

Table 4. Result of SNR (NTB), □ Proses Parameters

Factor	Control Factor	SNR (NTB),dB			Overall SNR (NTB),dB
		Level 1	Level 2	Level 3	
A	Adjustment VTH Implantation	31.94	34.78	32.47	
B	Compensation Implantation	31.51	33.04	34.64	
C	Compensation Energy Implantation	34.10	32.25	32.84	33.06
D	Source/Drain Implantation	33.66	33.89	31.65	
E	Halo Implantation	32.93	32.33	33.93	

Through this information, the dominating factor can be determined from the highest values SNR (NTB), □ in every factor. The highest SNR (NTB) means the better quality characteristic of threshold voltage, VTH [13]. Refer to Table 4, A2, B3, C1, D2 and E3 as the dominator factor for factor A, factor B, factor C, factor D and factor E respectively. The average values of SNR (NTB) data is 33.06 dB and the evaluation result without interactions process is A2 B3 C1 D1 E3.

In this section for analysis of ANOVA result with interaction, Taguchi L27 orthogonal array was used to optimize the process parameters variation in 18 NMOS device with considering the interaction effect between factor A, factor B, factor C, factor D with factor E. The aim is to calculate the average value of the interaction of factor E that is Halo Implantation (E1, E2, E3) with other factors such as Adjustment VTH Implantation (A1, A2, A3), Compensation Implantation (B1, B2, B3), Compensation Energy Implantation (C1, C2, C3), and Source/Drain Implantation (D1, D2, D3). Based on the interaction formulae, all the data were transfer to the graphs and study the interactions between process parameters to SNR (NTB) as shown in Figure 2 until Figure 5. The presence of interaction through graphs can be observed by the existence of lines that intersect and inconsistency among the factors involved.

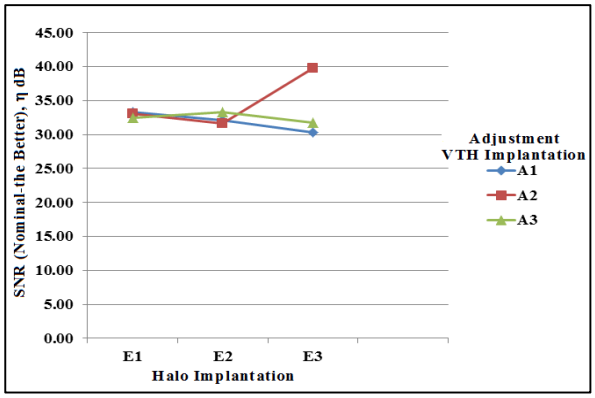

Figure 2. The interaction between Halo Implantation and Adjustment VTH Implantation

Figure 2 shows the graph interaction between Adjustment VTH Implantation (factor A) and Halo Implantation (factor E). The graph shows 3 lines, which are A1, A2 and A3 are intersect. So determined the highest SNR (NTB) level on lines that intersect with factor E3 is A2 (39.76 dB).

Refer to Figure 3 also shows the interaction between Compensation Implantation (factor B) with Halo Implantation (factor E). From the graph for SNR (NTB), there have interaction between lines B1, B2 and B3. From the graph, the highest SNR (NTB) level that intersection with E3 parameter is B3 (35.57 dB).

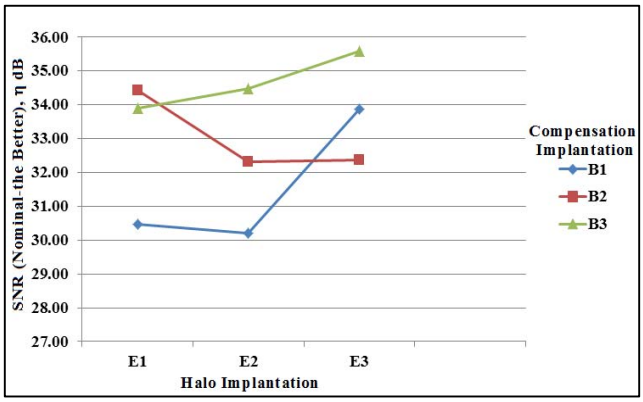

Figure 3. The interaction between Halo Implantation and Compensation Implantation

Figure 4 shows the interaction result between Compensation Energy Implantation (factor C) and Halo Implantation (factor E). The graph shows 3 lines which are C1, C2 and C3 are crossed to each other at E1 level. Between level E2 and level E3, the line C2 is intersect with line C3. Result shows the higher value of SNR (NTB) of Compensation Energy Implantation is interaction with Halo implantation is C1 with 36.44 dB.

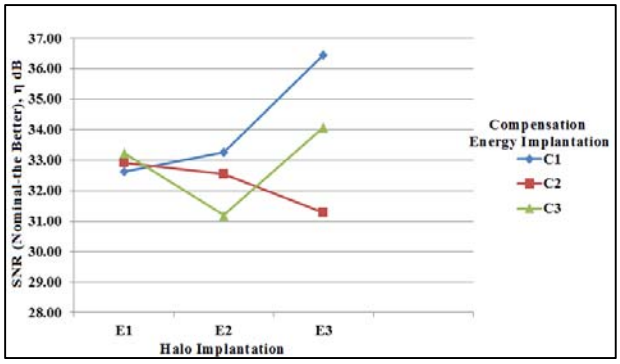

Figure 4. The interaction between halo implantation and compensation energy implantation

Figure 5 shows the SNR (NTB) interaction between Source/Drain Implantation (factor D) and Halo Implantation (factor E). The graph displays the 2 lines are crossing to each other which are between line D1 and line D2 at level E1. The highest value of SNR (NTB) for Source/Drain Implantation is D2 with 34.56 dB. Based on information analysis above, the optimum combination for VTH value of 18 nm NMOS device that takes into account the effect of interaction is A2 B3 C1 D2 E3.

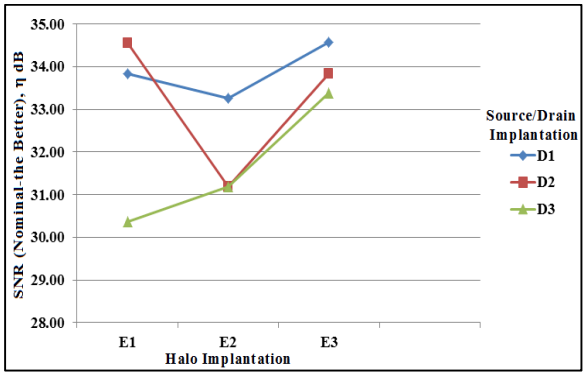

Figure 5. The interaction between Halo Implantation and Source/Drain Implantation

3.1. Confirmation Test

The end of the simulation with the noise factor of the final test verification should be carried out to verify the accuracy of the forecast Taguchi method. The combination of optimum control factors A2 B3 C1 D1 E3 are listed in Table 5.

Table 5. Combination of Optimum L27 Analysis for 18 nm NMOS

Symbol	Control factor	Unit	Level	Best Value
A	Adjustment VTH Implantation	atom/cm^3	2	10.00 x 10^{10}
B	Compensation Implantation	atom/cm^3	3	8.50 x 10^{12}
C	Compensation Energy Implantation	keV	1	30
D	Source-Drain Implantation	atom/cm^3	1	4.00 x 10^{12}
E	Halo Implantation	atom/cm^3	3	16.20 x 10^{12}

Table 6 shows the lists of the percentage difference between the results of the combination without the interaction and combination with interaction during device optimization process is carried out, which it refers to the nominal value projected by ITRS 2012. The final decision analysis methods in designing model L27 Taguchi 18 nm NMOS device shows that the two experiments in which the interaction or without interaction take effect of VTH value within the range of the nominal value (0.302 □ 12.7% volts). However, the percentage of the experiment that takes into account the effect of the interaction is better than nominal values without taking interaction with 1.16%. Analysis shows that the key factor or factor E in this Halo Implantation dosage factor had interaction with other control factors.

Table 6. Analysis of Percentage Threshold Voltage, VTH 18nm NMOS

	Before Interaction	After Interaction	ITRS value
Noise Factor (^{0}C)	X2,Y2	X2,Y2	0.302 □□□□□□□□ volts
Combination of optimum factors	A2 B3 C1 D2 E3	A2 B3 C1 D1 E3	
Threshold voltage, VTH	0.3152 volts	0.3055 volts	
Percentage from nominal value	4.37%	1.16%	

4. CONCLUSION

This research proves that the threshold voltage is effected by the control factors, VTH of 18 nm NMOS transistor was successful found together with the optimal factors level predicted by Taguchi method. Halo Implantation factor has been identified as key factor had interaction with other control factors such as Compensation Implantation, Compensation Energy Implantation, Source/Drain Implantation. Therefore, it has been proven that 18 nm transistor can be achieved produced the VTH value is well within the ITRS 2012 requirements of 0.302 ± 12.7% volts.

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