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Compact modeling of strained GAA SiNW

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ABSTRACT

Strain-based on advanced MOSFET is a promising candidate for the future of CMOS technology. A numerical model is not favorable compared to a compact model because it cannot be integrated into most simulator software. Thus, a compact model is proposed to overcome the shortcomings in the analytical model. In this paper, a charge-based compact model is presented for long-channel strained Gate-All-Around Silicon Nanowire (GAA SiNW) from an undoped channel to a doped body. The model derivation is based on an inversion charge which has been solved explicitly using the smoothing function. The drain current model is formulated from Pao Sah's dual integral which is formed in terms of inversion charge at the drain and source terminals. The proposed model has been extensively verified with the numerical simulator data. The strained effect on the electrical parameters are studied based on inversion charge, threshold voltage and current-voltage (I-V) characteristics. Results show that the current, the inversion charge and the threshold voltage can be greatly improved by the strain. The threshold voltage was reduced approximately 40% from the conventional GAA SiNW. Moreover, the inversion charge was improved by 30 % and the on-state current has doubled compared to unstrained device.

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1. INTRODUCTION

An advanced MOSFET such as Gate-All-Around SINW (GAA SiNW) is introduced to overcome the shortcomings in the conventional MOSFET. The architecture of the gate completely surrounding the channel in GAA SiNW allows the device to have excellent gate control and able to minimize the short channel effects [1-2].

To understand the behavior of the device, an analytical model is required [1-10]. However, this modeling method is impractical because it is unable to extend into the circuit level simulator. The models need to be solved iteratively and this function(iteration) not provided in the circuit simulator such as Hspice. As a result of this limitation, more compact modeling works have been proposed which are needed for the design and characterization of the GAA SiNW at circuit level [14-19].

There is extensive literature on improving the model for a different condition such as undoped and doped body channel [2-10]. However, there is little work on device modeling using strain on GAA structure. From previous studies, strain-based on Ge fraction is used to boost up the current and lowering the threshold for conventional and advanced MOSFET structures [17-23]. For strain application in GAA structures, the existing models have used the analytical approach [22-23]. However, the model is limited to the threshold and is not enough to analyse the strain behaviour.

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In order to enable the extension of the strained GAA into the circuit level, a compact model approach is introduced. In this paper, we present a compact model for strained GAA SiNW. This model can be derived from the analytical model and solved explicitly using the smoothing function. The model was incorporated with the interfaced trapped charge and fixed oxide charge. Moreover, the model is also valid for a practical range of doping. We have considered a long channel device to focus the effect of strain on device behaviour. This work can be used as a core model for strained GAA device. To validate our model, results are compared with publishing work and three-dimensional (3D) simulations obtained using Technology Computer Aided Design (TCAD) software.

2. MODELING OF STRAINED GATE ALL-AROUND SILICON NANOWIRE

Figure 1 illustrates the schematic diagram of the proposed model using the explicit method. In this model, fixed oxide $(\phi_f = v_{th} \ln(N_A/n_i))$ charge is considered to enumerate the actual fabrication environment especially for a thin oxide layer. The diameter and channel are defined at r-direction and y-direction, respectively.

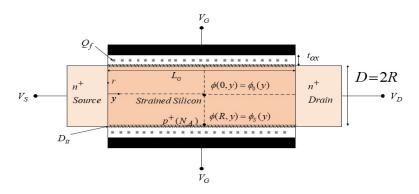


Figure 1. Cross sectional diagram for n-type strained Gate All Around GAA SiNW

One dimensional (1D) Poison-Boltzmann for GAA SiNW Figure 1 can be represented in cylindrical coordinate as

$$\frac{1}{r}\frac{d}{dr}\left(\frac{rd\phi}{dr}\right) = q\frac{N_a}{\varepsilon_{si}}(1 + e^{\beta(\phi - V_{ch} - 2\phi_f)})$$
(1)

where r and ϕ are defined as the radial of the GAA and potential at the channel region due to gate biasing. The constant, $^{\beta}$, is defined as $^{1/\nu_{th}}$, where $^{\nu_{th}}$ is the thermal voltage. This model can be used for both the undoped and doped channel. The quasi-fermi potential along y-axis (channel) is assumed as constant and fermi potential can be explicitly calculated as $^{\phi_f} = ^{\nu_{th}} \ln(N_A/n_i)$ with intrinsic doping body, $n_i = 1.45 \times 10^{10} cm^{-3}$. The potential at the surface (ϕ_s) and center region (ϕ_o) can be determined using the following boundary conditions:

$$\frac{\delta\phi}{\delta r}\Big|_{r=0} = 0, \ \phi_{(r=0)} = \phi_0, \ \phi_{(r=R)} = \phi_s$$
 (2)

The vertical electric field (E_s) at the surface can be formulated as

$$-E_s = \frac{d\phi}{dr}\bigg|_{r=R} = \frac{Q_{inv} + Q_{dep}}{\varepsilon_{si}}$$
(3)

where q_{inv} and q_{dep} are inversion charge and depletion at the channel. By solving equation (2) and (3), the changes of potential at r-direction can be simplified as

$$\frac{d\phi}{dr} = \frac{Q_{dep}}{\varepsilon_{si}} + \frac{2Q_{dep}}{R} \left(\frac{1}{Q_{dep} + q_{inv}}\right) e^{\frac{\phi_s - V_{ch} - 2\phi_f}{v_{th}}} \left(1 - e^{\frac{\phi_s - V_{ch} - 2\phi_f}{v_{th}}}\right)$$
(4)

The final solution of surface potential can be represented as

$$\phi_{s} = 2 \phi_{f} + V_{ch} + v_{th} \ln(Q_{in}) + v_{th} \ln(\frac{R}{v_{th} \varepsilon_{si}}) + v_{th} \ln(1 + \frac{Q_{in}}{Q_{dep}}) - v_{th} \ln(e^{\frac{-qN_{a}R^{2}}{4\varepsilon_{si}}} (e^{\frac{-qN_{a}R^{2}}{4\varepsilon_{si}}} - 1))$$
(5)

where $q_{dep}' = C_{ox}v_{th}/H'$ is defined in terms of the doping effect (H') and structural parameter which were taken from [16-17]. From the Gauss Law, the charge can be calculated as

$$Q_t = C_{ox}(V_{GS} - V_{fb} + \frac{Q_f}{C_{ox}} - \phi_S \eta)$$
(6)

where $^{C_{ox}}$ is the oxide gate capacitance, $^{V_{fb}}$ is the flatband voltage and $^{\eta}$ is the variable related to the interfaced trapped charge which is significant at heavily body doping ($^{\eta=1+qD_{it}/C_{ox}}$). Thus, for undoped and lightly doped cases, $^{\eta}$ can be set as 1[10]. The equation in (6) can be rearranged to form a unified charge control model (UCCM) adapted from [11] by replacing the equation (5) into equation (6). The final form of UCCM model can be formulated as

$$\frac{Q_{in}}{C_{ox}} + \eta v_{th} \ln(Q_{in}) + \eta v_{th} \ln(1 + \frac{Q_{in}}{Q_{dep}}) = V_{GS} - V_0 - \eta V_{ch}$$
(7)

where V_0 is the threshold voltage for GAA SiNW can be explicitly calculated as

$$V_{0} = \Delta \phi + 2 \phi_{f} - \frac{Q_{f}}{C_{ox}} + \frac{Q_{dep}}{C_{ox}} + \eta v_{th} \ln \left(\frac{R}{2 v_{th} \varepsilon_{si}}\right)$$
$$- \eta v_{th} \ln \left[1 - \exp \left(\frac{-q N_{a} R^{2}}{4 \varepsilon_{si}}\right)\right]$$
(8)

Meanwhile, the threshold voltage with strained effect can be formulated as

$$V_{0_strain} = V_{fb_strain} + \phi_{s_strain} + \frac{Q_{dep}}{C_{ox}} + \eta v_{th} \ln\left(\frac{R}{2v_{th}\varepsilon_{si}}\right) - \eta v_{th} \ln\left[1 - \exp\left(\frac{-qN_{a}R^{2}}{4\varepsilon_{si}}\right)\right]$$
(9)

where V_{fb_strain} and ϕ_{s_strain} are the strain parameter based on Ge fraction (x) which can be found in [17-18]. The new form of UCCM model with strain can be represented as

$$V_{GS} - V_{0_strain} - V_{ch} - \eta v_{th} \ln(q_{dep}') = \frac{Q_{in}}{C_{ox}} + \eta v_{th} \ln(\frac{Q_{in}}{Q_{dep}'}) + \eta v_{th} \ln(1 + \frac{Q_{in}}{Q_{dep}'})$$
(10)

The implicit equation from (7-8) can be solved explicitly using the following function as suggested in [13]:

$$f(z; s, G) = \ln(\sqrt{z + z^2}) + sz - G = 0$$
(11)

The final solution of function g can be represented as

$$z = \sqrt{\left(\frac{1}{2s^2}\right)^2 + \left(\frac{1}{s}\right)^2 \ln^2(1 + e^G)} - \frac{1}{2s^2}$$
 (12)

where z is the explicit form of function g which can be applied on UCCM model to solve the charge model just like in [11]. Thus, the initial and final solution of explicit charge model for strained GAA SiNW can be represented as

$$Q_{in_0} = -\frac{2\eta^2 C_{ox}^2 v_{th}^2}{Q_{dep'}}$$

$$+ C_{ox} \sqrt{\left(\frac{2\eta^2 C_{ox}^2 v_{th}^2}{Q_{dep'}}\right)^2 + 4\eta v_{th}^2 \ln^2 \left(1 + \exp\left[\frac{V_{GS} - V_{0_strain} - \eta V_{ch}}{2\eta v_{th}}\right]\right)}$$
(13)

$$Q_{in} = -\frac{2\eta^{2}C_{ox}^{2}v_{th}^{2}}{Q_{dep'}} + C_{ox}\sqrt{\left(\frac{2\eta^{2}C_{ox}^{2}v_{th}^{2}}{Q_{dep'}}\right)^{2} + 4\eta v_{th}^{2} \ln^{2}\left(1 + \exp\left[\frac{V_{GS} - V_{th}_{f} - \eta V_{ch}}{2\eta v_{th}}\right]\right)}$$
(14)

where $V_{th}f_{-}f$ is the final explicit threshold based on initial inversion charge and depletion charge is formulated as

$$V_{th_{f}} = V_{0_{strain}} + 2\eta v_{th} \ln(1 + \frac{Q_{in_{0}}}{Q_{o}})$$
(15)

The current model can be derived from the following equation as

$$I_{DS}dy = \mu 2\pi Rq_{in}.dV_{ch} \tag{16}$$

where μ is the mobility for the electron or hole, R is the radius of the channel, and V_{ch} is the fermi potential which varies from source to drain along the channel. By solving the equation (15), the final drain current model is simplified as

$$\begin{split} I_{DS} &= \mu \, \frac{2\pi \, R}{L_G} \Bigg[\, 2 \, v_{th} \, (Q_{ins} - Q_{ind}) + \frac{1}{2 \, C_{ox}} (Q_{ins}^2 - Q_{ind}^2) \, \Bigg] \\ &+ \mu \, \frac{2\pi \, R}{L_G} \Bigg[\, v_{th} Q_{dep} \, \ln \big(\frac{Q_{ind} + Q_{dep}}{Q_{ins} + Q_{dep}} \big) \, \Bigg] \end{split}$$

(17)

3. RESULTS AND ANALYSIS

Figure 2 shows the comparison results of current-gate voltage (ID-VG) graph between the implicit model in (7) and proposed model in (13) which have been solved explicitly for unstrained GAA SiNW. The proposed model is considerably valid because both models indicate similar trends as can be seen in Figure 2(a) and Figure 2(b). The proposed model is then extended for strain application at the channel area of GAA SiNW.

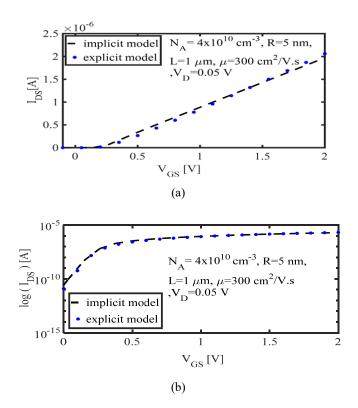


Figure 2. I_{DS} - V_{GS} characteristic of implicit and explicit of GAA SiNW with $Q_f = 3 \times 10^{10} \, cm^{-2}$ (x=0) (a) Linear scale (b) Log scale

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Another validation method is performed to identify the compatibility of strain in the proposed model (equation (14)). Figure 3 indicates that the I-V curves of both model and simulator agreed well (using Ge fraction, x=0.4). The significant outcomes prove that the model is applicable for strain device.

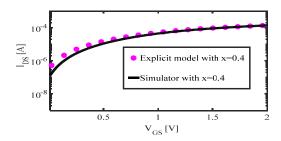


Figure 3. I_{DS} - V_{GS} characteristic of explicit model and simulator for strained GAA SiNW $(N_A = 5 \times 10 \text{ cm}^{-3}, t_{ox} = 2 \text{ nm}, L = 1 \mu \text{m}, V_D = 1V)$

The dependence of Id-Vg on strain is presented in Figure 4. The results indicate that the current is increased significantly as the strain levels are varied from x=0 to x=0.4. The current increment is almost doubled compared to the unstrained device. Other than that, with the strain application, the threshold voltage also shows a great improvement when operating voltage is reduced by ~ 40 % even without a further downscaling on its dimension. The trend of the on current and threshold changes align with reported data from [17-18,20]. From these findings, device performance is significantly improved with strain application.

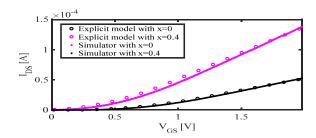


Figure 4. IDS-VGS characteristic of strained GAA SiNW for different strain level $(N_A = 5 \times 10^{10} \text{ cm}^{-3}, t_{ox} = 2 \text{ nm}, L = 1 \mu \text{m}, V_D = 1V)$

The current increment due to strain can be justified using charge density of electrons. Charge density dependence on the strain can be observed in Figure 5 with different levels of body doping. The concentration of carriers is increased by 30 % as the strain level is increased from $2.7 \times 10^{-6} \ C/cm^{-2}$ to $3.5 \times 10^{-6} \ C/cm^{-2}$, as shown in Figure 5(a) for undoped body. This increment will lead to current enhancement and improve the switching speed improvement of the device. Meanwhile, when the channel was doped with $1 \times 10^{15} \ cm^{-3}$, the carriers reduced from $2.8 \times 10^{-6} \ C/cm^{-2}$ Figure 5(a) to $2.2 \times 10^{-6} \ C/cm^{-2}$ Figure 5(b) at x=0. However, the lost carriers compensated by the strain(x=0.4).

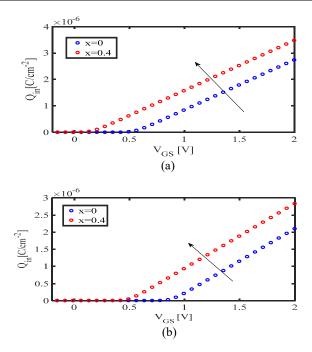


Figure 5. Q_{in} - V_{GS} characteristics of strained GAA SiNW for different strain at (a)undoped body (b) doped body $(N_A = 2 \times 10^{15} cm^{-3}, t_{ox} = 2 nm, L = 1 \mu m, V_D = 0.6V)$

4. CONCLUSION

In this work, compact modeling of strained GAA SiNW is presented and the results are compared to the unstrained device. The compact model technique has been extended for strain application resulting in better electrical properties compared to conventional GAA SiNW. The proposed model has been verified with the numerical model and 3D simulator data. By inducing strain in the channel area, the electrical properties of the device have improved significantly including on current, threshold voltage, and charge carrier density. The on current is doubled up compared to the unstrained channel. In addition, threshold voltage was reduced by 40 % depending on the Ge fraction. Besides, the inversion charges were also affected by the strained effect due to the carrier density enhancement with the increment of 30 %.

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REFERENCES

- [1] C. P. Auth and J. D. Plummer, "Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's," IEEE Electron Device Lett., vol. 18, no. 2, pp. 74–76, 1997.
- [2] D. Jimenez, B. Iníguez, J. Sune, L. F. Marsal, J. Pallares, J. Roig, and D. Flores, "Continuous analytic I-V model for surrounding-gate MOSFETs," IEEE Electron Device Lett., vol. 25, no. 8, pp. 571–573, 2004.
- [3] B. Yu, W.Y. Lu, H. Lu, and Y. Taur, "Analytic Charge Model for Surrounding-Gate MOSFETs," IEEE Trans. Electron Devices, vol. 54, no. 3, pp. 492–496, 2007.
- [4] N. K. Cho, S. H. Choi, N. H. Kim, S. H. Kim, and Y. S. Yu, "Continuous analytic current-voltage (I-V) model for long-channel doped surrounding-gate MOSFETs (SGMOSFETs)," in Proceedings - 2008 International Conference on Advanced Technologies for Communications, ATC 2008, Held in Conjunction with REV Meeting, 2008, pp. 315–318.
- [5] J. He, Y. Tao, F. Liu, J. Feng, and S. Yang, "Analytic channel potential solution to the undoped surrounding-gate MOSFETs," Solid. State. Electron., vol. 51, no. 5, pp. 802–805, 2007.

[6] J. He, X. Zhang, G. Zhang, M. Chan, and Y. Wang, "A carrier-based analytic DCIV model for long channel undoped cylindrical surrounding-gate MOSFETs," Solid. State. Electron., vol. 50, no. 3, pp. 416–421, 2006.

- [7] J. He, J. Zhang, L. Zhang, C. Ma, and M. Chan, "A surface potential-based non-charge-sheet core model for undoped surrounding-gate MOSFETs," J. Semicond., vol. 30, no. 2, 2009.
- [8] J. B. Roldan, F.Gamiz, F. Jiménez-Molinos, C. Sampedro, A. Godoy, F. J.García-Ruiz and N. Rodriguez, "An analytical I-V model for surrounding-gate transistors that includes quantum and velocity overshoot effects," IEEE Trans. Electron Devices, vol. 57, no. 11, pp. 2925–2933, 2010.
- [9] T. K. Chiang, "A compact, analytical two-dimensional threshold voltage model for cylindrical, fully-depleted, surrounding-gate(SG) MOSFETs," in 2005 IEEE Conference on Electron Devices and Solid-State Circuits, EDSSC, 2006, pp. 547–550.
- [10] S. F. Transistors, Y. S. Yu, N. Cho, S. W. Hwang, and D. Ahn, "Implicit Continuous Current Voltage Model for Implicit Continuous Current – Voltage Model for Surrounding-Gate Metal – Oxide – Semiconductor Field-Effect Transistors Including Interface Traps," vol. 58, no. August 2016, pp. 2520–2524, 2011.
- [11] B. Iniguez, D. Jimenez, J. Roig, H. A. Hamid, L. F. Marsal, and J. Pallares, "Explicit continuous model for long-channel undoped surrounding gate MOSFETs," IEEE Trans. Electron Devices, vol. 52, no. 8, pp. 1868–1873, 2005.
- [12] Y. S. Yu, N. Cho, J. H. Oh, S. W. Hwang, and D. Ahn, "Explicit Continuous Current-Voltage (I-V) Models for Fully-Depleted Surrounding-Gate MOSFETs (SGMOSFETs) with a Finite Doping Body," Journal of nanoscience and nanotechnology, vol. 10, no. 5, pp. 3316–3320, 2010.
- [13] B. Yu, H. Lu, M. Liu, and Y. Taur, "Explicit continuous models for double-gate and surrounding-gate MOSFETs," IEEE Trans. Electron Devices, vol. 54, no. 10, pp. 2715–2722, 2007.
- [14] F. Liu, J. Zhang, F. He, F. Liu, L. Zhang, and M. Chan, "A charge-based compact model for predicting the current-voltage and capacitance-voltage characteristics of heavily doped cylindrical surrounding-gate MOSFETs," Solid. State. Electron., vol. 53, no. 1, pp. 49–53, 2009.
- [15] A.Tsormpatzoglou, D.H.Tassis, C.A.Dimitriadis, G.Ghibaudo, G.Pananakakis, R.Clerc, and A. Tsormpatzoglou, "A compact drain current model of short-channel cylindrical gate-all-around MOSFETs," Semiconductor Science and Technology, vol. 24, no. 7, pp.75017, 2009.
- [16] B. Smaani, S. Latreche, and B. Iniguez, "Compact drain-current model for undoped cylindrical surrounding-gate metal-oxide-semiconductor field effect transistors including short channel effects," Journal of Applied Physics, vol. 114, no. 22, 2013.
- [17] S. Mohammadi and A. Afzali-Kusha, "Drain current model for strained-Si/Si 1- x Ge x /strained-Si double-gate MOSFETs including quantum effects," Semiconductor Science and Technology, vol.26, no.9, pp. 95022, 2011.
- [18] H. M. Nayfeh, C. W. Leitz, A. J. Pitera, E. A. Fitzgerald, J. L. Hoyt, and D. A. Antoniadis, "Influence of high channel doping on the inversion layer electron mobility in strained silicon n-MOSFETs," IEEE Electron Device Lett., vol. 24, no. 4, pp. 248–250, 2003.
- [19] P.J. Chao, and Y. Li, Impact of geometry aspect ratio on 10-nm gate all-around silicon-germanium nanowire field effect transistors. In: Proceedings of the 14th IEEE International Conference on Nanotechnology, pp. 452–455, 2014.
- [20] T. V. Singh and M. J. Kumar, "Effect of the Ge mole fraction on the formation of a conduction path in cylindrical strained-silicon-on-SiGe MOSFETs." Superlattices and Microstructures, vol.44, no.1, pp79–85,2008.
- [21] Y.Jiang, N.Singh, , T.Y.Liow, W.Y. Loh, S.Balakumar, K.M.Hoe, C.H.Tung, V.Bliznetsov, S.C. Rustagi, G.Q. Lo, and D.S.H. Chan, "Ge-rich (70%) SiGe nanowire MOSFET fabricated using pattern-dependent Ge-condensation technique," IEEE Electron Device Letters 29.6, 595-598, 2008.
- [22] Y. Zhang, Z. Li, C. Wang, and F. Liang, "Compact Analytical Threshold Voltage Model of Strained Gate-All-Around MOSFET Fabricated on Si 1-x Ge x Virtual Substrate." IEICE Transactions on Electronics, vol.99, no.2, pp.302-307,2016.
- [23] Y. Liu, and Z. Li, "An analytical threshold voltage model of strained surrounding-gate MOSFETs," Solid-State and Integrated Circuit Technology (ICSICT), 2012 IEEE 11th International Conference on. IEEE, 2012.

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