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Optimization of high-k composite dielectric materials of variable oxide thickness tunnel barrier for nonvolatile memory

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ABSTRACT

Downscaling the tunnel oxide thickness has become one of the innovative solutions to minimize the operational voltage with better the programming/erasing (P/E) operation time. However, the downscaling technique faces several challenges where the conventional SiO2 tunnel layer has reached its limit. But a practical alternative has been introduced; Variable Oxide Thickness (VARIOT) technology in flash memory has been promising. VARIOT is one of tunnel barrier engineering technology for incorporating the high-k dielectric materials as a composite tunnel barrier. This paper presents the VARIOT concept to determine the optimum set of combination, the equivalent oxide thickness (EOT) and the low-k oxide thickness (Tox) for alternate high-k materials. Fowler-Nordheim (F-N) tunneling coefficients are also extracted for various combinations of VARIOT, where in this work ZrO2, HfO2, Al2O3, La2O3, and Y2O3 are used. The VARIOT optimization is conducted using 3-Dimensional (3D) Silicon Nanowire Field-Effect-Transistor (SiNWFET) device structure and simulated in TCAD Simulation tools. From the simulation results, it has found out that the high-k materials of La2O3 asymmetric stack is the excellent dielectric material among four (4) other dielectric materials; ZrO2, HfO2, Al2O3 and Y2O3 for EOT=4nm and Tox=1nm.

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1. INTRODUCTION

As the demand of flash memory device has increased, it is necessary to continuously downscale of the flash memory device. Memory capacity and performance must scale as the flash memory size has been scaled to maintain the device performance such as P/E voltage, P/E time, better retention and endurance. Nevertheless, the scaling becomes challenging because of the high electric fields acquired in the programming/erasing process [1] and direct tunneling effect [2].

Reduction of the thickness of the tunnel oxide may solve this challenge, but it also presents a severe bottleneck due to stress-induced leakage current (SILC). Many reports document the tunnel oxide should not reduce beyond 7-8nm because of the tradeoff between P/E process and retention reliability [3-4]. This condition will restrict the betterment of the device performance in terms P/E voltage and time. When the tunnel oxide is thinner, the P/E process will become faster, but the charge leakage will destroy the retention time. Therefore, it is necessary to find ingenious solutions to omit this restriction.

As one of the effective solutions, the inception of the different dielectric with high dielectric constant (high-k) materials stacks to engineer the tunnel oxide is proposed. Many researches have been reported about the tunnel barrier engineering (TBE) approach to analyze the performance before and after the inception of high-k dielectric materials [1-4]. TBE technology is an approach to modify the tunnel barrier by incorporating

the high-k dielectric materials in which the high-k dielectric will extend scalability of the same equivalent oxide thickness (EOT) by applying a thicker physical tunnel stack. TBE technology is divided into two approaches; 1) Crested Barrier Engineering and 2) Variable Oxide Thickness (VARIOT).

The VARIOT concept is proposed by Govoreanu et al. (2003) consisted of the two-layer dielectric stack where the low-k layer and high-k layer is combined hence it is called asymmetric stack [5]. Beforehand, the concept of Crested Barrier Engineering first is introduced by Likharev et al. in 1999 [6]. Few reports stated that TBE stack has a higher field-sensitivity compared to the single SiO_2 layer which allows shorter P/E time, smaller operating voltage plus the ten (10) years retention time is not affected [2, 7]. Also, it was stated that different dielectric materials would exhibit different performance of the device performance as their properties are different each other [7-8]. Driussi et al. (2005) have conducted theoretical analysis on the performance of Crested Barrier and VARIOT concept as resulting that the VARIOT combinations yield better performance than Crested Barrier combinations in terms of low operating voltage and better retention. Thus, VARIOT dielectric stack will be focused in this paper.

In this paper, the optimization work comparing high-k dielectric materials engineered in the tunnel barrier performance implementing VARIOT concept is conducted by using the asymmetric stack (low-k/high-k). Several high-k materials with fixed low-k SiO_2 thickness are explored using Direct Quantum Tunneling (DQT) model which represents the tunnel barrier under test.

2. RESEARCH METHOD

The VARIOT optimization involved two parts which are the parameter optimization and F-N coefficients extraction. The primary purpose of VARIOT optimization work has been divided into two objectives: 1) To simulate and determine the optimum set of dielectric material combination, the equivalent oxide thickness (EOT), the optimum thickness of low-k (T_{ox}) dielectric layer for minimum programming voltage (V_{prog}) and 2) To extract F-N tunneling coefficients of the optimum asymmetric stack. The equivalent oxide thickness (EOT) and optimum thickness of low-k (T_{ox}) are determined for each combination of the asymmetric stack (low-k/high-k) in which satisfying program, retention and read-disturb constraints of flash memory using the method proposed by Verma et al. (2010) [7]. Thus, the optimum combination of the asymmetric stack is selected based on minimum programming voltage (V_{prog}). Generally, Figure 1 shows the flowchart of the VARIOT optimization process.

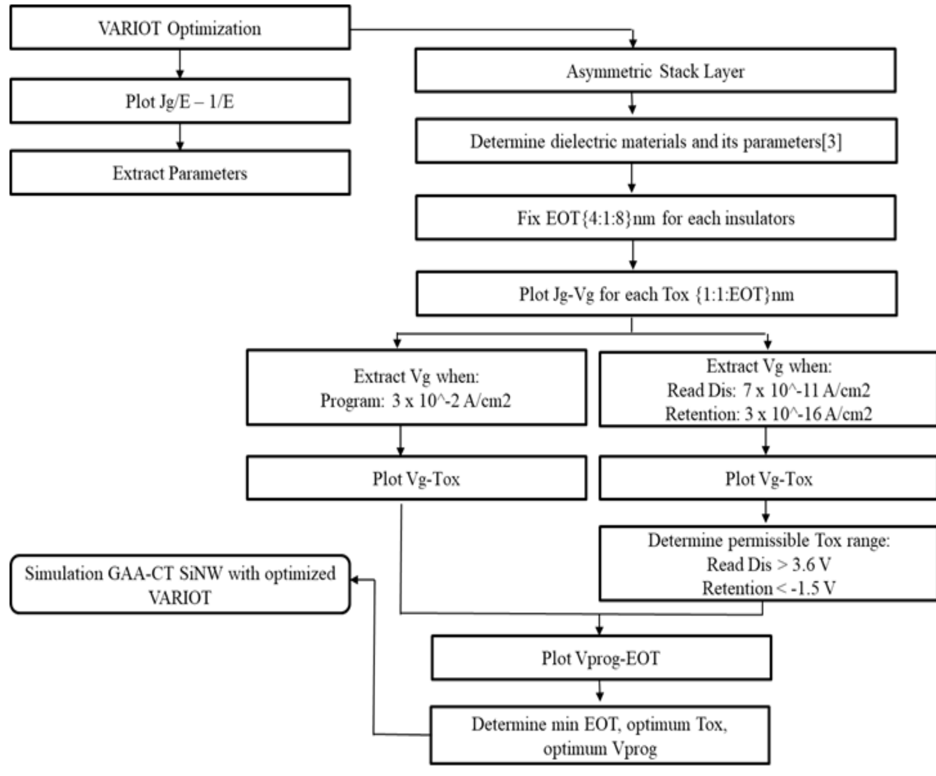


Figure 1. Flowchart of VARIOT optimization process

In order to optimize these parameters, there are two things need to be clarified. Firstly, the high-k materials of the asymmetric stacks need to be chosen based on their criteria [7-8]. One of the critical criteria is the materials can be deposited on the SiO_2 layer. Therefore, there are five (5) different high-k materials are selected in this optimization work (i.e., HfO_2, ZrO_2, Al_2O_3, La_2O_3 and Y_2O_3). High-k material plays a vital role in engineering the tunnel barrier. The relevant parameters of high-k material are the dielectric constant, tunneling mass of the electron and the conduction/valence band offset as stated in Table 1. Figure 2 shows the cross-sectional diagram of incorporation of VARIOT in SiNWFET device structure.

Table 1. Parameters for Different Dielectric Materials Used in the Simulation

Dielectric Parameters	HfO_2	ZrO_2	Al_2O_3	La_2O_3	Y_2O_3
Barrier Height, Φ_B (eV)	1.5	1.4	2.8	2.3	1.6
Dielectric Constant, ϵ_r	19	25	9.6	27	25
Electron Affinity, χ (eV)	2.7	2.8	1.3	1.9	2.4
Band Gap, E_G (eV)	6.0	5.8	8.8	6.0	6.0
Effective Mass, m^*/m_0	0.2	0.2	0.3	0.25	0.25

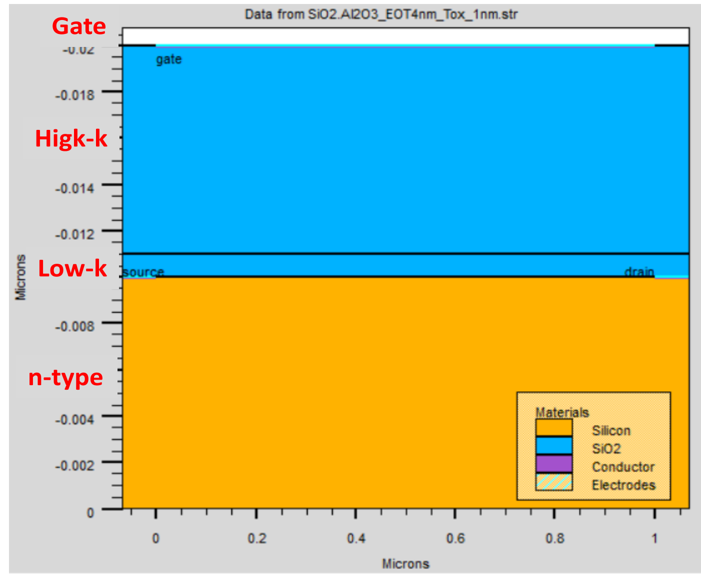


Figure 2. Cross-sectional of 3-D SiNWFET device structure with low-k/high-k stack as its gate oxide

After these materials' selection, the optimization work is conducted using TCAD Silvaco tool. The tunneling model used in this optimization process is DQT model considering high non-linearity of the composite barrier structure. The EOT physical dimension of each asymmetric combination is fixed for 4:1:8 nm, while the T_{ox} is varied from 1:1:EOT nm. The low-k dielectric thickness, T_{ox} is calculated as

$$EOT = Tox + (\frac{3.9}{\epsilon_{hk}})T_{hk} \quad (1)$$

where ϵ_{hk} and T_{hk} are the thickness and dielectric constant of the high-k material respectively. The high-k thickness is calculated based on the dielectric constant as in Table 1 by using (1). High-k dielectrics with a thicker physical barrier for an equal EOT act as an ideal alternative material. Secondly, constraints of flash memory must be considered in the optimization process because it will be the limit of allowable high-k material and its thickness as presented in Table 2, resulting in a domain down-selection.

Table 2. Flash Memory Operational Constraints [7]

Tolerable read-disturb current density (A/cm^2)	< ~ 4 x 10^{-11} at around 3.6V.
Tolerable retention current density(A/cm^2)	< 10^{-16} at around -1.5V.
Tolerable programming current density(A/cm^2)	3 x 10^{-2}
Endurance	> 10^4 P/E cycles

3. RESULTS AND ANALYSIS

Figure 3 illustrates the JV relationship of VARIOT stack of SiO_2/La_2O_3 for EOT=4nm. By varying the SiO_2 layer thickness of the VARIOT stack, the changes of JV curve can be observed. It shows that the J-V curve for VARIOT stack is steeper than the J-V curve of single tunnel SiO_2 layer. To be noted that by varying the thickness of low-k or high-k layer can change the leakage current characteristic as it is one of the limitations when downscaling the tunnel oxide layer. The potential drop across the SiO_2 layer changes due to varied low-k thickness, resulting in, changes of the potential drop across the high-k layer. Thus, for the same P/E current densities, the P/E voltage can be improved by varying the thickness of the SiO_2 layer.

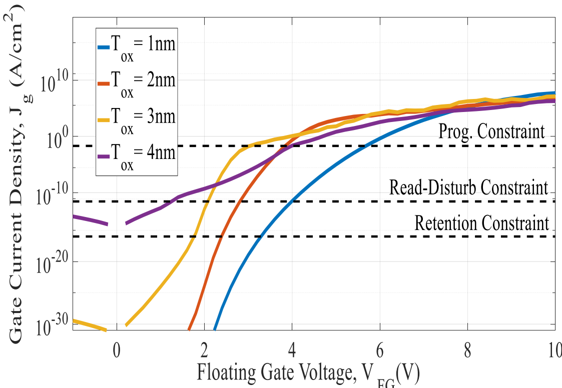


Figure 3. J-V Curve of Sio_2/La_2O_3 Dielectric Combinations for EOT = 4nm. the Dotted Line Indicates the Single Sio_2 Layer and the Solid Line Indicates the Sio_2/La_2O_3 Stack for T_{ox} 1:1:3nm

The J-V curve was plotted for T_{ox} in 1:1:EOT nm and the process was repeated to the different dielectric material of asymmetric stack. After that, the constraints (program, read disturb and retention) were imposed to the J-V curve, and the gate voltage that satisfies each constraint were extracted for every EOT-of all VARIOT stacks, and next step is plotting the $V_g - T_{ox}$ curve. Figure 4 represents the $V_g - T_{ox}$ curve for all VARIOT stacks which indicating the program constraint.

The lowest program voltage pattern can be identified from Figure 2. It is found that the minimum program voltage for 4 dielectric stack materials is at T_{ox}=2nm except for combination of SiO_2/La_2O_3 stack. The minimum gate voltage of SiO_2/La_2O_3 stack is at T_{ox}=3nm. As presented in Figure 4, all combination stacks have reached their peak program voltage at T_{ox}=3m and become saturated after that except for SiO_2/La_2O_3 stack. SiO_2/La_2O_3 stack behaves differently where its program voltage peak happened to be at T_{ox}=1nm and then saturated at the further changes.

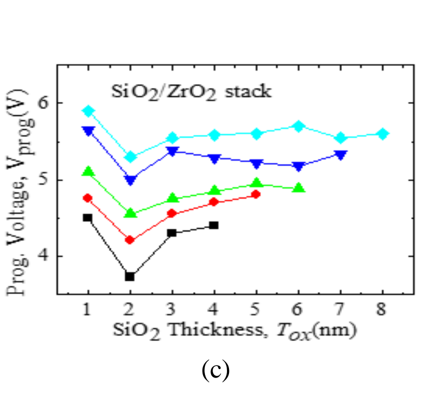
From Figure 4, it is expected that the direct tunneling occurred at $T_{ox} \leq$ 2nm as low voltage is needed. Then as T_{ox} is increased, it required higher gate voltage to perform F-N tunneling and become saturated because EOT is fixed and does not change the gate electrostatic control.

Even though the minimum program voltage is expected to be mostly at T_{ox}=2nm or 3nm but it does not elucidate that it is the optimized T_{ox}. For next step, both retention and read disturb constraints are imposed on the J-V curves to prevent memory contamination. Then the gate voltage that fulfills these constraints are extracted, and the $V_g - T_{ox}$ curve is plotted.

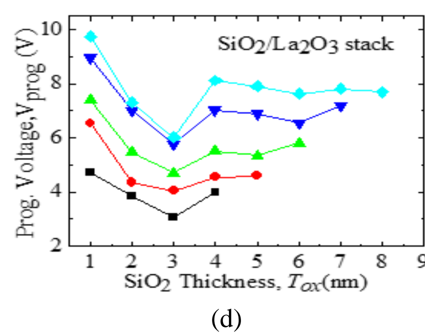
Figure 5 indicates the $V_g - T_{ox}$ curve for all VARIOT stacks under this study in which satisfying the read disturb and retention constraints. As can be seen in Figure 5, the trend of read disturb constraint is quite similar to the program constraint. However, dissimilar trend is observed for retention constraint, where lower gate voltage acquired to perform direct tunneling-at the retention constraint. However, higher gate voltage needed as the T_{ox} is scaled up.

As can be seen in Figure 5, the maximum allowable retention (V_{ret}) and read disturb (V_{read}) voltages on Floating Gate (FG) are also considered: V_{read}=3.6V (modern industry standard) and V_{ret}=-1.5V. To meet the retention and read disturb criteria, only above $V_{readdis}$ dashed line and below V_{ret} dashed line parts are considered.

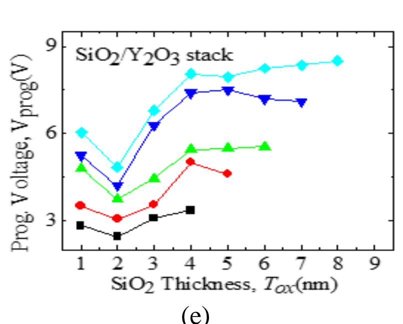
(a) (b)



(c)



(d)



(e)

Figure 4. V_g-T_{ox} plot for program constraint for (a) SiO_2/HfO_2 (b) SiO_2/Al_2O_3 (c) SiO_2/ZrO_2 (d) SiO_2/La2O3 (e) SiO_2/Y_2O_3

Then, all domains selected are plotted as Figure 6 to choose the minimum programming. Figure 6 illustrates the gate voltage for each EOT of all combinations of VARIOT stack for both constraints. Obviously the optimized T_{ox} for retention and read disturb is not exactly at T_{ox}=2nm or T_{ox}=3nm as previous case in Figure 4 because it does not satisfy both fixed constraints. Figure 6(a) shows that all the VARIOT tunnel layer are satisfied the retention constraint for EOT=4:1:8nm. As can be observed, the lowest programming voltage is ~2-3V can be obtained from composite stack with ZrO_2, HfO_2 and Y_2O_3 at EOT=4nm. However, the VARIOT tunnel stack with La_2O_3 cannot obtain the low V_{prog} due to the larger of barrier height (2.3 eV).

On the other hand, read disturb constraint has been a restrictive to the selection of domain Tox. The similar trend can be observed from Figure 6(b). Only the combination of SiO_2/La_2O_3 layer can fulfill the read disturb criteria at EOT = 4nm with the minimum programming voltage, V_{prog} (~4.70V). This is due to the higher band offset owing by La_2O_3's dielectric material. The composite with ZrO_2 and HfO_2 stack only satisfies the stringent read disturb condition at EOT=7nm whereas the SiO_2/Y_2O_3 stack only fulfill the criteria at EOT=8nm. The optimum EOT and T_{ox} are determined by comparing their programming voltage as in Figure 2. As expected, La_2O_3 can yields the lowest programming voltage as it satisfies the requirement of both retention and read disturb constraints. All the parameters extracted for each selection of all VARIOT asymmetric stack are summarized in Table 3.

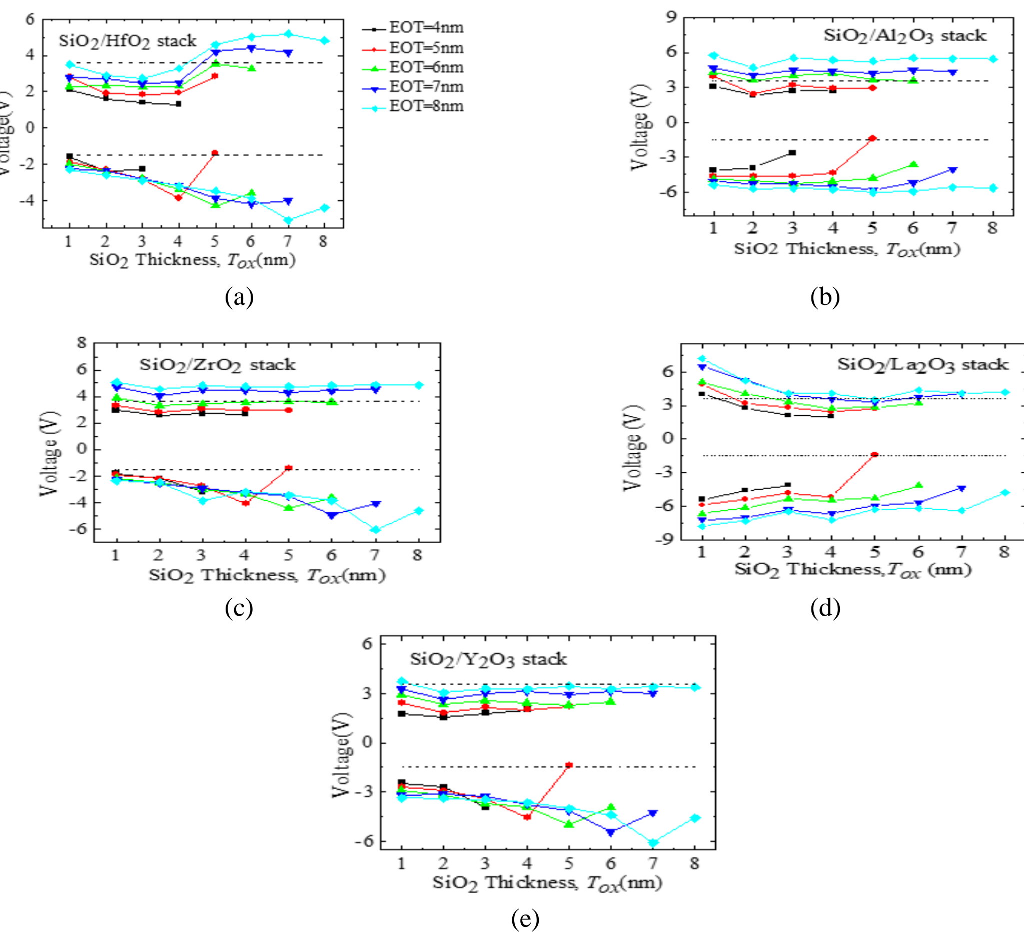


Figure 5. V_g-T_{ox} plot for retention and read disturb constraints for (a) SiO_2/HfO_2 (b) SiO_2/Al_2O_3 (c) SiO_2/ZrO_2 (d) SiO_2/La2O3 (e) SiO_2/Y_2O_3.. Dotted line refers to maximum allowed retention and read disturb voltages

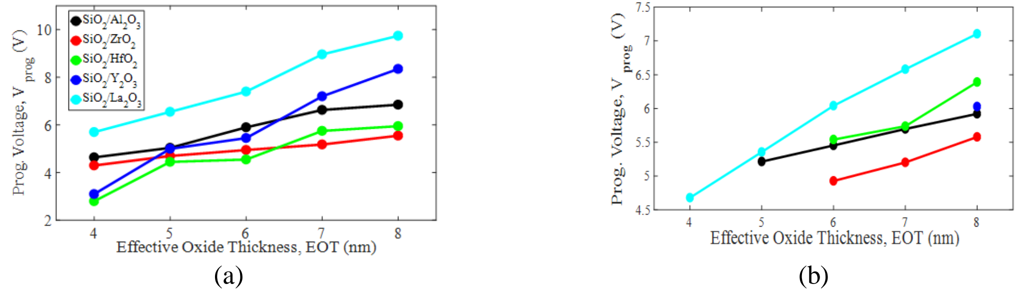


Figure 6. Gate Voltage for each EOT of all VARIOT stack (a) Retention constraint < |-1.5V| (b) Read Disturb Constraint > 3.6V

Table 3. Optimum Parameters Each of the VARIOT Asymmetric Stack

Parameters	HfO_2	ZrO_2	Al_2O_3	La_2O_3	Y_2O_3
EOT (nm)	6nm	6nm	5nm	4nm	8nm
T_{ox} (nm)	5nm	5nm	1nm	1nm	1nm
V_{prog} (V)	5.55	4.95	5.22	4.70	6.05
$V_{readdis}$ (V)	3.55	3.61	3.94	4.00	3.75
V_{ret} (V)	-4.3	-4.45	-4.63	-5.40	-3.35
F-N Coefficients Extraction					
$A_{FN_program}$, (A/V^2)			2.50×10^{-7}		
$B_{FN_program}$, (A/cm)			3.40×10^{8}		
A_{FN_erase}, (A/V^2)			6.77×10^{-7}		
B_{FN_erase}, (A/cm)			5.60×10^{8}		

4. CONCLUSION

The VARIOT optimization of composite tunnel barrier with respect to the SiO_2 layer (low-k) and EOT are performed to obtain the minimum V_{prog} which satisfying the flash constraints (program, retention and read-disturb constraints). The optimization is simulated using TCAD Silvaco ATLAS Simulator. The simulation is conducted using Silicon Nanowire FET structure. On top of that, five high-k dielectric materials under the asymmetric stack of tunnel barrier engineering are chosen to determine the optimum set of material, the lowest EOT, and optimum T_{ox}. Considering the flash constraint is one of important condition as read-disturb constraint has been found to be the most restrictive factor which limiting the advantage offered by the composite tunnel barrier. La_2O_3 appears to be the promising dielectric material, in yielding the minimum programming voltage, V_{prog} (4.7V) compared to the other dielectric materials (Al_2O_3, ZrO_2, HfO_2, and Y_2O_3). La_2O_3 also meet all the flash constraints requirement considered in the VARIOT optimization. Minimum EOT and optimum T_{ox} also can be determined from this study which is EOT=4nm and T_{ox}=1nm for the optimum combination of the SiO_2/La_2O_3 asymmetric stack.

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REFERENCES

[1] H. W. You, J. W. Son, and W. J. Cho, “Engineering of tunnel barrier for highly integrated nonvolatile memory applications,” *Appl. Phys. A Mater. Sci. Process.*, vol. 102, no. 4, pp. 921–926, 2011.
[2] J. Jung and W.-J. Cho, “Tunnel Barrier Engineering for Non-Volatile Memory,” *J. Semi. Technol. Sci.*, vol. 8, no. 1, pp. 29–32, 2008.
[3] S. Verma, E. Pop, P. Kapur, K. Parat, and K. C. Saraswat, “Operational Voltage Reduction of Flash Memory Using High-K Composite Tunnel Barriers,” *Electron Device Lett. IEEE*, vol. 29, no. 3, pp. 252–254, 2008.
[4] S. Verma, E. Pop, P. Kapur, P. Majhi, K. Parat, and K. C. Saraswat, “Feasibility Study of Composite Dielectric Tunnel Barriers for Flash Memory,” *65th Annu. Device Res. Conf.*, vol. 24, pp. 85–86, 2007.
[5] C. Zhao, C. Z. Zhao, S. Taylor, and P. R. Chalker, “Review on non-volatile memory with high-k dielectrics: Flash for generation beyond 32 nm,” *Materials (Basel).*, vol. 7, no. 7, pp. 5117–5145, 2014.
[6] S. Jain, D. Gupta, V. Neema, and S. Vishwakarma, “BE-SONOS flash memory along with metal gate and high- k dielectrics in tunnel barrier and its impact on charge retention dynamics,” *J. Semicond.*, vol. 37, no. 3, p. 034002, Mar. 2016.
[7] S. Jain, V. Neema, D. Gupta, and S. K. Vishvakarma, “Investigation of Band-Gap Engineered Silicon-Oxide-Nitride-Oxide-Silicon Flash Memory with High-k Dielectrics in Tunnel Barrier and Its Impact on Charge Retention Dynamics,” *J. Nanoelectron. Optoelectron.*, vol. 11, no. 6, pp. 663–668, Dec. 2016.
[8] F. Driussi, S. Marcuzzi, P. Palestri, and L. Selmi, “Gate current in stacked dielectrics for advanced FLASH EEPROM cells,” *Proc. ESSDERC 2005 35th Eur. Solid-State Device Res. Conf.*, vol. 2005, pp. 317–320, 2005.
[9] C. Sun, L. Liu, Z. Zhang, and L. Pan, “Comparison of reliability of single and stacked high-k structures of charge trapping memories,” *IEEE Int. Integr. Reliab. Work. Final Rep.*, pp. 59–61, 2013.
[10] G. Chen *et al.*, “Metal Floating Gate Memory Device with SiO_2/HfO_2 Dual-Layer as Engineered Tunneling Barrier,” *IEEE Electron Device Lett.*, vol. 35, no. 7, pp. 744–746, Jul. 2014.
[11] B. Govoreanu, P. Blomme, M. Rosmeulen, J. Van Houdt, and K. De Meyer, “Variot: A novel multilayer tunnel barrier concept for low-voltage nonvolatile memory devices,” *IEEE Electron Device Lett.*, vol. 24, no. 2, pp. 99–101, 2003.
[12] K. K. Likharev, “Layered tunnel barriers for nonvolatile memory devices,” *Appl. Phys. Lett.*, vol. 73, no. 15, pp. 2137–2139, 1998.
[13] S. Verma, “Tunnel Barrier Engineering for Flash Memory Technology,” 2010.
[14] A. Hamzah, N. Ezaila Alias, and R. Ismail, “Low-voltage high-speed programming gate-all-around floating gate memory cell with tunnel barrier engineering,” *Jpn. J. Appl. Phys.*, vol. 57, no. 6, pp. 1–20, 2018.
[15] D. S. Software, “Atlas User’s Manual,” no. 408, pp. 567–1000, 2013.
[16] J. Robertson and R. M. Wallace, “High-K materials and metal gates for CMOS applications,” *Mater. Sci. Eng. R Reports*, vol. 88, pp. 1–41, 2015.
[17] R. D. Clark, “Emerging applications for high K materials in VLSI technology,” *Materials (Basel).*, vol. 7, no. 4, pp. 2913–2944, 2014.
[18] M. Salmani-Jelodar, H. Ilatikhameneh, S. Kim, K. Ng, P. Sarangapani, and G. Klimeck, “Optimum high-k oxide for the best performance of ultra-scaled double-gate mosfets,” *IEEE Trans. Nanotechnol.*, vol. 15, no. 6, pp. 904–910, 2016.

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