Indonesian Journal of Electrical Engineering and Computer Science
Vol. 14, No. 2, May 2019, pp. 895~902
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v14.i2.pp895-902

Low voltage CMOS power amplifier with integrated analog Pre-Distorter for BLE 4.0 application

Selvakumar Mariappan[1], Jagadheswaran Rajendran[2], Norlaili Mohd Noh[3], Harikrishnan Ramiah[4], Asrulnizam Abd Manaf[5], Shukri Korakkottil Kunhi Mohd[6], Yusman Mohd. Yusof[7]
[1,2,5,6]Collaborative Microelectronic Design Excellence Centre (CEDEC), Universiti Sains Malaysia, Malaysia
[3]School of Electrical & Electronic Engineering, Universiti Sains Malaysia, Malaysia
[4]Department of Electrical Engineering, Faculty of Engineering, Universiti Malaya, Malaysia
[7]Silterra Malaysia Sdn. Bhd, Kulim Hi-Tech Park, Malaysia

Article Info

Article history:

Received Sep 28, 2018
Revised Nov 26, 2018
Accepted Dec 10, 2018

Keywords:

Active inductor
Analogue pre-distorter
Bluetooth low energy
CMOS
Power amplifier

ABSTRACT

In this paper, a low power consumption linear power amplifier (PA) for Bluetooth Low Energy (BLE) application is presented. An analogue pre-distorter (APD) is integrated to the PA. The APD consist of an active inductor, driver amplifier, and a RC phase linearizer. The PA delivers more than 12dB power gain from 2.4GHz to 2.5GHz. At the center frequency of 2.45GHz, the gain of the PA is 13dB with PAE of 26.7% and maximum output power of 14dBm. The corresponding OIP3 is 27.6dBm. The supply voltage headroom of this PA is 1.8V. The propose APD serves to be a solution to improve the linearity of the PA with minimum trade-off to the power consumption.

Corresponding Author:

Jagadheswaran Rajendran,
Collaborative Microelectronic Design Excellence Centre (CEDEC),
Universiti Sains Malaysia,
Sains@USM Level 1, Block C No. 10, Lebuh Bukit Jambul, 11900 Bayan Lepas, Pulau Pinang, Malaysia.
Email: jaga.rajendran@usm.my

1. INTRODUCTION

In recent years, wireless communication system has evolved rapidly to accomplish higher data rate transmission scheme. Wireless communication is aiding in the development of Internet of Things (IoT) which includes communication devices such as Wi-Fi, Zigbee, and Bluetooth.

Bluetooth devices work in the Industrial, Scientific, and Medical (ISM) band which is located at 2.4 – 2.483 GHz. Bluetooth devices is classified into 3 classes based on their data transmission distance. Higher transmission distance requires higher output power from the transmitter. The classes are Class 1, Class2, and Class 3 with maximum output power of 20dBm, 4dBm, and 0dBm respectively [1]. Bluetooth power amplifier usually works in low power mode, which requires the Class 1 power amplifier to be controlled down to 4dBm or less in a monotonic sequence in order to save the power [2]. Figure 1 depicts the location of the PA in the block diagram of BLE transmitter.

CMOS power amplifier have been broadly examined to satisfy the demand of low cost and minimal size transceivers. Due to the high tradeoff between linearity and efficiency in CMOS PAs as compared to GaAs PAs, arduous challenges have been faced in order to achieve stringent linearity requirements for modern wireless communication system [3-6]. Various intrinsic drawbacks in CMOS PA such as low quality factor, lossy substrate of passive structures, low breakdown voltage, and low trans-conductance of active devices contributes to the difficulty of CMOS PA commercialization. Therefore, numerous exertions

in terms of linearity enhancement techniques and efficiency enhancement techniques have been implemented on overcoming the drawbacks of CMOS technology for PA designs [7-9].

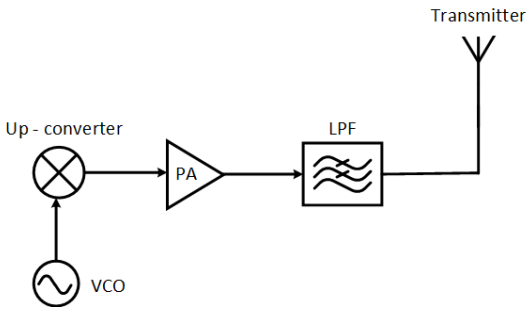

Figure 1. The block diagram of BLE transmitter

A simple linearization technique using passive components have been proposed by P. Gunasegaran et al (2017) for BLE application [10]. A simple RC network is connected at the gate of the transistors which reduces Cgs effect and thus improves linearity. Moreover, linearization using a simple body network have been proposed by G. Jeong et al (2016) for WLAN application [11]. A linearizing body network is implemented by utilizing a resistor that connect the body and drain node of a power transistor. Also, a common-gate combining PA with load impedance adaptor have been proposed by Y. Jin et al (2017) [12]. The PA is utilized for WLAN application in which the main amplifiers are biased differently to apply the adaptive power cell technique which enhances linearity.

The purpose of this work is to design a linear low power CMOS PA for BLE application. High linearity is targeted to enhance the communication distance while preserving the quality of the data transmitted. An analogue pre-distorter is implemented in the CMOS PA to achieve this target. The outline of this work is arranged as follows. In Section 2, the design methodology of the CMOS PA is described. Section 3 represents the post layout results obtained for the designed CMOS PA. Finally, the conclusion is presented in Section 4.

2. DESIGN METHODOLOGY

The schematic diagram of the proposed CMOS power amplifier (PA) with APD is illustrated in Figure 2. Zout APD denotes the output impedance of the APD while Zout Main denotes the output impedance of the main amplifier. The main amplifier is biased at Class AB with quiescent current of 17 mA. The input matching network is represented by C1, C2, C3, and L1. On the other hand, the output matching network is represented by C11, C12, C13, and L3. Capacitor C10 functions as a decoupling capacitor to shunt the third order non-linear component produced from the drain supply to ground. Inductor L2 and capacitor C9 nullifies the effect of parasitic drain-source capacitance, Cds, thus improving the PAE of the PA.

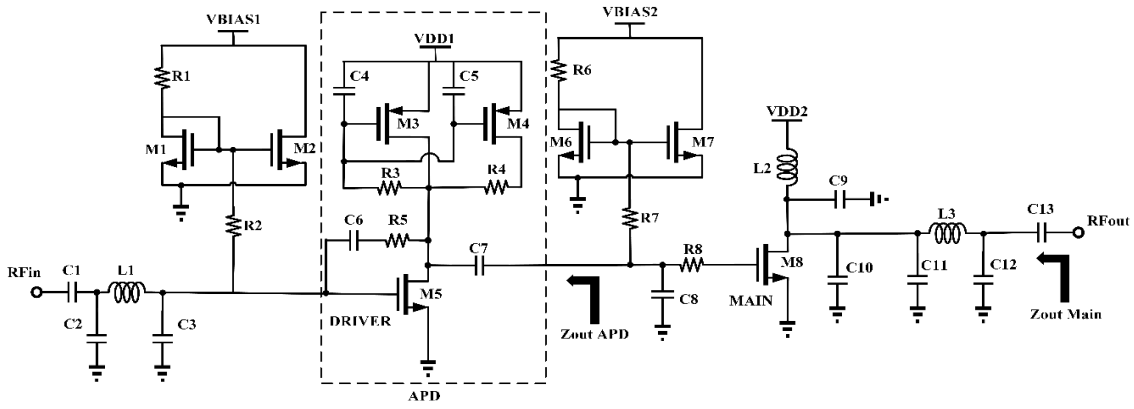

Figure 2. The schematic of the PA with APD

Figure 3 depicts the AM – PM responses of the APD and main amplifier. The phase response between the APD and main amplifier are opposite to each other and is represented in 1 and 2 respectively.

$$Z_{out\_APD} = \frac{[(R_5R_3R_{o1}R_{o2}R_{o3}R_8 + R_5R_3R_4R_{o1}R_{o3}R_8) - j\omega(C_8R_5R_3R_{o1}R_{o2}R_{o3} + C_8R_5R_3R_4R_{o1}R_{o3} + C_8R_3R_8R_{o1}R_{o2} + C_7R_3R_8R_{o1}R_{o2} + C_7R_3R_4R_8R_{o1} + C_7R_5R_8R_{o1}R_{o2} + C_7R_5R_8R_4R_{o1} + C_7R_3R_5R_8R_{o2} + C_7R_3R_4R_5R_8 + C_7R_3R_5R_8R_{o1} + C_7R_8R_{o3} + C_6R_3R_8R_{o1}R_{o2}R_{o3} + C_6R_3R_4R_8R_{o1}R_{o3})]}{[(R_5R_3R_{o1}R_{o2}R_{o3} + R_5R_3R_4R_{o1}R_{o3}) - j\omega(C_6R_{o1}R_{o2}R_{o3}R_3 + C_6R_3R_4R_{o1}R_{o3} + C_7R_{o1}R_{o2}R_3 + C_7R_{o1}R_4R_3 + C_7C_3R_5R_{o1}R_{o2} + C_7C_3R_{o3}R_4 + C_7R_5R_3R_{o2} + C_7R_3R_4R_5 + C_7R_3R_5R_{o1} + C_7R_{o3} + C_8R_{o1}R_{o2}R_3 + C_8R_{o1}R_4R_3 + C_8R_{o1}R_{o2}R_5 + C_8R_{o1}R_4R_5 + C_8R_{o2}R_3R_5 + C_8R_3R_4R_5 + C_8R_3R_5R_{o1} + C_8R_{o3})]} \quad (1)$$

where R_{o1}, R_{o2}, and R_{o3} are the resistor representation of the channel length modulation of transistors M3, M4, and M5 respectively.

$$Z_{out\_MAIN} = \frac{j\omega(C_{10}C_{11}C_{12}R_{o4} + C_{10}C_{11}C_{13}R_{o4} + C_{10}C_{12}C_{13}R_{o4} - C_{10}C_{12}L_3R_{o4} - C_{10}C_{13}L_3R_{o4} + C_{11}C_{12}C_{13}R_{o4} - C_{11}C_{12}L_3R_{o4} - C_{11}C_{13}L_3R_{o4})}{[(C_{11}L_3R_{o4} - C_{11}C_{12}R_{o4} + C_{10}L_3R_{o4} - C_{10}C_{12}R_{o4} - C_{11}C_1R_{o4}) + j\omega(C_{10}C_{11}C_{12} - C_{10}C_{11}L_3)]} \quad (2)$$

where R_{o4} is the resistor representation of channel length modulation of transistor M8.

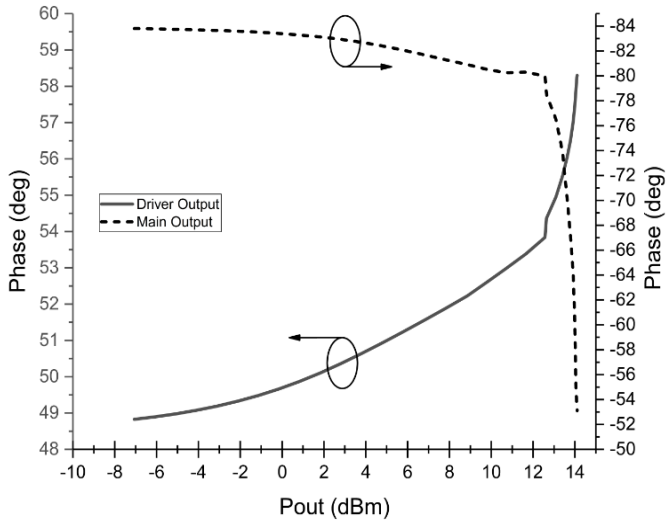

Figure 3. The AM-PM responses of the APD and main amplifier

3. VALIDATION RESULTS

The small signal parameters of the PA is as shown in Figure 4. At the center frequency of 2.45GHz, the PA produces a gain of 13dB. The S11 and S22 value of the PA are -19.5dB and -19.7dB respectively which provides a good reverse isolation of both input and output.

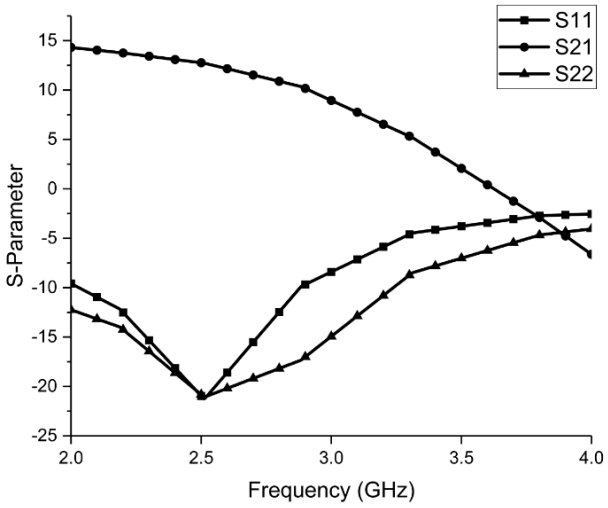

Figure 4. Small signal parameters of the designed PA

The stability factor of the PA is depicted in Figure 5. It can be observed from the figure that the PA is unconditionally stable across the frequency of 1GHz to 5GHz.

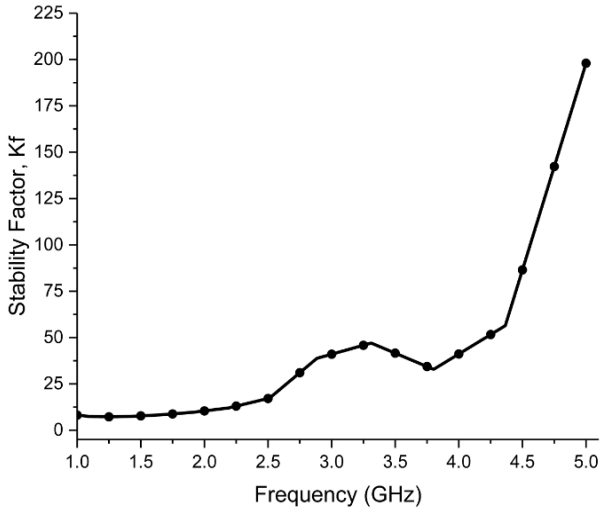

Figure 5. The stability factor of the PA is unconditionally stable

Figure 6 shows power gain, PAE, and OIP3 of the PA. The power gain of the PA across output power shows a flat gain is achieved up to 1dB compression point. The maximum delivered output power is 14.1dBm while the 1dB compressed output power (P_{1dB}) is 12.6dBm. The PA achieves a peak power added efficiency (PAE) of 26.7% at the center frequency of 2.45GHz. In addition, the linearity of the PA is presented in terms of output third order intermodulation product (OIP3). The PA produces maximum OIP3 of 27.6dBm when a dual tone signal with 1MHz spacing is injected to the input of the PA. At this point, the phase cancellation is maximum.

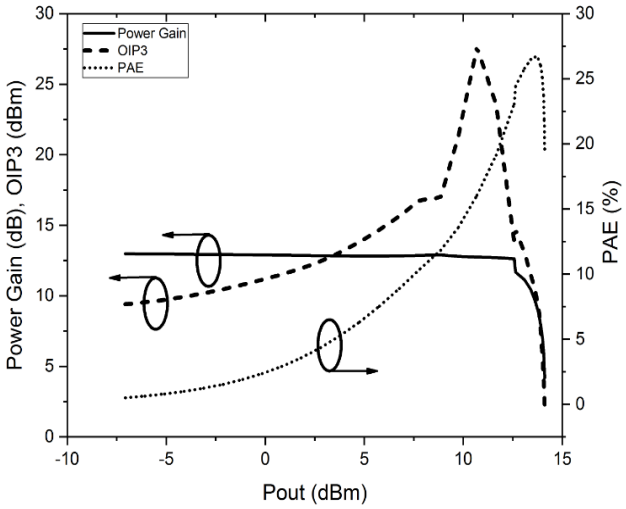

Figure 6. The power gain, PAE, and OIP3 achieved by the PA

The layout of the designed PA is depicted in Figure 7. The chip size of the PA is 1678um x 1748um including the pads for measurement. The post layout simulation performance of the PA is summarized in Table 1. On the other hand, the recent works on low power CMOS PA is summarized and compared in Table 2.

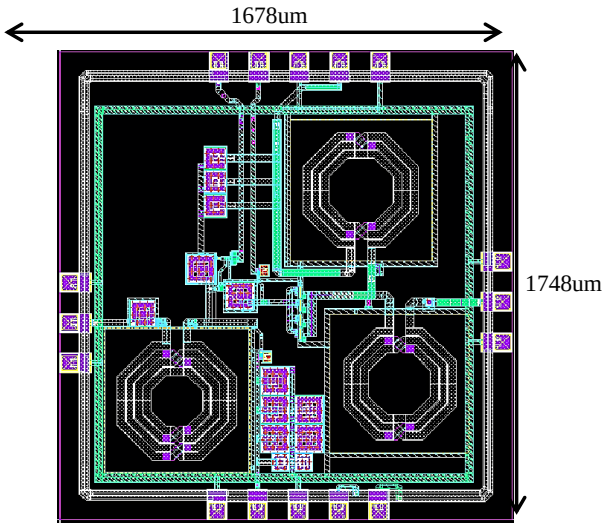

Figure 7. The layout of the designed PA

Table 1. Post Layout Simulation Performance of the PA

Operating Frequency	2.45GHz
Bandwidth	100MHz
Power Gain, S21	12.9dB
Input Return Loss, S11	-19.5dB
Output Return Loss, S22	-19.7dB
Peak PAE	26.7%
Max. Output Power	14.1dBm
OIP3	27.6dBm
Power Supply Voltage	1.8V
Technology	180nm CMOS

Table 2. Work Comparison with Published Power Amplifiers

Ref	PA Tech.	Supply (V)	Max Linear Pout (dBm)	Peak PAE (%)	Gain (dB)	Freq. (GHz)	Linearity	Application
[10]	180nm	1.8	13	38.4	10	2.45	20.6dBm (OIP3)	BLE
[11]	55nm	3.3	16	16	30	2.45	-34dBc (IMD3)	WLAN
[12]	180nm	3.3	22.08	31.97	30.7	2.4	-	WLAN
[13]	130nm	2.0	19	32	31	2.5	-	-
[14]	180nm	3.3	16.5	36.6	22	0.6	-	IoT
This work	180nm	1.8	12.6	27.6	13	2.45	27.6dBm	BLE

4. CONCLUSION

In this paper, an 180nm CMOS PA was designed with an integrated analogue pre-distorter (APD) in which an active inductor is a part of it. The APD improves the linear output power of the PA for low power BLE power amplifier. The PA achieved an OIP3 of 27.6dBm with maximum PAE of 26.7%, as well as maximum output power of 14.1dBm. Hence, the proposed PA design serves as a good solution to be integrated with a low power BLE transceiver.

ACKNOWLEDGEMENTS

This research work is funded by Collaborative Research in Engineering, Science and Technology (CREST) [304/PELECT/6050378/C121] and Universiti Sains Malaysia [304/PCEDEC/6315056].

REFERENCES

[1] Specification of the Bluetooth System, "BLUETOOTH SPECIFICATION Version 2.0 + EDR", vol 3, pp. 31, Nov. 2004.
[2] V. Vathulya, T. Sowlati, and D. M. W. Leenaerts, Class-1 Bluetooth power amplifier with 24-dBm output power and 48% PAE at 2.4 GHz in 0.25□m CMOS," Proc. of 27th European Solid-State CircuitsConf. ESSCIRC, 2001, pp. 84–87.
[3] B. Koo, Y. Na, and S. Hong, "Integrated bias circuits of RF CMOS cascode power amplifier for linearity enhancement," IEEE Trans. Microw. Theory Techn., vol. 60, no. 2, pp. 340–351, Feb 2012.
[4] S. Jin, B. Park, K. Moon, M. Kwon, and B. Kim, "Linearization of CMOS cascode power amplifiers through adaptive bias control," IEEE Trans. Microw. Theory Techn., vol. 61, no. 12, pp. 4534–4543, Dec 2013.
[5] E. Kaymaksut and P. Reynaert, "Dual-mode CMOS Doherty LTE power amplifier with symmetric hybrid transformer," IEEE J. Solid-State Circuits, vol. 50, no. 9, pp. 1974–1987, Sep 2015.
[6] K. Oishi et al., "A 1.95 GHz fully integrated envelope elimination and restoration CMOS power amplifier using timing alignment technique for WCDMA and LTE," IEEE J. Solid State Circuits, vol. 49, no. 12, pp. 2915–2924, Dec 2014.
[7] Gwanghyeon Jeong, Bonhoon Koo, Taehwan Joo, and Songcheol Hong, "Linearization of RF CMOS Power Amplifier," IEEE Inter. Symposium on Radio Frequency Integration Technology, 2015, Korea, pp 154-156.
[8] P. Asbeck and C. Fallesen, "A 29 dBm 1.9 GHz class B power amplifier in a digital CMOS process," Proc. ICECS, 2000, vol. 1, pp. 17–20.
[9] T. C. Kuo and B. Lusignan, "A 1.5 W class-F RF power amplifier in 0.2 m CMOS technology," ISSCC Dig. Tech. Papers, 2001, pp. 154–155.
[10] P. Gunasegaran, J. Rajendran and H. Ramiah, "A CMOS 180nm class-AB power amplifier with intergrated phase linearizer for BLE 4.0 achieving 11.5dB gain, 38.4% PAE and 20dBm OIP3," 2017 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia), Kuala Lumpur, Malaysia, 2017, pp. 61-64.
[11] G. Jeong, S. Kang, T. Joo and S. Hong, "An Integrated Dual-Mode CMOS Power Amplifier With Linearizing Body Network," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 9, pp. 1037-1041, Sept 2017.
[12] Y. Jin and S. Hong, "A 2.4-GHz CMOS Common-Gate Combining Power Amplifier With Load Impedance Adaptor," IEEE Microwave and Wireless Components Letters, vol. 27, no. 9, pp. 836-838, Sept 2017.
[13] H. Madureira, A. Gros, N. Deltimple, M. Dematos, S. Haddad, D. Belot and E. Kerherve, "Design and measurement of a 2.5 GHz switched-mode CMOS power amplifier with reliability enhancement," *2016 IEEE MTT-S International Wireless Symposium (IWS)*, Shanghai, 2016, pp. 1-4.
[14] J. Cui, K. Zhang and T. Tian, "A dual-level and dual-band class-D CMOS power amplifier for iot applications," *2013 IEEE 11th International New Circuits and Systems Conference (NEWCAS)*, Paris, 2013, pp. 1-4.

BIOGRAPHIES OF AUTHORS

Selvakumar Mariappan graduated in Bachelor of Electrical Engineering Technology (Industrial Power) degree from Universiti Teknikal Malaysia Melaka (UTeM) in 2017. He is currently pursuing the M.Eng degree in Microelectronics in Universiti Sains Malaysia, Pulau Pinang and also a Postgraduate Intern in Silterra (M) Sdn. Bhd. His current research interests include CMOS RF power amplifier design.

	Jagadheswaran Rajendran was born in Pulau Pinang, Malaysia. He received his B.Eng degree (Hons) from Universiti Sains Malaysia, Pulau Pinang, Malaysia, in 2004, the M.Eng degree in Telecommunications from Malaysia Multimedia University, Cyberjaya, Malaysia, in 2011, and the Ph.D. degree in Radio Frequency Integrated Circuit (RFIC) design from the University of Malaya, Kuala Lumpur, Malaysia, in 2015. He is currently a Senior Lecturer at Collaborative Microelectronic Design Excellence Centre (CEDEC) and School of Electronic Engineering, Universiti Sains Malaysia. Prior joining the university, he worked in Laird Technologies, Motorola Solutions, Broadcomm and Silterra as Research and Development Engineer. His research interest is RFIC design, analog IC design and RF system design for mobile wireless communications which has resulted several technical publications. He holds one US patent and one International patent. Dr Jagadheswaran was the recipient of the IEEE Circuit and System Outstanding Doctoral Dissertation Award in 2015. He is a Senior Member of IEEE and currently serves as the Chairman of IEEE ED/MTT/SSC Penang Chapter.
	Assoc.Prof.Ir.Dr. Norlaili Mohd Noh graduated with B.Eng. Electrical Engineering (Honours) from Universiti Teknologi Malaysia, and both MSc. in Electrical and Electronic Eng. and Ph.D in Integrated Circuit Design from Universiti Sains Malaysia. She is currently an Associate Professor with the School of Electrical and Electronic Engineering, Universiti Sains Malaysia. Her specialization is in Analog RFIC Design. She is also a professional engineer registered with the Board of Engineers Malaysia and a Chartered Engineer registered with UK Engineering Council.
	Harikrishnan Ramiah is currently an Associate Professor at Department of Electrical Engineering, University of Malaya, working in the area of RFIC design. He received his B.Eng(Hons), MSc and PhD degrees in Electrical and Electronic Engineering, in the field of Analog and Digital IC design from Universiti Sains Malaysia in 2000, 2003 and 2008 respectively. He was with Intel Technology, Sdn. Bhd attached in power gating solution of 45 nm process. In the year 2003, he was with SiresLabs Sdn. Bhd, CyberJaya, Malaysia working on 10Gbps SONET/SDH Transceiver solution. At the year 2002 he was attached to Intel Technology, Sdn. Bhd performing high frequency signal integrity analysis for high speed digital data transmission and developing Matlab spread sheet for Eye diagram generation, to evaluate signal response for FCBGA and FCMMAP packages. Harikrishnan was the recipient of Intel Fellowship Grant Award, 2000-2008. He is a Chartered Engineer of Institute of Electrical Technology (IET) and also a Professional Engineer registered under the Board of Engineers, Malaysia. He is a member of The Institute of Electronics, Information and Communication Engineers (IEICE) and an elevated Senior Member of the Institute of Electrical and Electronics Engineer (IEEE). His research work has resulted in several technical publications. His main research interest includes Analog Integrated Circuit Design, RFIC Design, VLSI system and RF Energy Harvesting Power Management Module Design.
	Asrulnizam Abd Manaf received the Bachelor Engineering in Electrical and Electronic Engineering from Toyohashi University of Technology, Japan in 2001. Then, he worked as Electrical Engineer at Toyo-Memory Technology Sdn. Bhd at Kulim High Tech Park, MALAYSIA before he further his master degree at Toyohashi University of Technology, Japan. He received Master Engineering in Electrical and Electronic Engineering in 2005. He pursued his Ph.D study in Keio University, Japan in 2006. He received Ph.D in Engineering from Department of Applied Physic and Physico Informatics, School of Fundamental Science and Technology, Keio University Japan in 2009. Since 2009, he joined the school of Electrical and Electronic Engineering, Universiti Sains Malaysia as a senior lecturer. Then, promoted to Associate Professor in 2015. He has graduated 7 Ph.D students and 16 MSc students. Currently, 6 Ph.D students and 2 MSc under supervision. He has authored and co-authored 60 international technical journal or conference papers. He won several innovation awards at national and International Invention competition. Currently he has 2 patent filings for DNA sensor and CMOS based tuneable inductor. His current research interest includes development of microfluidic-based DNA sensor integrated with CMOS circuitry, miniaturized of fluidic-based inclination sensor, bio inspired based microfluidic acoustic, pressure and flow sensor for underwater system, micro fluidic based memristor, micro fluidic based tuneable inductor, micro fluidic Thermoelectric Generator (mTEG)-based energy harvesting, Graphene-based transistor and micro 3-dimension fabrication technique by using grayscale Technology. From 1st January 2016, he appointed as academic staff at Collaborative Microelectronic Design Excellence Center (CEDEC), Universiti Sains Malaysia.

	Shukri Korakkottil Kunhi Mohd graduated BEng (mechatronic) and MSc (electronic) degrees from Universiti Sains Malaysia (USM) in 2006 and 2011, respectively. Currently, he is pursuing doctoral postgraduate study as part time student in device modeling and characterization at USM. Besides that, he is working as a research officer at Collaborative Micro-Electronic Design Excellence Center (CEDEC), USM.
	Yusman Mohd. Yusof received his BEng degree in electronic and computer engineering from Universiti Putra Malaysia (UPM) in 1999. He is currently working at Silterra (M) Sdn. Bhd. focusing on devices characterization and models development including the radio frequency (RF) and electrostatic discharge (ESD).