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Study of CMOS power amplifier design techniques for ka-band applications

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ABSTRACT

This paper reviews of high efficiency CMOS power amplifiers (PAs) in millimeter (mm) wave Ka - Band applications. The study is focused on the challenges in designing PA especially in GHz frequencies inclusive of high gain, good input and output matching, efficiency, linearity, low group delay and low power consumption. Several works on CMOS PA from year 2009 to 2018 are discussed in this paper. Recent developments of CMOS PAs are examined and a comparison of the performance criteria of various techniques is presented.

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1. INTRODUCTION

Research on fifth generation (5G) wireless services by 2020 is in progress, and mm-Wave Ka-Band technology will offer a vital role in meeting high demand for broadband data traffic [1-2]. Recently, it is reported that Samsung's 5G network also adopts the 28 GHz mm-wave Ka-Band frequency.This is the triggering point for the researcher to research on Ka-Band mm-wave Power Amplifier (PA).

Since the PA operates at very high frequency, it can have wide bandwidth. However, as the signal bandwidth increases, the linearity of the PA is degraded because the asymmetric sideband is generated by the memory effect [3-5]. Furthermore, the critical part in designing CMOS PA in Ka-Band spectrum is to achieve high gain, low power, inputand output matching and power added efficiency over wide band frequency from 26.5-40 GHz.

A number of CMOS PA designs for mm-wave Ka-Band spectrum have been proposed with different techniques: 2-stage cascade [6- 7], cascade pairs[8], 2 stage cascade with optimal bias selection [9], 2 stage cascade with adaptive bias [10], 2 stage cascade with reverse body bias [11], 2 stage cascade with power combiner [12], and 2 stage cascade with linearization on/off [13]. Adding power combiner to the design led to achieve high gain but such design trade off on size. 2 stages with stagger tuning concept was used to improve gain flatness and lead to achieve maximum PAE and output power [14]. Ideally most of the designer use cascade architecture to obtain wider gain bandwidth.

2. KA BAND DESIGN TECHNIQUE

A race to provide 5G technology by the next decade is in progress. 5G wireless services usually operate in Ka-Frequency band (18 - 28GHz). In 2009, [6] proposed two-stage 20–24 GHz PA with each stage using cascode configuration as shown in Figure 1. In this design, the size of each transistor in the driver stage was chosen to be 32 fingers and width of 2.5 um. The size of each transistor in the power stage was 64 fingers and a width of 2.5 um. The cascode structure makes the device more unilateral between input and output port, and at the same time, provides higher gain in comparison with single MOS transistor. This PA was biased at class-AB operation to compromise between power and linearity. The ratio of output to input total periphery was 4:1. The bypass capacitor of each drain dc path was set to be 4 pF.A 20–24 GHz PA using TSMC standard 0.18 CMOS process has shown a small signal gain above 15 dB in 20–24 GHz frequency band with 16.8 dBm output saturation power and PAE of 10.7%.

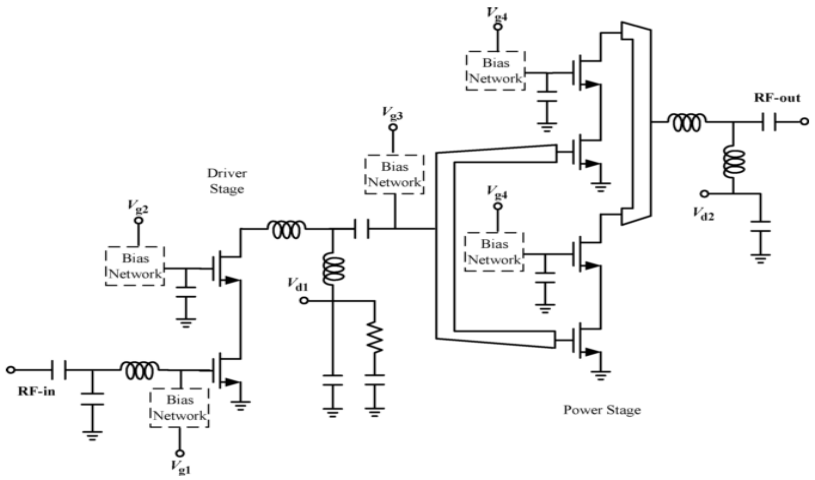

Figure 1. Schematic of 20 – 24 GHz PA[6]

In 2010, [8] proposed the cascode pairs that biased in class A as shown in Figure 2 in order to achieve higher gain and better linearity performance. Deep n-well and the gate terminals of transistor are all biased via 5-Kn. Metal 1 and metal 6 are used as thin-film microstrip line for interconnection and matching stubs. VDD and deep n- well are biased at 3.6-V for maximum output power. With a chip size of 0.6 mm x 0.7 mm, the amplifier had shown an OP1dB of 20-dBm and a Psat of 22-dBm. The peak PAE is 20 % under 3.6-V bias supply.

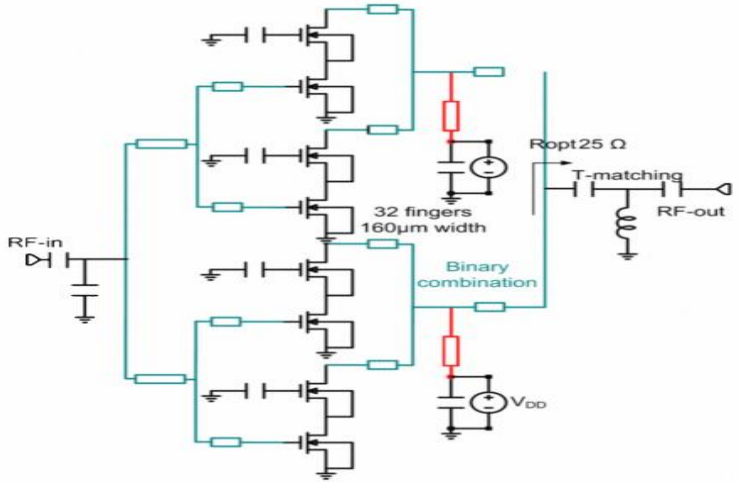

Figure 2. Schematic for cascode pairs[8]

In 2011, [7] proposed a fully-integrated K-band differential power amplifier was designed in 65 nm CMOS as shown in Figure 3. The power amplifier comprised of the 2-stage cascode configuration has the matching networks based on the transformer. To match the impedances, turn ratios of each transformer were designed to be 1:1 for the input stage, 2:1 for the inter stage, and 1:1.5 for the output stage, respectively. The saturation power of more than 20 dBm was obtained in the band between 16 GHz and 25 GHz. The peak value of the saturation power was 23.8 dBm, and the power added efficiency (PAE) was 25.1 % at 19 GHz. The chip occupied area including the DC and RF pads is 1.2 x 0.8 mm.

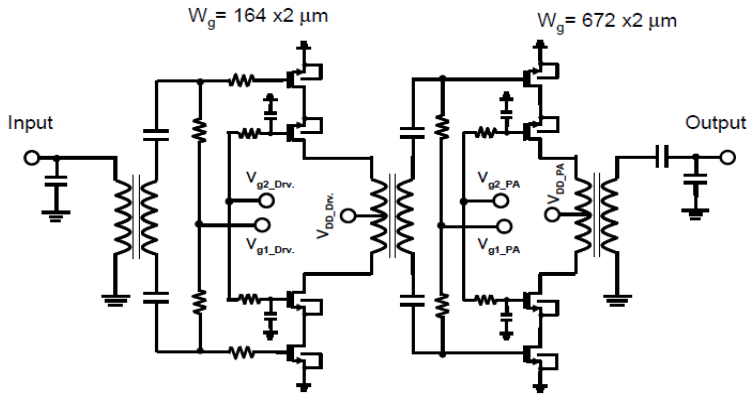

Figure 3. K-band differential power amplifier[7]

In 2011, [9] proposed two-stage design, and the complete schematic was shown in Figure 4. The transistor (M3, M4) in the second stage and the first stage (M1, M2) are selected to be 56 fingers with 6-um unit finger width and 48 fingers with 4-um unit finger width, respectively. The proposed power amplifier was implemented in a 0.18-um CMOS technology. All of the passive components including spiral inductors and MIM capacitors are simulated by full- wave simulator. The chip size of the PA was 0.47 x 0.65 mm2 including all testing pads. This PA has a P1dB of 16.8 dBm with 15.5% PAE at 21 GHz, and the peak PAE is 18.9% while the output power is 18 dBm.

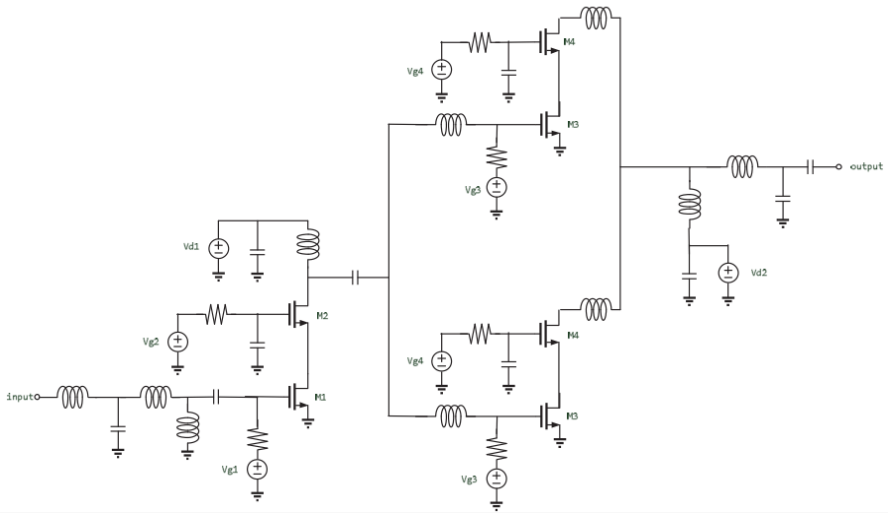

Figure 4. CMOS Cascode power amplifier with optimum bias selection[9]

In 2011, [10] proposed power amplifier with adaptive bias for enhancement in back off efficiency as shown in Figure 5. In this design, two diode-connected transistors are inversely shunted at the gate of the CS stages and with quiescent bias voltage of 0.2 and 0.35 V. The diode of the second stage with total periphery of 54 µm is biased at 0.35 V. With the 1-kΩ bias resistor, the diode is expected to generate a dc voltage of

0.35 V in order to lift the gate bias from 0.65 to 1 V when the PA is operated at its OP1dB. This PA has a P1dB of 16.8 dBm with 15.5% PAE at 21 GHz, and the peak PAE is 18.9% while the output power is 18 dBm.

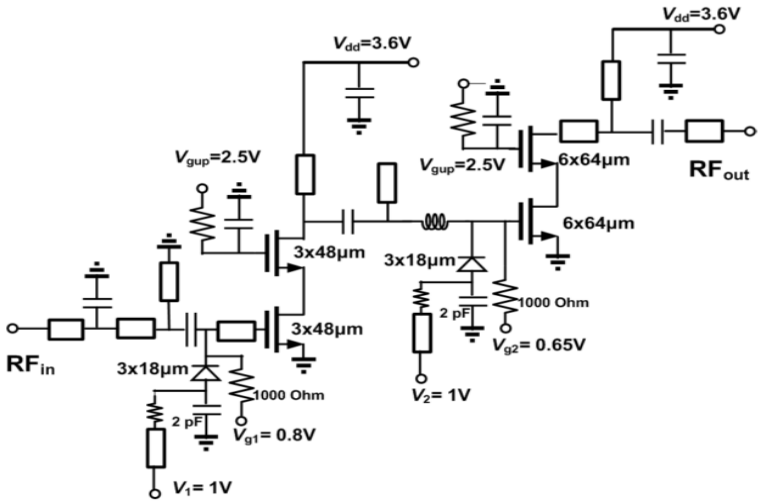

Figure 5. CMOS power amplifier with adaptive bias[10]

In 2012, [11] proposed two stages cascode device with input, output, and inter-stage matching networks as shown in Figure 6. In order to achieve maximum output power, the transistors (M3, M4) of the second stage are 64 fingers with unit finger width of 6 11m. In order to achieve higher power added efficiency (P AE), the transistors (Ml, M2) of the first stage are selected to be 16fingers with unit finger width of 6 um.The amplifier achieves a high gain of 19 dB, and delivers an output power of 19 dBm with 24.7% PAE at 24 GHz and OPldB is 15.7 dBm.

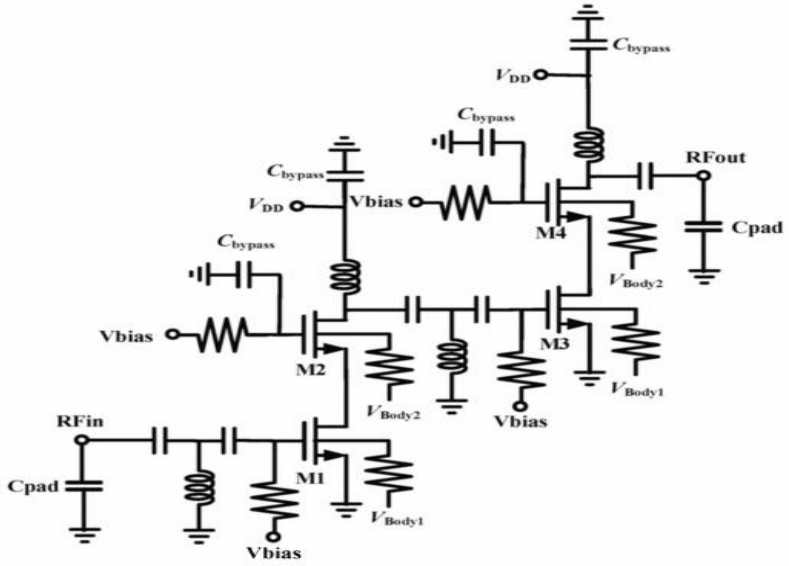

Figure 6. CMOS power amplifier with reverse body bias [11]

In 2014, [12] proposed two cascaded cascode stages for high power gain, followed by a common source stage as shown in Figure 7for high power linearity. To increase Psat and PAE, the output stage adopts a Wilkinson-power-divider- and combiner-based two-way power dividing and combining architecture.The

proposed PA achieves power gain of 21.5 ± 1.5 dB forfrequencies 22.7–26.9 GHz, and excellent Psatof 5.9dBmand relatively high PAE of 14.6 % at 24 GHz. Theseresults demonstrate the proposed PA architecture is verypromising for 24-GHz short-range communication system applications.

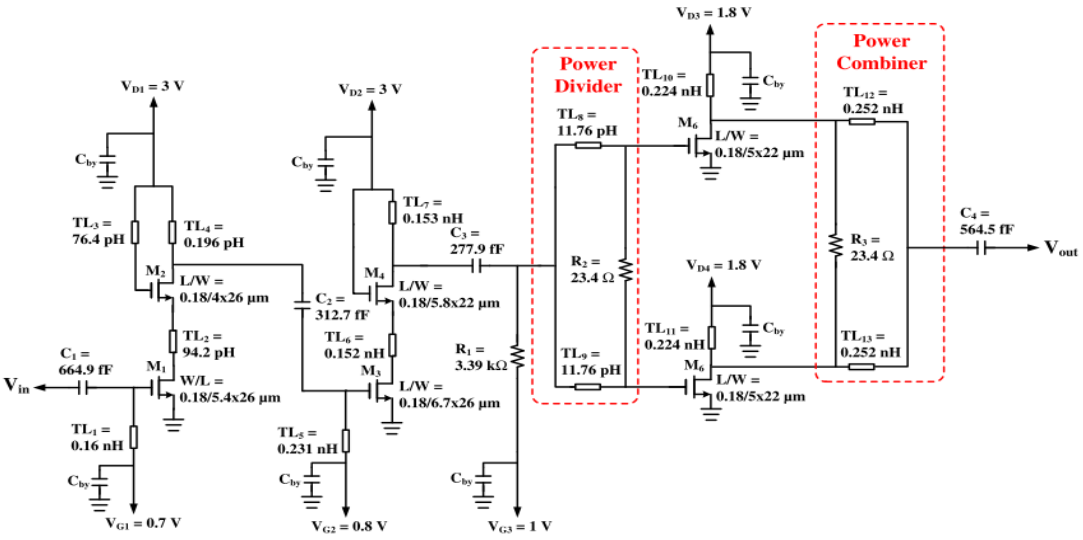

Figure 7. Two cascade cascode CMOS power amplifier [12]

In 2015, [13] proposed adaptive bias with enhanced linearizer as shown in Figure 8. Although the common-source is the simplest topology for PA design, the common-source PA cannot achieve sufficient gain at high frequency due to the Miller effect from the parasitic capacitance. Therefore, the cascade topology is used to reduce the Miller effect by common-gate transistor and improve the high frequency performance. The power stage is chosen for higher output power under the tradeoff between power capability and gain due to the parasitic effect.The proposed PA demonstrates outstanding 6.8%PAE at 6-dB back-off from P1dB, 14.1% PAE at OP1dB, and high linear output power 9.2 dBm with IMD3 of -40 dBc. The proposed PA can deliver comparable linear output power with the lowest quiescent power consumption and achieve better efficiency in back-off operation.

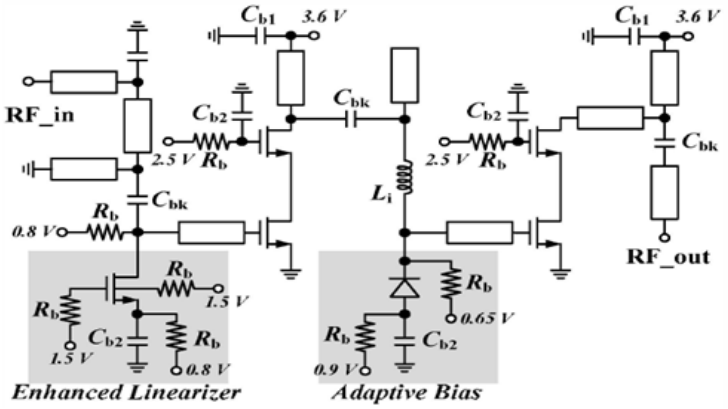

Figure 8. CMOS power amplifier with adaptive bias selection[13]

In 2016, [15] proposed two stages PA as shown in Figure 9. The stagger tuning concept is employed, where gain flatness is accomplished by using two different center frequencies at 20.5 GHz and 15.5 GHz for the first and the second stage, respectively. The tuning frequencies (peak gain frequencies) of

the two stages are adjusted by optimizing the width of transistors M1, M2 and M3, which control the current-gain cut off frequencies wt1, wt2 and wt3. The first stage is designed to achieve a high unilateral gain while for the second stage is designed and optimized to achieve maximum PAE and output power.The proposed PA has a measured power gain of 10.5 +- 0.7 db and average saturated output power of 14dBm across the bandwidth. In addition, it achieves a small group delay variation of +- 20ps and maximum PAE of 26% which is the highest among the recently published 0.18um CMOS Pas while consuming 50 mW of DC power.

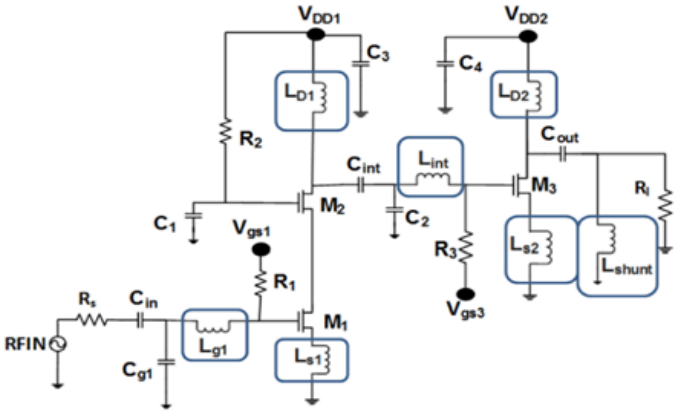

Figure 9. Two stage CMOS power amplifier[15]

In 2016, [16] proposed one-stage differential structure having a harmonic control circuit to minimize the 2nd harmonics produced by the non-linear CS amplifier at the drain and source as shown in Figure 10. By short circuit the drain and source, 2nd harmonic issue can be reduced as it will be trap at drain and source. 2nd harmonic need to be eliminated as it generates sideband asymmetric resulting lower PAE.The CS / 2 Stack PAs achieve PAE of 27% / 25%, and EVM of 5.17% /4.2% and ACLRE-UTRA of -33 dBc / -33 dBc, respectively, with an average output power of 9.5 dBm / 14.2 dBm at 28.5 GHz for a 20-MHz BW, 64QAM, and 7.5-dB PAPR LTE signal.

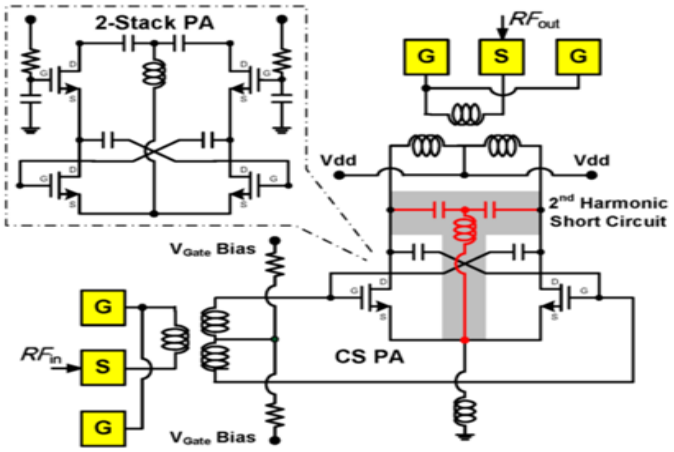

Figure 10. One-stage differential structure CMOS power amplifier with a harmonic control circuit[16]

Later, [17] proposed a small inter-stage inductor between the cascode common-source and common-gate to improve PA's output power and PAE as shown in Figure 11. The input balun separates the single-ended RF signal into a pair of differential signals, and then these signals are amplified through two-stage cascodeamplifiers, in the end the output balun merges the differential signals for a higher output power. Two

tuning capacitors beside the baluns are used to help realize input and output impedance matching. The inter-stage matching network is composed of two spiral inductors and two MIM capacitors. The cascode structure is adopted to get a higher power gain and reverse isolation. A series inter-stage inductor is added between the common source and common gate transistors to improve the output power and PAE of the PA. The chip occupies 0.66 mm×1.09 mm including all DC and RF pads. The supply voltage is 3 V, the gate bias voltages VB1 and VB2 are 0.95 V, 2.7 V respectively. Result shows S21 is above 21 dB from 27.5-28.5 GHz. When operating at 28 GHz, the saturated output power (Psat) is 20 dBm, the output-referred 1-dB compressed output power (OP1dB) is 15.7 dBm, the maximum power gain (G) is 22.6 dB, the peak power added efficiency (PAE) is 19 %.

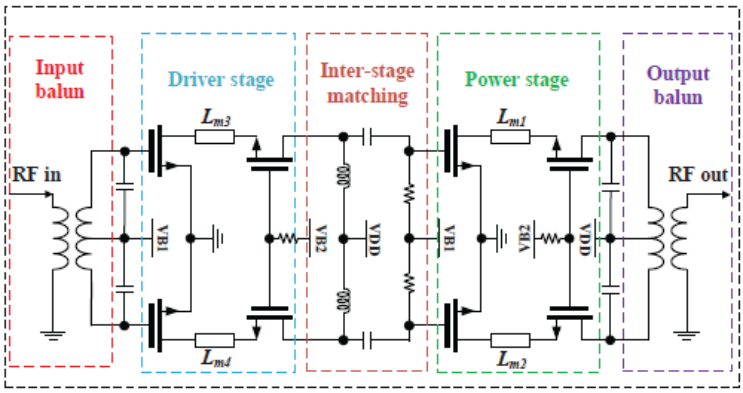

Figure 11. CMOS power amplifier with a harmonic control circuit[17]

In 2018, [18] proposed a high-efficiency frequency reconfigurable CMOS power amplifier (PA) design technique at 24 and 28 GHz using integrated tunable neutralization and matching networks as shown in Figure 12. Figure13(a) and (b) shows the circuit diagram of a conventional fixed coupling-coefficient transformer (kfixed) and the proposed reconfigurable coupling-coefficient transformer (krec), respectively. The proposed krec is achieved by adopting a switched substrate-shield inductor tuning topology [19] cope with the adverse effects of gate–drain capacitance (Cgd) in millimeter-wave (mm-wave) CMOS PAs in deep-submicron technologies. The reconfigurable coupling coefficient can be achieved in a two-coil system by introducing a third coil which can modulate the inductance of the Ld and Lg depending on the state of the third coil, and thus, the coupling coefficient. Figure 13(c) and (d) shows the circuit diagram of the proposed concept, where krec can be controlled by setting the gate voltage (VSW,TFR) of the switch (Msw) in the third coil.These techniques enable high efficiency in a PA prototype in 65-nm CMOS, obtaining better than 40% PAEsat at both 24 and 28 GHz.

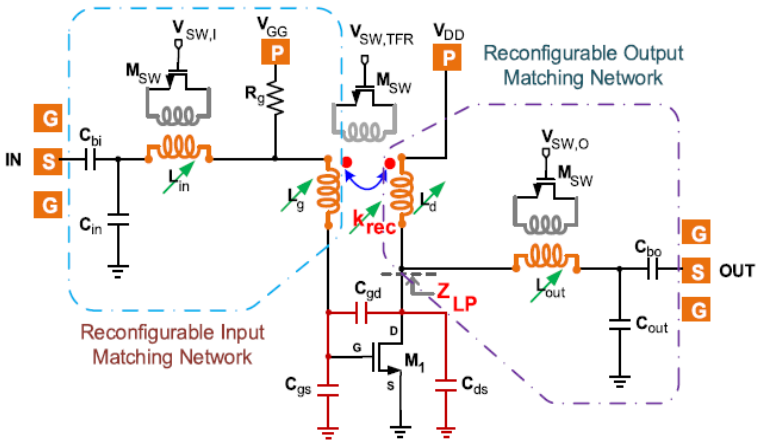

Figure 12. CMOS power amplifier with integrated tunable neutralization and matching networks[18]

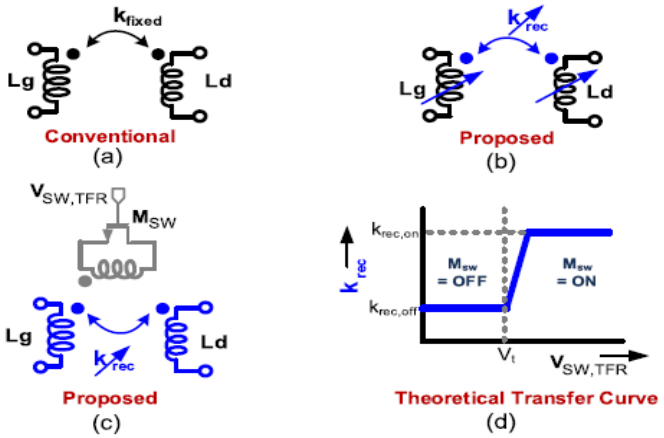

Figure 13. Circuit diagram of (a) conventional fixed, (b) proposed (conceptual) reconfigurable coupling-coefficient-based transformer, (c) practical realization of (b) with a control switch of MSW, and (d) theoretical relationship between krec and VSW,TFR [18]

3. PERFORMANCE SUMMARY

Table 1 shows the summary of the performance CMOS PAs design from 2009 to 2018 in Ka-Band frequency for 5G application. As can be seen, most of the PA design meets the gain requirement of less than 10 dB, except the PA with Cascode Pair [2]. The high gain can also be achieved easily when the PA is designed using 2-stage cascade topology. Amongst all the works, the PA with minimal bias selection [3] and power combiner [6] achieve good gain, output power and PAE which is suitable for 5G applications. Furthermore, most of the works manage to get good PAE using 2-stage cascade topology. Besides, design with tunable gate-drain also shows the promising results with PAE higher than 40%. However such design can lead to bigger size as additional transformer design need to be consider in the architecture.

Table 1. Performance Summary of CMOS PAs at Ka-Band Frequency for 5G Application

Ref & Year	Technology	Frequency (GHz)	PAE %	Gain (dB)	Pout (dBm	Technique
[6] 2009	0.18 um CMOS	20-24	10.7	15	16.8	2-stage Cascode.
[7] 2011	65 nm CMOS	16-25	25.1	22	23.8	2-stage Cascode.
[8] 2010	0.18 um CMOS	24	20	8	22	1-stage Cascode.
[9] 2011	0.18 um CMOS	21	18.9	20	18	2 Stage cascade with optimal bias selection.
[10] 2011	0.18 um CMOS	22	12	11.9	15.4	2-stage cascade with adaptive bias.
[11] 2012	0.18 um CMOS	24	24.7	19	15.7	2 Stage cascade with reverse body bias.
[12] 2014	0.18 um CMOS	22-29	14.6	23	22	2 Stage cascade with power combiner.
[13] 2015	0.18 um CMOS	23	16.8	14.5	12.4	2 Stage Cascode with
	0.18 um CMOS	23	15	12.8	15.8	Linearization On & Off
[15] 2016	0.18 um CMOS	12-24	26	10.5	12	2 stage.
[16] 2016	28 nm CMOS	28.5	25	13.6	18.6	1-stage , 2-stack.
[17] 2016	0.13 um CMOS	28.5	25	13.6	18.6	2-stage Cascode.
[18] 2018	65 nm CMOS	28.5	40.1	8.9	14.4	1-stage CS with Tunable Gate–Drain Neutralization

Over the past decade, PA mostly used expensive technology, for example, Silicon Germanium (SiGe) orGallium Arsenide (GaAs) to be realized in transmitter. During that time, the PA was not achievable in CMOS technology due to its limitation. With the increasing of CMOS technology used in cellular phones and millions of devices that are developed and marketed at monthly intervals, it becomes a motivation to all researchers to investigate and demonstrate new topology and architecture that are different from the PA topologies as summarized in Table 1. However, based from the data obtained, it is found that the usage of CMOS power amplifier still has its limitation that needs to be improved and strengthened in the future PA

topology. Firstly, the CMOS PA have been studied intensively, however the question of which PA topologies is the best topology still has not been resolved. The result shows that there is trade-off between the characteristics, and difficult to achieve all design specifications over high frequency spectrum.

Secondly, many studies have shown great effort and achievement, but several characteristic shortcomings of the CMOS, such as lower fT of transistors that has not been discussed in detail before, causes the circuits design in CMOS enormously challenging indeed.

4. CONCLUSION

A review of CMOS power amplifier design techniques in Ka-Band frequency for 5G application has been discussed. Several approaches PAs have been implemented with different kind of topologies. The performance of the CMOS PA depends on the selection of the techniques and requirement of 5G applications. Current publish has achieved very good PA performance in Ka-Band frequency for 5G application. Up to date, design with Tunable Gate–Drain Neutralization for 28-GHz reported highest PAE with 40.1 % and 14.4 dBm Pout. This review hopefully can help to facilitate other researchers working in the area of power amplifier circuit design.

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