Indonesian Journal of Electrical Engineering and Computer Science
Vol. 13, No. 2, February 2019, pp. 801~807
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v13.i2.pp801-807

A comparison of performance between double-gate and gate-all-around nanowire mosfet

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Article Info

Article history:

Received Oct 24, 2018
Revised Nov 25, 2018
Accepted Dec 29, 2018

Keywords:

Complementary Metal-Oxide-Semiconductor
Double-Gate MOSFET
Gate-All-Around MOSFET
Short channel effects (SCEs)
Technology Computer-Aided Design (TCAD)

ABSTRACT

Due to the rapid scaling of Complementary Metal-Oxide-Semiconductor (CMOS), the structure of the planar MOSFET approaches the scaling limits when the short channel effects (SCEs) become the main problem. The Double-Gate and Gate-all-Around nanowire MOSFETs are said to be the promising candidate to replace the planar MOSFET in order to pursue CMOS scaling. Therefore, this paper present the result of device simulation using Silvaco TCAD tools for Double-Gate and Gate-All-Around nanowire MOSFETs. The purpose of this simulation work is to compare the performance of GAA nanowire and DG MOSFET and then study the effect of physical parameter on electrical behavior for both devices. The result of the simulated model of Gate-All-Around nanowire is compared with published data. It was found that when the gate length of DG was scaled from 80nm to 10nm, the subthreshold slope is increasing from 62mV/dec to 162.7mV/dec. While for GAA, the subthreshold slope is increasing from 65.8mV/dec to 127mV/dec. The threshold voltage in DG and GAA at Lg=80nm are 0.40646V and -0.17505V respectively. Even though heavy doping was good for suppressing SCE, the lower doping concentration is desirable as the DG and GAA nanowire had higher on-state currents with 1.42x10-3A and 3.23x10-4A respectively. It also showed that the threshold voltage of DG and GAA nanowire increase from -0.0734V to 0.2312V and -0.0319V to 0.2232V respectively when the channel doping is varies from lower to higher concentration.

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1. INTRODUCTION

Recently, the efforts to make a miniaturization of electronic component with a great performance are actively carried out by industry. The requirement mention by the ITRS [1] and demand from the industry for high speed and low power device has triggered chipmakers and transistor designer to produce a reliable device. Therefore, a rapid scaling towards nanoscale regime are widely done to increase the chip density in order to achieve a great quality product. Note that when the channel length of the devices is narrowed, the ability of the gate to control the channel will degrade. This will lead to the SCEs problem such as increase of leakage current, threshold voltage roll-off and some others problem related to SCE [2]. Since planar MOSFET can no longer sustain the SCE problem when scaling down, many alternatives have been proposed

to overcome the problem. Double-Gate (DG) and Gate-All-Around nanowire (GAA nanowire) MOSFET have been considered as reliable candidate to replace the planar MOSFET [3-5]. Many of the architectures that have been proposed consist of two or more gates to control the channel. Both of the device are able to extend the use of CMOS technology as they are good at suppressing SCE [6].

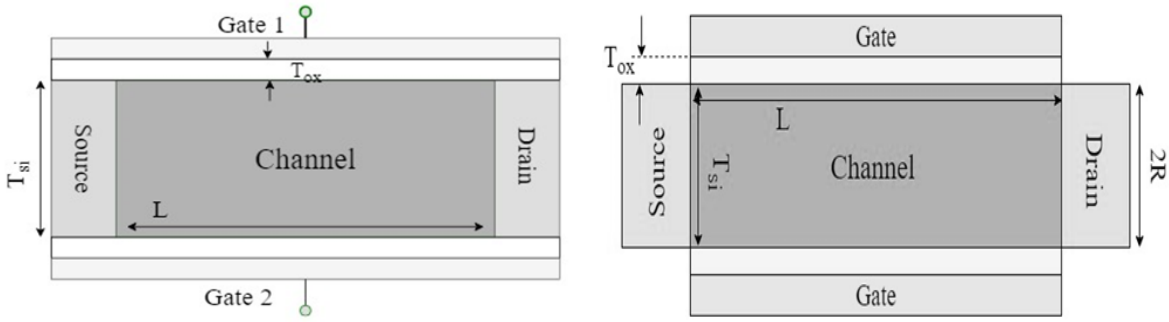
The process of performance enhancement and modification of the device need to be continued over time to identify the optimum conditions that a device can achieve. Hence, a new structure design, and dimension should be improved to keep the SCE problem under control when scaling down the channel length. By manipulating the physical parameters such as silicon thickness (tsi), gate length (Lg) and also doping concentration will help to improve the performance of the device. Hence, the transfer characteristics (ID-VG), leads to measuring several device parameters such as subthreshold slope (SS), Threshold Voltage (VTH), and also the ratio of ION/IOFF. These parameters will disclose the effect of scaling towards the performance of the device.

2. DEVICE STRUCTURE AND SIMULATION

3D view of the proposed cylindrical gate-all-around nanowire MOSFET generated by ATLAS as shown in Figure 1.

Figure 1. 3D view of the proposed cylindrical gate-all-around nanowire MOSFET generated by ATLAS

The device simulation was done by using ATLAS simulator in Silvaco TCAD tool. Both DG and GAA MOSFET have n-type channels with a doping region of NA=1.45x1010cm-3, while the source/drain doping concentration was set to 1x1020 cm-3. Basically, the physical parameters that consist of the gate length (Lg) that was set to 1µm, 10nm for the silicon thickness (tsi) and the gate oxide thickness (tox) was set to 1.5nm. Figure 2 shows the illustration of the DG and GAA MOSFET cross-section structure used in this study. The advantage of nanowire channel is that it will reduce the corner effects that lead to lower current drive face by the cubical channel [7].



(a) (b)

Figure 2. (a) The structure of DG MOSFET and (b) GAA nanowire MOSFET

First of all, the device simulator is used to validate models of GAA MOSFET with the published data [8]. Figure 3 shows the comparison of I-V characteristics that have a good agreement when compared to the reference model.

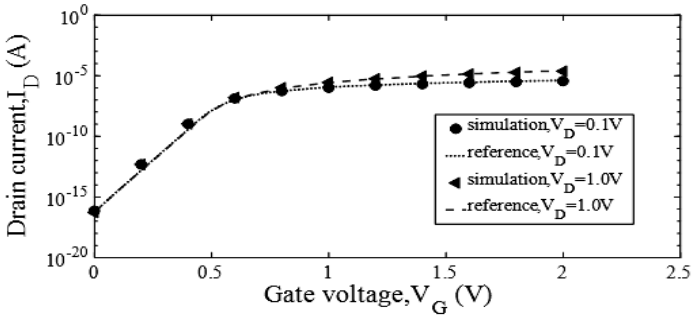


Figure 3. Transfer characteristics at VDS = 0.1V and 1.0V of the simulated device and the reference model (dashed line)

3. RESULTS AND ANALYSIS

3.1. Comparison of GAA and DG MOSFET Performances

We compared the basic model of DG and GAA nanowire with the same physical parameter and dimension to observe their performance. Figure 4 shows the comparison of transfer characteristics for both DG and GAA MOSFET. The results show that GAA has a bigger ION/IOFF ratio with 4.395x1011 compared to DG with 6.378x108. A bigger ION/IOFF ratio will lead to a better performance and very small of IOFF current is essential for static power reduction while the device is in an idle state [9]. Even though the on-state current of GAA is smaller, it has a very small off-state current Besides that, DG has better value of SS with 59.6 mV/dec compared to GAA MOSFET with 221.8 of SS value. Normally, devices that have better SCE immunity has better characteristics of SS where the desired value is at 60mV/dec.

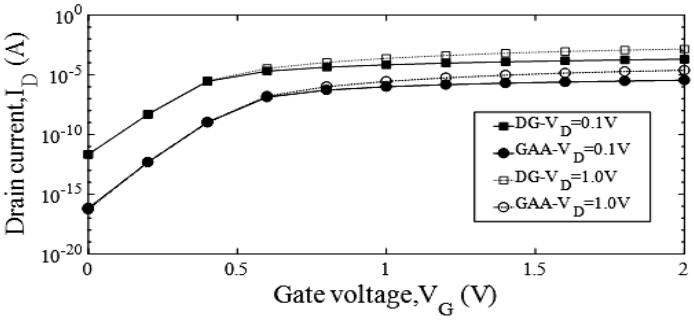


Figure 4. Transfer characteristics of simulated DG and GAA MOSFET at VD = 0.1V and 1.0V

3.2. The Effect of Variation Physical Parameter towards Electrical Behavior

The process of scaling MOSFET will eventually lead to a smaller gate length, oxide thickness and also the channel thickness. Thus, in order to observe the performance of the device, the variation of the scaled dimension must be simultaneously observed with the related electrical parameter characteristics. Firstly, this study focuses on the scaling of gate length. By taking the various gate lengths starting from 80nm, 60nm, 40nm, 20nm to 10nm, observations have been made regarding the subthreshold value, threshold voltage, I_{ON} and I_{OFF}. The reduction of the drain current was noticeable as the gate length increased due to high channel resistance [10]. When the gate length is shorter, it clearly shows that the subthreshold slope will increase due to the increasing drain current as shown in Figure 5. The figure shows the simulation results of subthreshold slope for both DG and GAA when the gate length is varied. But the increment rate of subthreshold slope for GAA is much better than DG because it is still in the acceptable values even though the gate length approaches 10nm.

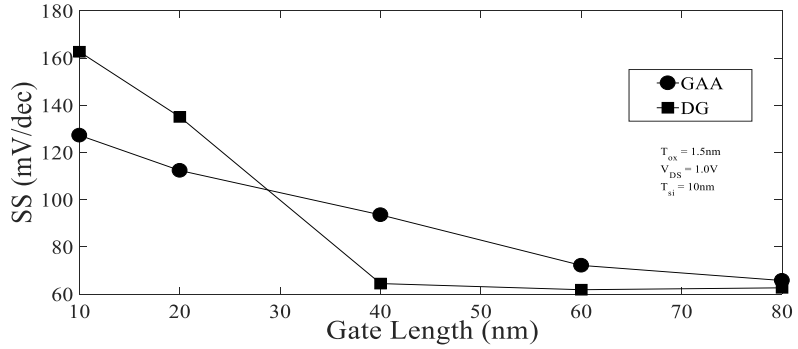


Figure 5. Subthreshold slope of DG and GAA MOSFETs with variation of gate length (Lg)

Besides that, the effect of the gate length scaling towards the threshold voltage has been plotted in the graph to see the behavior of the electrical parameter. Figure 6 shows the relationship of the threshold voltage with the variation of gate length. In all cases, below the critical length Lg>100nm, threshold voltage will decrease with the decreasing gate length. Once the critical length is met, the properties of the threshold voltage can be varied. Based on observations, the reduction rate of the threshold voltage in DG is smaller than in GAA. A lower threshold voltage is desirable especially for low power application. It was found that GAA MOSFET having a better subthreshold slope but then it has a really low threshold voltage compared to DG.

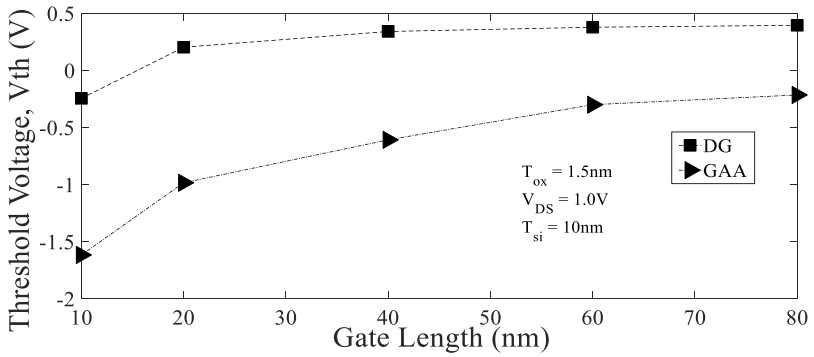


Figure 6. Threshold Voltage characteristics of DG and GAA MOSFETs versus the gate length, Lg

One of the ways to optimize the characteristics of MOSFET device is to modify the silicon film thickness. It is practical to depend on the film thickness since it is desirable to lessen the floating body effect. Figure 7 shows the relationship between the threshold voltage and the silicon film thickness. The gate length was set to 1µm. Based on observation, the threshold voltage of the device will increase when the silicon film thickness increase. Studies have found that even though there is only small increment, the value of threshold voltage increase with the increasing of silicon film thickness [11]. But when approaching L_g< 30nm, the results may be contradict. When the silicon film thickness is greater, the increasing width of the depletion regions will decreases the source/body and drain/body junction capacitance. It will cause the gate and surface potential coupling increases, thus the threshold voltage decreases with the increase of silicon film thickness [12]. It shows that the gate length do effect the relationship between threshold voltage and silicon thickness. The gate length and the film thickness should not be excessively scaled even though the lithography allowed it in order to minimize the SCE.

With the gate length scaling approaching sub-100nm regime, the body-doping concentration becomes one of the requirements to control the SCEs and improves the performance of the device [13]. Figure 8 shows the comparison of I-V characteristic for both DG and GAA with two different doping concentrations. Since early simulations have implemented low doping concentration for the channel, this part of the study is to compare and observe the electrical behavior for lightly doped, $3x10^{16}$ cm^{-3} and the heavy doped channel with $5x10^{18}$ cm^{-3}. Heavy channel doping concentration is desirable for suppressing SCEs.

However the lower doping concentration results in a better saturation region and higher current drive. Besides that, lowering the concentration of the doping will lead to better mobility and less velocity saturation [14].

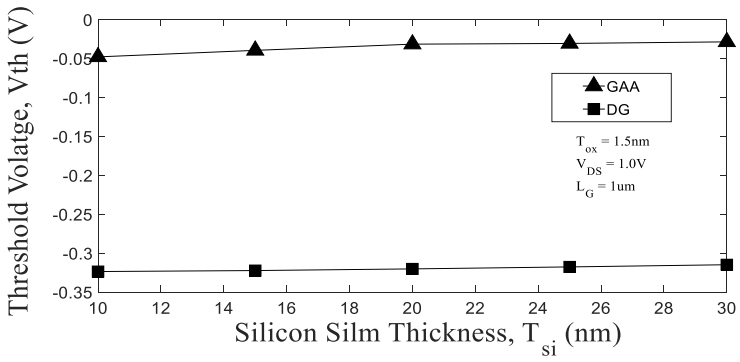


Figure 7. Threshold voltage Vth versus silicon film thickness Tsi

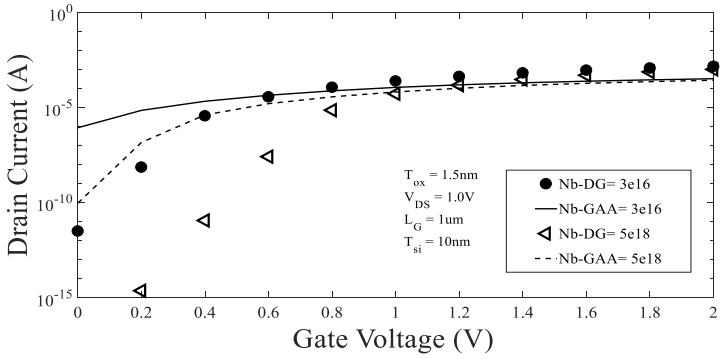


Figure 8. I_D-V_G curves of DG and GAA for different concentration of body doping profile

Table 1 show the results of various electrical parameter of both device when the doping concentration is varied. It shows that the value of the subthreshold slope decreased when the doping concentration, as well as the drain current increased. Meanwhile, the value of threshold voltage will increase when approaching higher doping concentration. As for DG, the threshold voltage increased from -0.0734V to 0.2312V when the doping concentration is changing from low-doped to heavy-doped. The GAA nanowire had a smaller increment of threshold voltage from -0.0319V to 0.2232V when the doping concentration increased.

Table 1. The results of electrical parameter for DG and GAA nanowire MOSFET with vary doping concentration

Device	Parameter	Low-doped ($1x10^{10}$ cm^{-3})	moderately-doped ($3x10^{16}$ cm^{-3})	Heavy-doped ($5x10^{18}$ cm^{-3})
DG	I_{ON} (A)	$1.42x10^{-3}$	$1.42x10^{-3}$	$9.99x10^{-4}$
	I_{OFF}(A)	$2.99x10^{-12}$	$3.17x10^{-12}$	$2.367x10^{-15}$
	I_{ON}/I_{OFF} ratio	$2.11x10^{-9}$	$2.23x10^{-9}$	$2.37x10^{-12}$
	SS(mV/dec)	59.6	59.5	48.9
	V_{TH} (V)	-0.0721	-0.0415	0.4020
GAA	I_{ON}(A)	$3.23x10^{-4}$	$3.23x10^{-4}$	$4.69x10^{-4}$
	I_{OFF}(A)	$8.69x10^{-7}$	$8.92x10^{-7}$	$9.46x10^{-11}$
	I_{ON}/I_{OFF} ratio	$2.69x10^{-3}$	$2.76x10^{-3}$	$2.02x10^{-7}$
	SS(mV/dec)	221.8	219.5	62.7
	V_{TH}(V)	-0.0319	-0.0303	0.2232

4. CONCLUSION

The simulation of model DG and GAA was completed using Silvaco TCAD tools. The comparison of performance between the DG and GAA was observed and analysed. Even though there are changing in the dimension when scaling the transistor size, the degradation rate of GAA is still better than in DG. When gate length is shorter, the subthreshold slope will increase especially when Lg<30nm. It shows that DG will have higher subthreshold slope with 162.7mV/dec compared to GAA with 127mV/dec when Lg<30nm. While when Lg>30nm, GAA have better subthreshold trend which are nearly-ideal value compared to DG. Besides that, the changes in doping concentration gives an impact on the device as it provides a higher drain current and decreases threshold voltage when the body concentration is lower. While heavy doped region is good SCE controller. Lower-doped channels in GAA had 3.23x10-4 A of on-state current and threshold voltage of -0.0319V compared to heavy-doped with 4.69x10-4A and 0.2232V respectively. However, DG MOSFET is beneficial for ultralow power application due to its near-ideal subthreshold slope characteristics and it can also achieve better isolation at lower control voltage. The behavior showed by GAA indicates that it is more affective in suppressing short-channel-effects than DG MOSFET at Lg=1µm. This is because GAA has better threshold voltage characteristics, exhibits higher ION/IOFF compared to the DG MOSFET. The degradation rate of subthreshold slope in GAA is better compared to DG when scaling. It also found that, GAA is more suitable for high speed and low power application since it can reduce SCE and has better performance when scaling compared to planar MOSFET. But, the fabrication and process variation is still a concern for GAA nanowire when it continues to scaling down.

ACKNOWLEDGEMENTS

The authors would like to acknowledge the financial support from the Research University grant of the Ministry of Higher Education (MOHE), Malaysia under the Fundamental Research Grant Scheme (FRGS) vot no 1535. Also thanks to the Research Management Centre (RMC) of Universiti Tun Hussein Onn Malaysia (UTHM) and Universiti Teknologi Malaysia (UTM) for providing excellent research management and facilities in which to complete this work.

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