Indonesian Journal of Electrical Engineering and Computer Science
Vol. 14, No. 2, May 2019, pp. 780~787
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v14.i2.pp780-787

Design and implementation of embedded concurrent laser missile jammer system using FPGA

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Article Info

Article history:

Received Sep 14, 2018
Revised Nov 25, 2018
Accepted Dec 8, 2018

Keywords:

Field programmable gate array
Missile jamming
Real time system
Spatial parallelism

ABSTRACT

In real time system, every second takes into count as any extra delay could cause critical consequences. Nowadays, almost every system involving multiple data processing. To handle multiple data at the same time, spatial parallelism is required to enhance system performance and provide multitasking feature. Currently, frequency jamming system only can jam one signal at a time. When it comes to missile jamming, the delaying in processing the frequency could cause serious impact as there will be multiple missiles launched to hit a target. These missiles just need few seconds to hit the target within range. Laser missile jammer is designed, which can jam multiple missiles at a time from different directions. The potentials of Field Programmable Gate Array (FPGA) and spatial parallelism is used in this system, to enhance the performance of the system by increasing operating frequency, system throughput, decreasing system cost, power consumption of the system, and get lower complexity. Quartus II version 14.1 is used in this project as a development CAD tool, the entire system implemented on FPGA DE1-SoC board. Also, other components such as Laser Detector, Laser Transmitter, and monitoring screen is integrated with the board. A signal emulator module was designed, to generate signals for on-board self-testing purpose, this system can detect the frequency of laser missile and create an over-powered signal with similar frequency to jam the missile(s) through diffused plates. All the results are shown on control display. This system had achieved a better throughput and lower complexity in terms of less resource usage (3153 Logic Elements) and high operating frequency (up to 1.6 GHz).

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1. INTRODUCTION

A jamming system is defined as a system that has the ability to disturb communication between devices by preventing receiver to receive sender's signal. There were many usages of frequency jamming. Police and military could use frequency jamming to disturb the communication between the opponents while terrorist can use frequency jamming to prevent people from calling help from police and etc. [1].

Another major usage of frequency jamming is to jam missile(s) launched from the opponent to avoid protected target from being destroyed or to protect certain important person from being attacked. In this project, a laser missile jamming system will be designed, which has the ability to jam guiding signal of multiple missiles launched from attacker and leading the missile(s) away from the target [2].

The jamming of the missile consists of two parts, which is to disturb the ranging guidance system from the attacker and to jam the launched missile by frequency jammer. In order for a missile to be fired, range have to be first determine by using laser. The disturbance of the range guidance will cause difficulty

for enemy to release the missile and giving the jamming system a chance to detect the position of the fighter jet [3, 4].

While frequency jammer is used to disturb any transmission of a signal, including the ranging guidance [5]–[6] signal and missile directional signal [7] through the use of over-powered signal in the same frequency. It will first detect the frequency of the laser signal from the fighter jet, after analyzing the signal, frequency jammer will then send an over-powered signal with the same frequency to lead the missile away from the protected target [8, 9].

2. RESEARCH METHOD

According to our research, current frequency jammer [10] only able to jam a signal at a time. When it comes to missile jamming, even a small delay will cause serious consequences. In order to solve this issue, a concurrent laser missile jammer is designed, and this laser missile jammer will have the ability to jam multiple signals at the same time. In order to achieve this purpose, spatial parallelism [11] is used in this project. Besides spatial parallelism, the internal clock frequency of DE1-SoC board [12] had been increased using Phase-Locked Loop (PLL) [14], to further enhance the system performance and improve the accuracy of the detected frequency. Further details of PLL will be discussed in this section. However, there were still many steps needed in order to design this concurrent laser missile jamming system, and all these will be explained in details throughout this section [13-14].

2.1. Flow of the System

Basically, the system continuous reading input from surrounding, by using signal detector. If there is any signal detected, the system will perform counting operation, for every pulse detected from the surrounding the system counts once, and the total counts within one operating clock is used to calculate the frequency of the detected signal.

After obtaining the details of the detected signal, the system will then generate another overpowered signal, with similar frequency and modulation of the detected signal to take over the control of the missile, leading the missile away from the protected target. It is noted that the performance of the system is highly related to the operation of the system in and out through the memory. Therefore, Input Data Buffer [15] is used to store temporary data, such as details of the detected signal. By using this method, the operation time of the system can then be reduced since the system no longer need to interface with the memory in this case in order to use the data for further operation.

The final step of this project is to apply spatial parallelism to the system. Since there might be multiple missiles launched to hit a target, therefore the system should be able to perform every operation, without unnecessary delay. While more details of spatial parallelism will be further discussed in the next section.

2.2. Top Level Design

Nowadays, embedded system is getting more complex and complicated. Due to this, it is very difficult for designer to design the whole design in one-piece. The solution is to design the entire system in top level of abstraction, which separates the system into several parts, each part consists of its own specific functionality [16]. The main code then connects each and every block of module, or component to form a complete system. As compared to low level abstraction design, top level design has a lot of advantages in terms of reducing circuit complexity, at the same time, do not decrease the functionality of the whole system. Moreover, designing the system in top level also helps in debugging whenever error occurs. This is very important as finding a small error in a large system is exclusively difficult.

Figure 1 shows the top level design view of the laser missile jammer system. As shown in the Figure 1, there were test module, which consists of signal emulator and signal receiver, just to test the performance of the jamming system. While the jamming system consists of 4 processing units, which continuous receive signal from surrounding. Whenever the system receives any signal(s), the system will determine the frequency of the signal and send another over-powered signal with similar frequency to diffused plate to lead the missile away from the protected target.

There was also conversion module inside the jamming system, just to decode the signals into presentable data so they can be shown on the display module. This system provides several display models. Thus, user could select to show the data on seven segments, Liquid Crystal Display (LCD) or even monitoring screen by using Video Graphics Array (VGA).

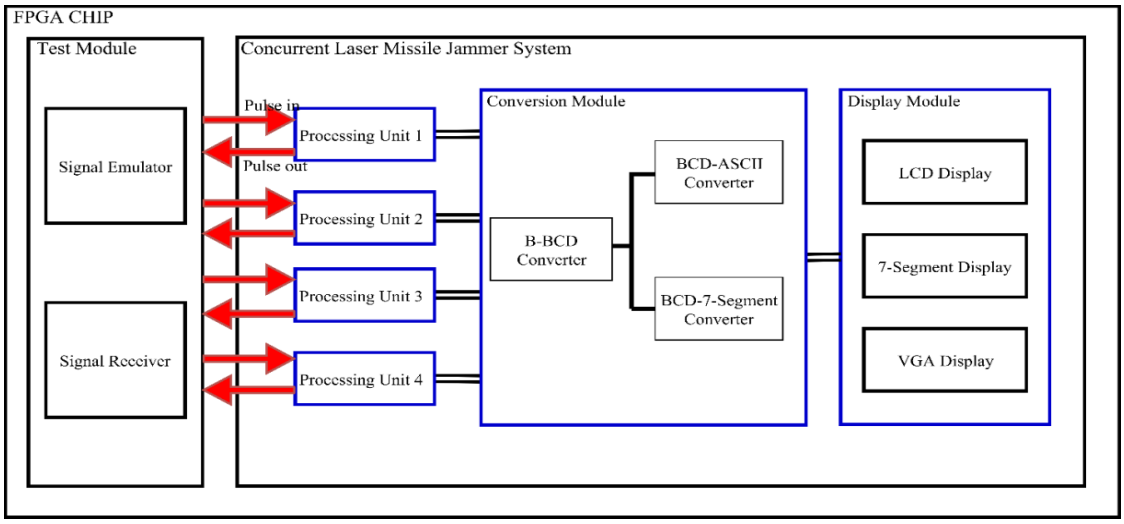

Figure 1. Top level design of the concurrent laser missile jammer system

2.2.1 Test Module

There were Signal Emulator and Signal Receiver inside this test module. Signal Emulator is to generate several of required frequencies for system testing purpose. The system should be able to react and perform required operation whenever signal is generated from this module. Besides that, this signal emulator also able to generate multiple signals at the same time through different directions, to demonstrate the situation, and analyze the performance of the jamming system, when multiple missiles are sent to hit the target. While Signal Receiver is used to verify the performance of the system, by checking the signal(s) generated from the jamming system.

2.2.2 Conversion Module

Conversion Module is used to convert zeros and ones from binary data into presentable data. Binary data will first be converted to Binary Coded Decimal (BCD) by using shifting technique, this BCD data will then be converted to Seven-segment code and American Standard Code for Information Interchange (ASCII) to be used in display module.

2.2.3 Display Module

As discussed in above, user could select 3 types of display as they wish, which is Seven-segment display, LCD display and monitoring screen by using VGA. Whichever the display model is, real time data from the system will be shown. For LCD and monitoring screen, we separated the display into 4 quadrants, status from 4 platforms will be concurrently showing on the screen. While for seven-segment, it can only show status of one platform at a time. User could change the platform on seven segments easily by pressing a push button.

2.2.4 Processing Units

Processing Units are the main module in this system. There were 4 processing units working concurrently in this system, which has the function to detect any signal transmit towards the target, determine the frequency of the detected frequency and generate another over-powered signal to the diffused plates to lead the missiles away from the protected target. Figure 2 shows the lower level view of processing unit. As shown in the Figure 2, each processing unit consists of several sub-modules, to provide the processing unit different functionality. The description of each sub-module as follows.

a) Phase Locked-Loop (PLL)

PLL is used in the system, to increase the operating frequency of pulse detector, to improve the accuracy of data out from pulse detector.

b) Pulse Detector

Pulse Detector is used to detect signal from surrounding and for every pulse-in, the counter increment by one, providing the output of total operating per detected pulse to the system. Figure 3 shows the relationship between detected pulse and operating clock.

c) Clock Generator

Clock generator is used to generate multiple clock signals, with different frequency for different module's usage.

d) Input Data Buffer (IDB)

It is well known that the performance of the system is highly related to the accessing time of the system to the memory. In order to further enhance the performance of the system, IDB is used, just to temporary store the data of the detected frequency, so the system do not have to access the memory all the time.

e) Frequency Calculator

By using the output from pulse detector, frequency calculator could calculate the frequency of the detected signal, by using formula below:

$$f_d = \frac{f_o}{N} \quad (1)$$

Where f_d = Detected Frequency
f_o = Operating Frequency
N = Total operating clock per pulse detected

f) Pulse Generator

Generate pulses by using calculated frequency.

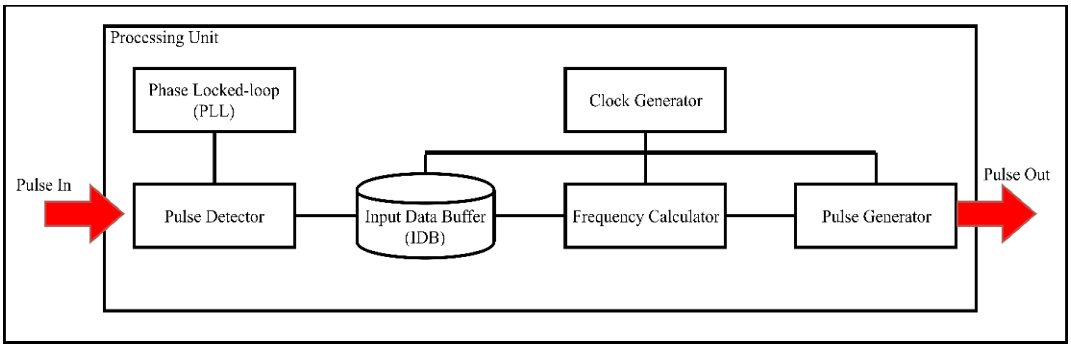

Figure 2. Lower level design view of processing unit

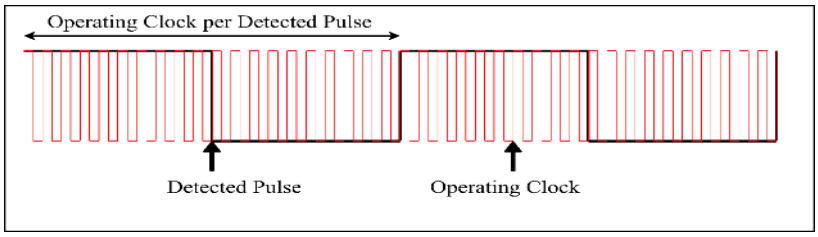

Figure 3. Relationship between detected pulse and operating clock

3. RESULTS AND ANALYSIS

By using Methodology stated above, we had built our system and below are the results:

3.1. Components Testing

Before the system build, components have to be tested first. There were 2 types of components used in this system, which is laser transmitter and laser receiver. Figure 4 shows the testing of laser transmitter with 50kHz pulses provided. Noted that the laser light is blinking in high speed (50,000 times per second), therefore we could not see it with naked eyes.

Next, we connect laser receiver to the oscilloscope, to test the reaction of the laser receiver with respect to the frequency transmitted by laser transmitter. Figure 5 shows the initial condition of laser receiver, without receiving any signal while Figure 6 shows the reaction of laser receiver with respect to 10kHz frequency transmitted by laser transmitter.

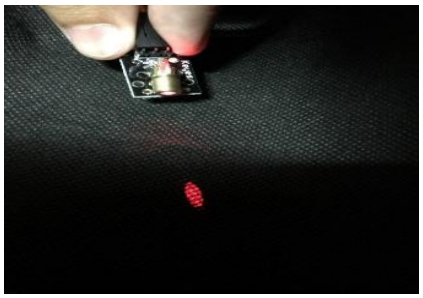

Figure 4. Laser transmitter testing with 50kHz frequency

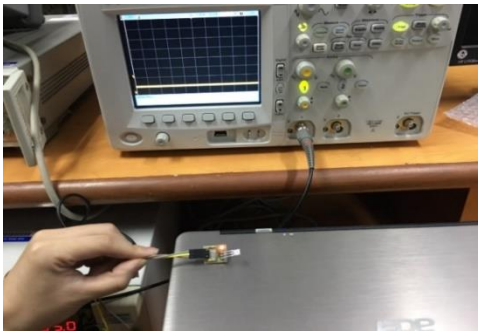

Figure 5. Laser receiver testing (without input signal)

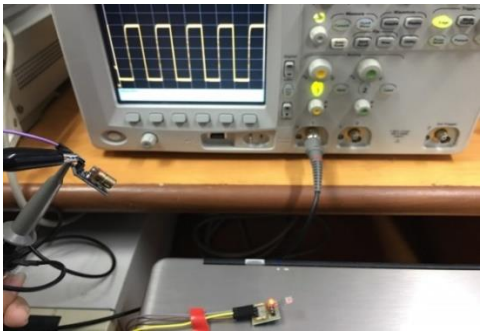

Figure 6. Laser receiver testing (with 10kHz input signal)

3.2. Single Processing Unit Design Testing

After the components had been tested and the result was satisfied, we start to design our main processing unit. This single processing unit is then being tested using internal signal provided from board, then proceed with external signal from function generator. Figure 7 shows detected frequency by the board, with respect to the external signal, 80kHz provided by function generator. Next, the system is then tested by interface the laser detector to the board. Figure 8 shows the reaction of the board towards 80kHz provided by laser transmitter.

Figure 7. System reaction towards 80kHz provided by function generator

3.3. Applying Spatial Parallelism

After every result had been satisfied, is time to apply spatial parallelism to the system. The processing unit is then being duplicated into 4, each of them is then doing its operation by itself. For easy design and illustration purpose, DE2 board had been used and the status of each platform is shown in the LCD screen and seven segments on DE2 board. Noted that the LCD screen is divided into 4 segments, concurrently showing the status of each platform, while seven segments are only able to show one status at a

time. User could change the display to other platform just by pressing push button. Figure 9 shows the LCD screen and the seven segments after applying spatial parallelism to the system.

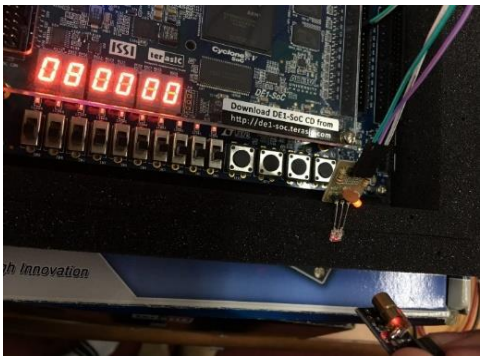

Figure 8. System reaction towards 80kHz provided by laser transmitter

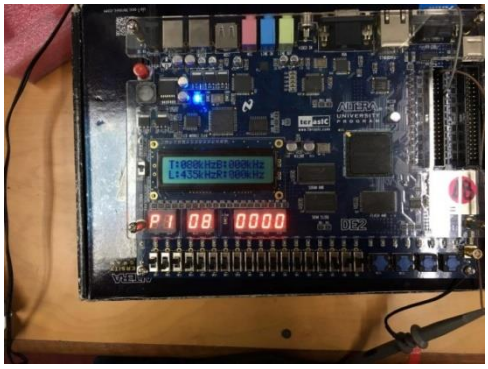

Figure 9. After applying spatial parallelism

3.4. VGA Interface

After spatial parallelism successfully implemented in DE2, the results are then being display in monitoring screen concurrently using VGA, since the main board, DE1-SoC did not have built-in LCD screen. As can be seen in Figure 10, the monitoring screen is separated into 4 segments, each showing the status from different platforms.

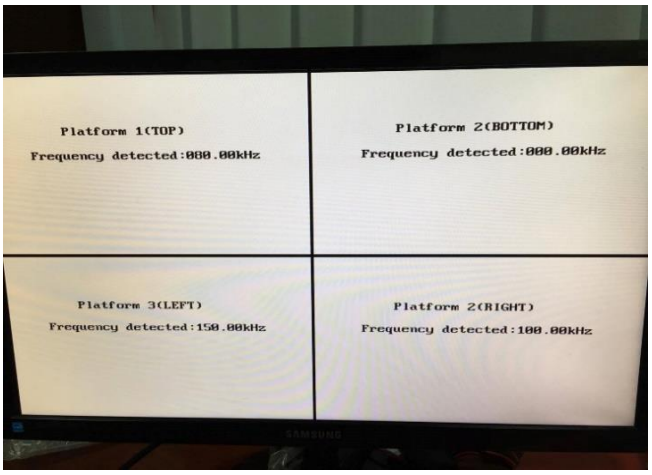

Figure 10. Results display on monitoring screen

3.5. Prototype Interface

The last step is to interface the design with prototype. Figure 11 shows the designed prototype for this project. This prototype is designed in such a way that simulate 4 missiles are to be launched to hit the target in the middle. The jamming system consists of 4 laser detectors as well as 4 laser transmitters. Laser detector to detect the frequency of laser transmit in that direction and generate a jamming signal with similar frequency using laser transmitter.

Figure 11. Prototype of the system

3.6. Discussion

In order to jam a missile, the system would need to detect the frequency of the missile and generate another over-powered signal with similar frequency. By sending this frequency through diffused plate, the missile will choose to follow the higher power's signal, which is transmitted by the jamming system. Hence the missile can then be lead to other location away from the target. However, this project is just to detect the frequency from the missile and generate another over-powered signal with similar frequency. The diffused plate control did not take into consideration due to the time and resource constraint.

4. CONCLUSION

The Concurrent Laser Missile Jammer System had been successfully designed and implemented on DE1-SoC board. The result of this system was satisfied and achieved a very good performance and throughput. However, as mentioned in the discussion, it still can be enhanced and completed by taking the diffused operation into consideration, which can be considered as future work.

ACKNOWLEDGEMENTS

The authors would like to thank the Ministry of Education Malaysia (MOE) for providing the FRGS research grant (Grant no. 9003-00474) and School of Computer and Communication Engineering, University Malaysia Perlis (UniMAP) for support.

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