

## Performances analysis of reducing router in ring and mesh topology for Network-on-Chip (NoC) architecture

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### Article Info

#### Article history:

Received Sep 27, 2018

Revised Nov 25, 2018

Accepted Dec 7, 2018

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#### Keywords:

Network-on-chip

Reducing router in a mesh

Reducing router in a ring

System-on-chip

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### ABSTRACT

The size of the transistor has reached physical processor limitation in particular for traditional bus-based and point-to-point architecture in system-on-chip (SoC). Therefore, network-on-chip (NoC) was proposed as a solution. The performances required for the optimization of the NoC are low network latency, low power consumption, small area, and high throughput. However, recently the size of the NoC architecture has increased and the communication between cores to core become complicated. To overcome this disadvantages, topology plays an important role. In this paper, we reduce the number of the router in the 16 cores and 64 cores ring and mesh topologies by connected more numbers of node in each router. Result shows that reducing the number of the router in 64 cores ring topology outperforms the conventional topologies in term of area, power consumption, latency, and accepted packet rate. Reducing router in 64 cores ring topology decrease the average area, power consumption, latency, and increase the average accepted packet rate by 160.45%, 23.88%, 54.76%, and 223.88% over the 64 cores mesh, reducing router in mesh, ring, and cross-link mesh topologies.

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## 1. INTRODUCTION

As the number of core increasing, the microprocessor industrial is moving from single core to multi-cores. Therefore, an efficient interconnection between processor is required. Point-to-point architecture and buses architecture is introduced before network-on-chip (NoC) architecture. The goods of buses interconnection architecture are scalable and reusable, but because of the shared channel as the broadcast channel, only one communication between nodes is allowed at a time. When the number of node and communication between a source and destination node increasing, time of delay become longer and total power consumption is increasing as the number of data to be sent is increasing. In the point-to-point architecture, the complexity of wiring grows as the number of IP core increasing, making it unable to scale.

Topology plays an important role in NoC, choosing a topology will affect the overall performance, such as increasing the latency, power consumption and degradation in communication quality [2]. The routing area, delay, and power consumption is increasing as the IP core increasing. Therefore, the reducing router in ring and mesh topologies technique is proposed. Besides that, a cross-link mesh topology is proposed by adding 8 additional links to mesh topology to reduce the average number of hop count to send the packet from source node to destination node. Figure 1 shows the network-on-chip architecture. A NoC consists of a router, processing element (PE), channel, and the network interface (NI) [1].

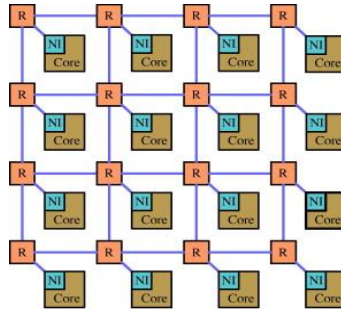


Figure 1. NoC architecture

This paper, we analyzed its architecture potential in term of total area, total power consumption, average network latency, and average accepted packet rate. We propose a reducing router in ring and mesh topologies and cross-link mesh topology. The proposed topologies is based on 16 cores and 64 cores ring and mesh topology. The aim of this work is to reduce the total area, total power consumption, and average latency. The rest of the paper is organized as follow. Section 2 presents the related work. Section 3 presents the design of reducing router in ring and mesh topologies. Section 4 presents the cross-link mesh topology. Section 5 presents the results and analysis. Finally, the last section concludes the paper.

**2. RELATED WORKS**

The number of researchers doing research on network-on-chip (NoC) is increasing. There are some technique has been proposed to improved the NoC performance. Heterogeneous and hybrid clustered topology is proposed by [3] to optimize the performances of latency and response time. The latency and response time are affected by the communication between cores. Therefore, choosing a suitable topology for network-on-chip architecture is important to optimize the latency and response time based on the communication between cores as the basic parameter. In addition, a spectral clustering approach to application specific network-on-chip synthesis proposed by [4]. Proposed method used cluster ensembles and spectral clustering to partition the system. The link between each router is created by using delay constrained minimum spanning trees. In [5], found out that clustering and message distance trade off in torus based network-on-chip. In torus topology, the clustering method has to increase the implementation costs. The clustering torus topology consumes more power compare to torus topology. Clustering methods in torus topology is benefited when there is a high degree of communication locality. Reconfigurable cluster based network-on-chip for application specific MPSoC is proposed by [6]. The nodes of the mesh topology is grouped into some cluster. The frequently communicating task of a given application is the cluster in the same group. The results from the proposed technique show a lower power consumption and performance efficiency. Energy efficient segmentation-link strategies for transparent IP over WDM core networks is introduced by [7]. The segmentation-link technique by using optical bypass and traffic grooming has reduced the energy.

**3. THE DESIGN OF REDUCING ROUTER IN RING AND MESH TOPOLOGIES**

Figure 2 shows the 4x4 and 8x8 mesh topologies. Currently, 2D mesh topology is widely used by researchers due to accepted wire cost and high bandwidth [8]. In a mesh topology, nodes is connected as a grid. In a mesh topology, the position of the node can be represented by m x n node where m and n is the node number in x-axis and y-axis respectively.

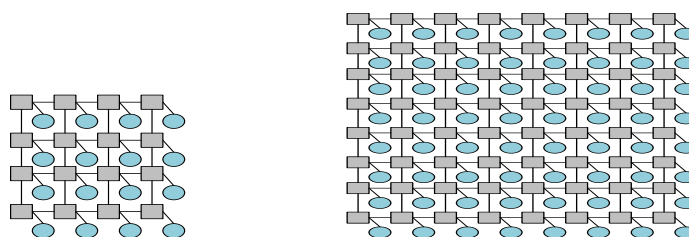


Figure 2. 4x4 and 8x8 mesh topologies

Figure 3 shows the design of reduced the number of router in 4x4 and 8x8 mesh topology. Each router in Figure 3 is connected to 4 cores. Total 12 and 48 routers have reduced compared to 4x4 and 8x8 mesh topology.

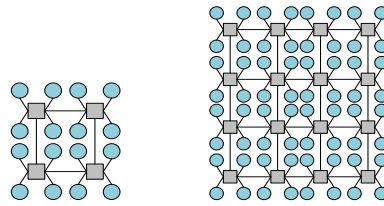


Figure 3. Reduced router in 4x4 and 8x8 mesh topologies

Figure 4 shows the 16 nodes and 64 nodes ring topology. In the ring topology, each processing element is connected to two neighbors. Low cost is needed to implement ring topology.

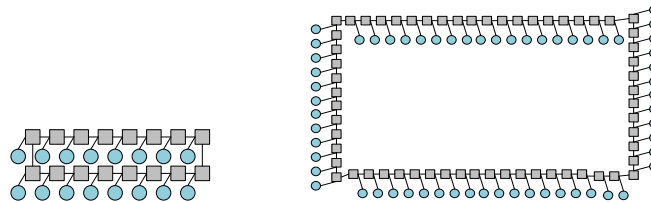


Figure 4. 16 and 64 nodes ring topologies

Figure 5 shows the design of reduced number of router in 16 nodes and 64 nodes ring topology. Each router is connected to 4 cores. Total 12 and 48 routers have reduced compared to 16 nodes and 64 nodes ring topologies.

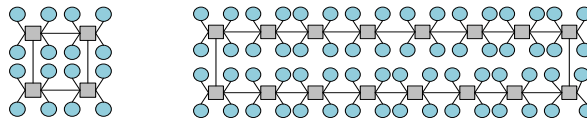


Figure 5. Reduced router in 16 and 64 nodes ring topologies

#### 4. CROSS-LINK MESH TOPOLOGY

Figure 6 shows a 64 nodes cross-link mesh topology. This topology is formed based on mesh topology. Additional 8 link is used to create 4 cross-links in the mesh topology. The purpose of the cross link is to reduce the number of hop count and the average latency to send data.

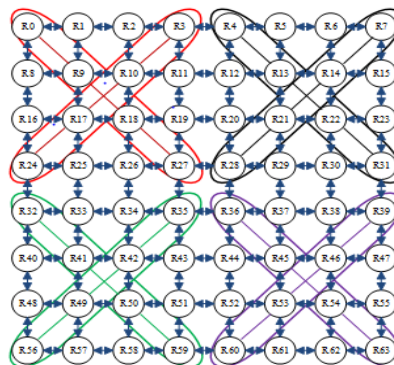


Figure 6. 64 Nodes cross link mesh topology

The summary of a number of hop count for mesh and cross-link mesh topologies is shown in Table 1 and 2. Hop count referred to the distance between the source node and the destination node.

$$\text{Average Number of Hop} = \frac{\sum_{i=1}^N \text{PacketHop}}{N} \quad [9]$$

Where N is the total number of packet arrived at the destination node. Packet hop defines as the number of hop count required to send the packet from source node to destination node [10]. Based on Table 1 and 2, cross-link mesh topology has reduced the average number of hop count compared to mesh topology.

Table 1. Average Number of Hop Count for Mesh Topology

Source Node	Destination Node	Path	Number of Hop
0	63	0→8→16→24→32→40→48→56→57→58→5	14
16	39	9→60→61→62→63	9
22	50	16→24→32→33→34→35→36→37→38→39	8
38	3	22→30→38→46→54→53→52→51→50	6
44	7	30→22→14→6→5→4→3	8
50	37	44→45→46→47→39→31→23→15→7	5
63	48	50→51→52→53→45→37	7
		55→54→53→52→51→50→49→48	

Table 2. Average Number of Hop Count for Corss-Link Mesh Topology

Source Node	Destination Node	Path	Number of Hop
0	63	0→9→18→27→28→36→45→54→63	8
16	39	16→17→18→27→28→36→37→38→39	6
22	50	22→21→28→36→35→42→50	5
38	3	38→30→22→13→4→3	5
44	7	44→36→28→21→14→7	4
50	37	50→42→35→36→37	7
63	48	55→54→53→52→51→50→49→48	

5. RESULTS AND ANALYSIS

In this section, we investigated the effectiveness of the proposed topologies. Reducing the number of the router in 16 cores and 64 cores ring and mesh topologies is proposed. The total area, total power consumption, average network latency, and average accepted packet rate of the mesh, cross-mesh, and ring topologies is compared with the proposed topologies.

Based on Figure 7 and 8, reducing a number of the router in ring and mesh topologies has reduced the total area compared to ring, mesh, and cross-link mesh topologies. Reducing router in 16 cores and 64 cores ring topology decrease the average area by 35% over the 16 and 64 cores ring topology. For mesh topology, reducing router in 4x4 and 8x8 topologies decrease the average area by 55% and 52% over the 4x4 and 8x8 mesh topology.

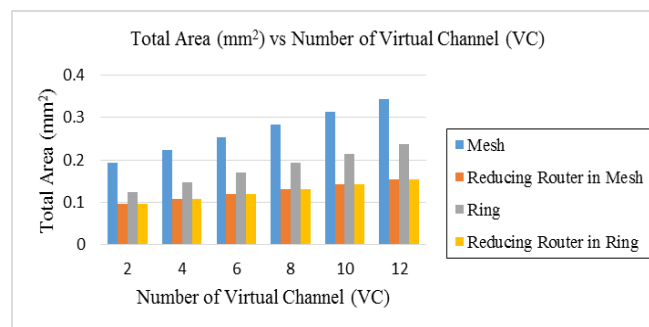


Figure 7. Total area (mm<sup>2</sup>) for 16 cores topologies

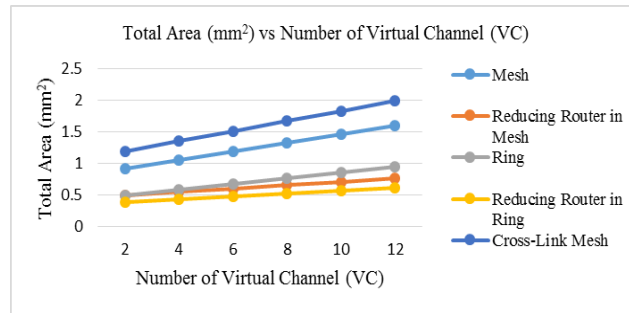


Figure 8. Total area (mm<sup>2</sup>) for 64 cores topologies

Optimize the power consumption in NoC has become attention due to the complexity of IC design increase. The total power consumption increase as the IP core increasing. The total power consumption from the interconnect can be estimated from the average communication distance. The total power to transmit a message of length can be calculated by

$$P_{total} = P_{router} + P_{link} \quad [11]$$

Where  $P_{router}$  and  $P_{link}$  are the power used to transmit the message from source node to destination node through the router and link respectively. Figure 9 and 10 shows the total power consumption in the ring, mesh, cross-link mesh, reduce router in ring and mesh topologies. The total power consumption is proportional to the number of virtual channels. To minimize the total power consumption, the technique by reducing the number of router in ring and mesh topology is proposed. Based on the result, reducing the number of the router in 64 cores ring topology has the lowest total power consumption compared to 64 core mesh, ring, and cross mesh topologies. Cross-link mesh has lower total power consumption than compared to mesh topology. However, reducing a number of the router in 8x8 mesh topology has increased the total power consumption.

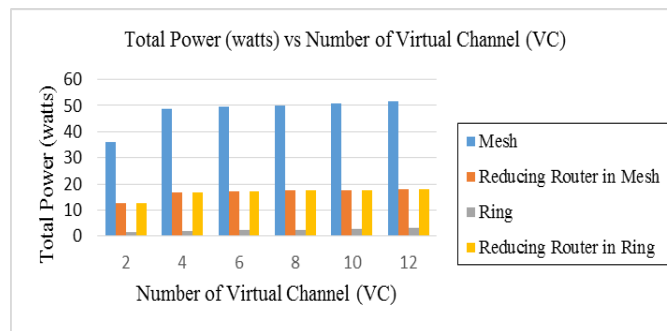


Figure 9. Total power (watts) for 16 cores topologies

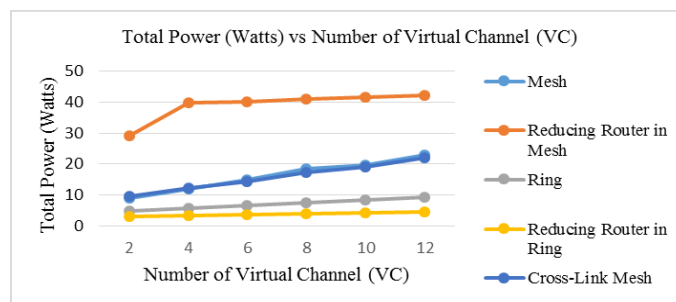


Figure 10. Total power (watts) for 64 cores topologies

Average packet latency [12] is the time needed to transmit packets from a point to another end point. A topology with the lower network latency has a better performance in NoC.

$$\text{Average Packet Latency} = L_{\text{avg}} = \left(\frac{1}{N}\right) \sum \left(\frac{1}{N_i} \sum L_{ij}\right) \quad [12]$$

Where:  $i = 1, 2, 3, \dots, N$

$L_{ij}$  = Packet J

$N_i$  = Total number packet receive by processor i

$N$  = Number of processor in platform

Based on figure 12, reducing router in 64 cores ring topology has the lowest latency compare to reduce router in the mesh topology and cross-link topology. However, cross-link mesh topology still shows a better performance compare to mesh topology. Cross-link mesh topologies reduce approximately 70% average latency compared to mesh. Reducing the number of the router is not suitable to apply in 16 nodes ring and mesh topologies. Figure 11 shows the reducing number of the router in 16 nodes topologies has increased the average packet latency.

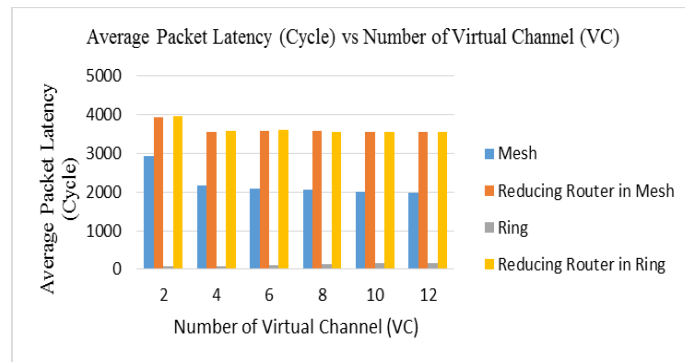


Figure 11. Average packet latency (cycle) for 16 cores topologies

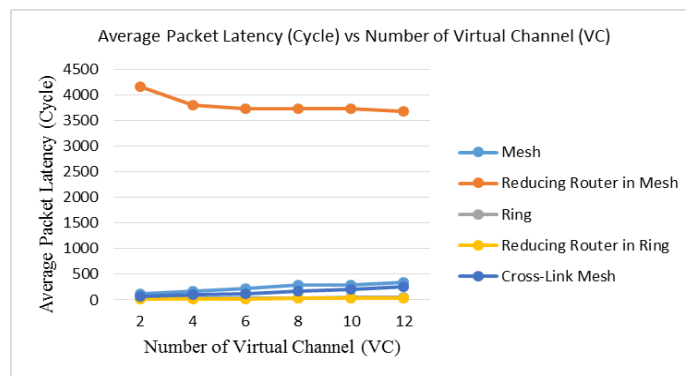


Figure 12. Average packet latency (cycle) for 64 cores topologies

The average accepted packet rate also known as throughput. Average accepted packet rate can define as the rate at which network can successfully accept and deliver packet per time unit [12]. Figure 14 shows the average accepted packet rate of 64 cores topology. Reducing the number of the router in 64 cores ring and mesh topologies has increased the average accepted packet rate compared to mesh, ring and cross mesh topologies. Based on Figure 13, reducing the number of the router in topology is suitable apply in 16 core ring topology but not suitable apply in the 4x4 mesh topology. From the result analysis, overall result shows that reducing router is suitable to apply in 64 core ring topologies.

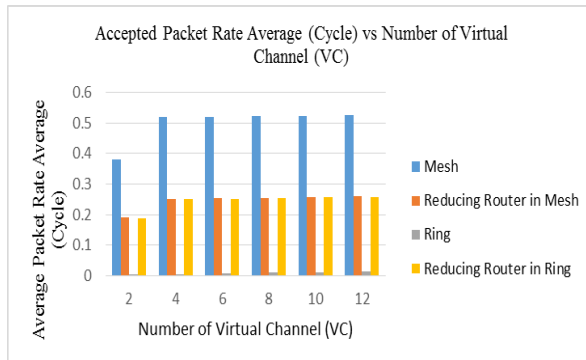


Figure 13. Average accepted packet rate (cycle) for 16 cores topologies

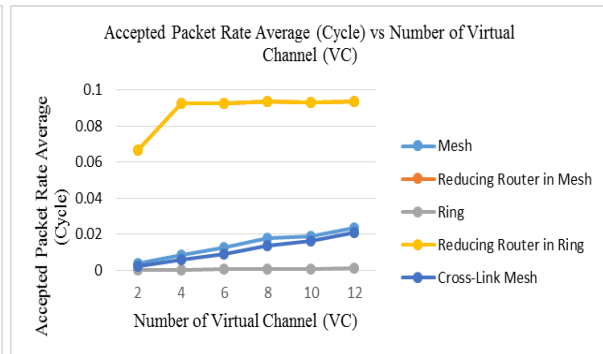


Figure 14. Average accepted packet rate (cycle) for 64 cores topologies

## 6. CONCLUSION

In this work, we have successfully presented a small area, low power, low latency, and high throughput of 64 cores ring topology. We have demonstrated the effectiveness of our proposed topology by comparing the performance of reducing a number of the router in mesh and ring topologies with the mesh, ring, and cross mesh topologies. The performance of the 16 and 64 core mesh, ring, and cross mesh topologies is analyzed in term of area, power, latency, and throughput. The experiment analysis shows that the reducing number of the router in ring topology decrease the total area, power consumption, latency and increasing average packet accepted rate by 160.45%, 23.88%, 54.76%, and 223.88% over the 64 cores mesh, reducing router in mesh, ring, and cross-link mesh topologies.

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