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Multistring seven-level quasi Z-source based asymmetrical inverter

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ABSTRACT

In this paper, a single-phase multistring seven-level Quasi Z-source based Asymmetrical Inverter suitable for grid-connected photovoltaic (PV) system is presented. This topology is an upgrade of quasi Z-source dc-dc (qZs) network and Asymmetrical multilevel inverter (AMLI). The AMLI generates a higher number of levels with reduced switch count and number of sources when compared to symmetrical cascaded based MLI. The qZs network acts as an intermediate stage between the low-voltage PV array and AMLI, to enhance the output voltage gain of the inverter. The steady state performance of the topology is verified through MATLAB simulation and experimentation. A laboratory prototype model is developed for a capacity of 200 W to validate the theoretical studies. Finally, a comparative assessment of the proposed with the existing topologies is presented.

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1. INTRODUCTION

The rise in electrical energy generation via renewable energy sources have drastically increased over the last decade. The distributed energy sources such as Photovoltaic and Fuel cell produces low voltage dc which can be interfaced to the grid only with a suitable power conditioner. The three widely used Configurations among the grid interface converters are Centralized, String and Multistring Inverters [1]. However, Multi-string inverter is quite popular due to its modularity feature which facilitates plug and play, flexible and independent control of individual string.

Multilevel Inverter (MLI) aims to offer significant advantages of the better quality of output voltage and current, reduction in filter size, enables the use of fast low voltage rating switches at high switching frequency with reduced switching losses and others when compared to conventional two-level inverters [2], [3]. The conventional and popular MLIs are Neural point Clamped (NPC), Flying capacitor (FC) and Cascaded H-bridge (CHB), well suitable for high and medium power applications. Moreover, MLI is also being adapted for low voltage and low power applications as well. Among the conventional MLIs, CHB is more suitable for PV based grid-connected system due to its modularity feature. However, Asymmetrical CHB-MLI reported in [4] requires less number of isolated dc sources and switches when compared to symmetrical MLI configurations. Recently, several inverter topologies have been introduced based on reduced switch count for increased output voltage levels. One such popular inverter is based on Packed U-Cell which utilizes one dc source and one capacitor for level generation. However, it requires complex control strategies for obtaining a seven-level output voltage. Further, it is modified by replacing the capacitor with a dc voltage source; named as Asymmetrical MLI or Modified PUC inverter which uses asymmetrical dc sources [5-6]. The maximum output voltage is equal to the sum of the input dc sources,

which is a limitation. In order to utilize this inverter for grid-connected PV system, a suitable power conditioner is necessary to step-up the low voltage dc generated from the PV.

On the other hand, Z-source inverters (ZSI) received attention for its features of inherent buck-boost capability in a single conversion stage, improved output voltage gain, increased reliability [7]. It is preferred when compared to traditional voltage source and current source inverters. Various topologies are derived based on ZSI, out of which quasi Z-source inverter (qZSI) is much popular for its continuous input current, reduced voltage stress and size of capacitor C2 and suitability to distributed generation [8-9]. The ZSI is mostly preferred for dc-dc and dc-ac power conversion. Integration of MLI in combination with Z-source based converter is preferred for renewable applications as it inherits the benefits of improved output voltage gain, better input voltage regulation, enhanced reliability, low harmonic distortion and reduced filter size [10].

Initially, Z-source based NPC is reported for three-level and five-level by utilizing two impedance networks, one or two dc sources for single-phase system [11-12]. These topologies are associated with limitation of discontinuous input current profile. Hence, a qZSI based three-level NPC inverter using the double qZs network is reported in [13]. A Z-source based seven-level inverter with reduced switches using multilevel dc link inverter is reported in [14]. A qZSI based seven-level CHB inverter [15] is reported for PV applications. From the literature [16], it is noticed that most of the Z-source based MLI topologies are based on NPC and CHB which demands more switch count, isolated dc sources and complexity in control for increased output voltage levels.

This motivates the authors to develop a multistring seven-level qZs based Asymmetrical inverter [17] with reduced dc sources, device count, size and increased overall efficiency for the grid-connected PV system. In this work, Quasi Z-source based dc-dc converter is used as the intermediate power conditioner between the PV and seven-level Asymmetrical inverter. It is utilized to boost to the desired dc link voltage in order to interface with the grid, discussed in Section 2. A comparative study is made with existing Z-source based seven-level inverters to showcase the merits of the proposed structure, given in Section 3. The theoretical studies are verified through Matlab simulation and experimental prototype, presented in Section 4. The steady state performance of the model is presented in Section 5. Finally, the concluding remarks are given in Section 5.

2. PROPOSED TOLOLOGY

Figure 1 depicts the proposed multistring seven-level qZs based asymmetrical inverter for grid-connected PV system. The qZs based dc-dc network acts as a basic unit and intermediate stage which boosts the intermittent input dc voltage obtained from the PV array, to the desired dc link voltage by regulating the duty cycle of the switches S_1 and S_2. A C filter is used for converting the pulsating dc link voltage to stable dc voltage. Each basic unit can be considered as a string. Here, two strings are considered which can be controlled independently; facilitates simple control of operation. The asymmetrical inverter is fed with two dc link voltages V_1 and V_2 whose values are binary in nature to generate the seven-level output voltages of $\pm 3V_{dc}, \pm 2V_{dc}, \pm V_{dc}$ and 0. It utilizes only six switches, out of which S_5 and S_6 are operated at the fundamental frequency. The switches S_3 and S_4 are operated at switching frequency, while the switches S_7 and S_8 are operated at around half the switching frequency. The topology can be extended to an increased number of levels, by adding the strings with suitable changes in the asymmetrical inverter. This multilevel inverter provides better performance in terms of enhanced output voltage gain with low THD, low-voltage ride through capability, filter size reduction and low EMI due to the increased number of levels.

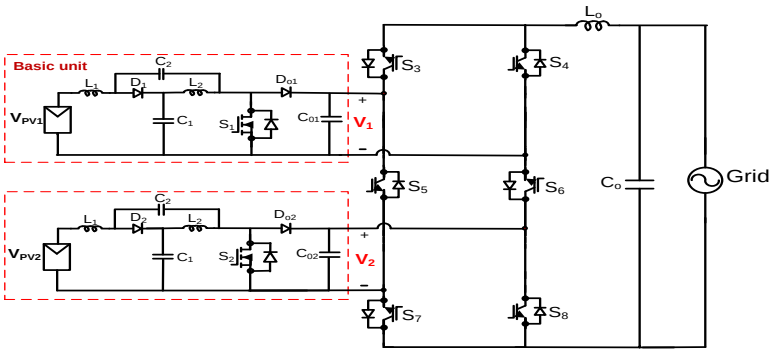


Figure 1. Proposed Multistring Seven-level qZs based Asymmetrical Inverter

2.1. qZs dc-dc Converter

The qZs based dc-dc converter boosts the input voltage obtained from the photovoltaic array to a constant dc link voltage. It consists of a typical impedance network, one switch for output voltage regulation. The C-filter is used for converting pulsating dc voltage obtained across the switch to regulated dc bus voltage V_1 and V_2. Assuming continuous conduction mode of operation, the total operating period T is basically divided into active state T_1 and shoot through state T_0. The equivalent circuits of qZs dc-dc converter under shoot-through states and active states are shown in Figure 2.

$$\frac{T_0}{T} + \frac{T_1}{T} = D_0 + D_1 = 1 \quad (1)$$

Where, D_0 and D_1 are the duty cycles under shoot through and active state respectively. The dc link voltage [18] across the switch of the qZs network is

$$V_{DC\,(max)} = V_{c1} + V_{c2} = \frac{1}{1-2D_0} V_{in} \quad (2)$$

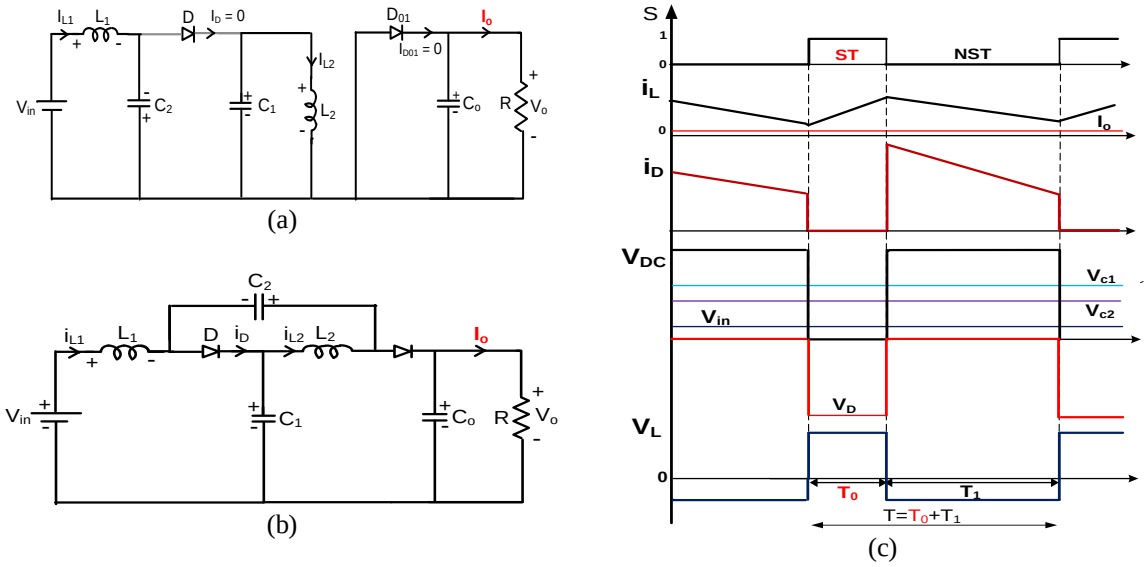


Figure 2. Equivalent circuits of qZs dc-dc converter (a) Shoot-through state (b) Active State (c) typical voltages and currents waveforms

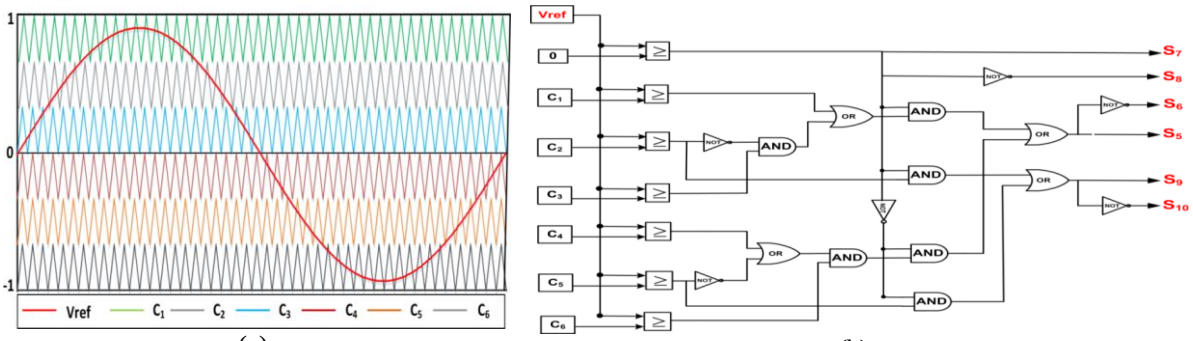
The attenuated filtered output voltage which is fed to seven-level asymmetrical inverter is given by

$$V_0 = V_{DC\,(max)} = \frac{1}{1-2D_0} V_{in} \quad (3)$$

The switches of the qZs dc-dc converter are operated at a lower duty cycle within the range of [0.1-0.3] when compared to the conventional boost converter for an equivalent output voltage gain. Operating at higher values of duty cycle invokes high input current which leads to increased losses and reduction in efficiency.

2.2. Seven-Level Asymmetrical Inverter

The asymmetrical inverter is fed with two constant dc bus voltages V_1 and V_2 obtained from the strings to synthesize the seven-level output voltage. This inverter is advantageous in comparison with CHB inverter; as it requires only six switches and operates with reduced average switching losses. However, it demands switches of different voltage ratings. The switches S_5 and S_6 are rated at $3V_{dc}$; switches S_3 and S_4 are rated at $2V_{dc}$, switches S_7 and S_8 are rated at V_{dc}. It can be noticed that the operating frequency of the switches is inversely proportional with respect to the voltage stress across the switch, which optimizes the overall switching loss. Figures 3(a)&(b) shows the multicarrier sinusoidal Pulse width modulation technique and the corresponding switching scheme for the generation of control pulses.



(a) (b)

Figure 3. (a) Multicarrier Sinusoidal PWM (b) Switching schemes for 7-level inverter

3. COMPARISON WITH EXISTING TOPOLOGIES

A brief comparison of the proposed inverter with existing seven-level qZs based inverters in terms of the number of active and passive components, total blocking voltage and control complexity is shown in Table 1. It can be noticed that the proposed inverter requires reduced switch count, less number of dc sources and inductors. The proposed inverter demands lower device count when compared to popular seven-level CHB-qZSI and Cascaded qZSI. The total blocking voltage; that is the sum of the voltage stresses across all the switches is computed to be 15 V_{dc} which is slightly higher compared to CHB-qZSI, where V_{dc} is the dc link voltage. The control is simple, as the qZs dc-dc converters consist of a single switch which can be controlled independently to produce constant dc bus voltage.

Table 1.Comparison of Proposed Inverter with Existing Topologies

Parameters	CHB-qZSI [15]	Cascaded qZSI [14]	Proposed Inverter
Input dc sources	3	3	2
Inductors	6	6	4
Capacitors	6	6	6
Diodes	3	3	4
Switches	12	10	8
Total Blocking Voltage	12 V_{dc}	18 V_{dc}	15 V_{dc}
Control Complexity	Medium	Medium	Low

4. RESULTS AND DISCUSSION

4.1. Simulation Results

Firstly, the performance of the model is tested in Matlab simulation with the parameters shown in Table 2. Assuming continuous conduction mode of operation, the steady state performance of the model is tested for input voltages VPV1, VPV2 of 30V and 60V respectively, shoot through duty cycle, DO of 0.25 to produce a desired 110Vrms ac output voltage. The values of the inductance and capacitance of the qZs network are designed as per the guidelines are given in [19]. The filter capacitor is selected as 2000µF in order to keep the voltage fluctuations in specified limits [20].

Table 2. Simulation and Experimentation Parameters

Parameters	Attributes
Inductance of the qZs converter L,r_L	0.5 mH, 0.092Ω
Capacitance of the qZs converter C,,r_c	1000μF,0.12Ω
Switching Frequency of qZs network	10 KHz
Switching Frequency of MLI	3 KHz
Filter Capacitor C_o,r_{c0}	2000μF,0.12
Filter Parameters L_f,C_f	4mH, 25 μF
RL Load	60 Ω,10 mH

Figure 4(a) shows the simulated waveforms of the input voltage, input current, diode current and dc bus voltage for the qZs I network. It can be noticed that the input current is continuous in nature, which is also evident from the diode current profile and the dc bus voltage is almost maintained constant. Figure 4(b)

depicts the dc link voltage and diode voltage which are pulsating and complimentary to each other. Figure 4(c) shows the capacitor voltages V_{c1} and V_{c2} which are boosted to 45V and 15V respectively. Figure 4(d) depicts the inverter output voltage, filtered output voltage and output current. The waveforms for the qZs II network are also similar to that of qZs I.

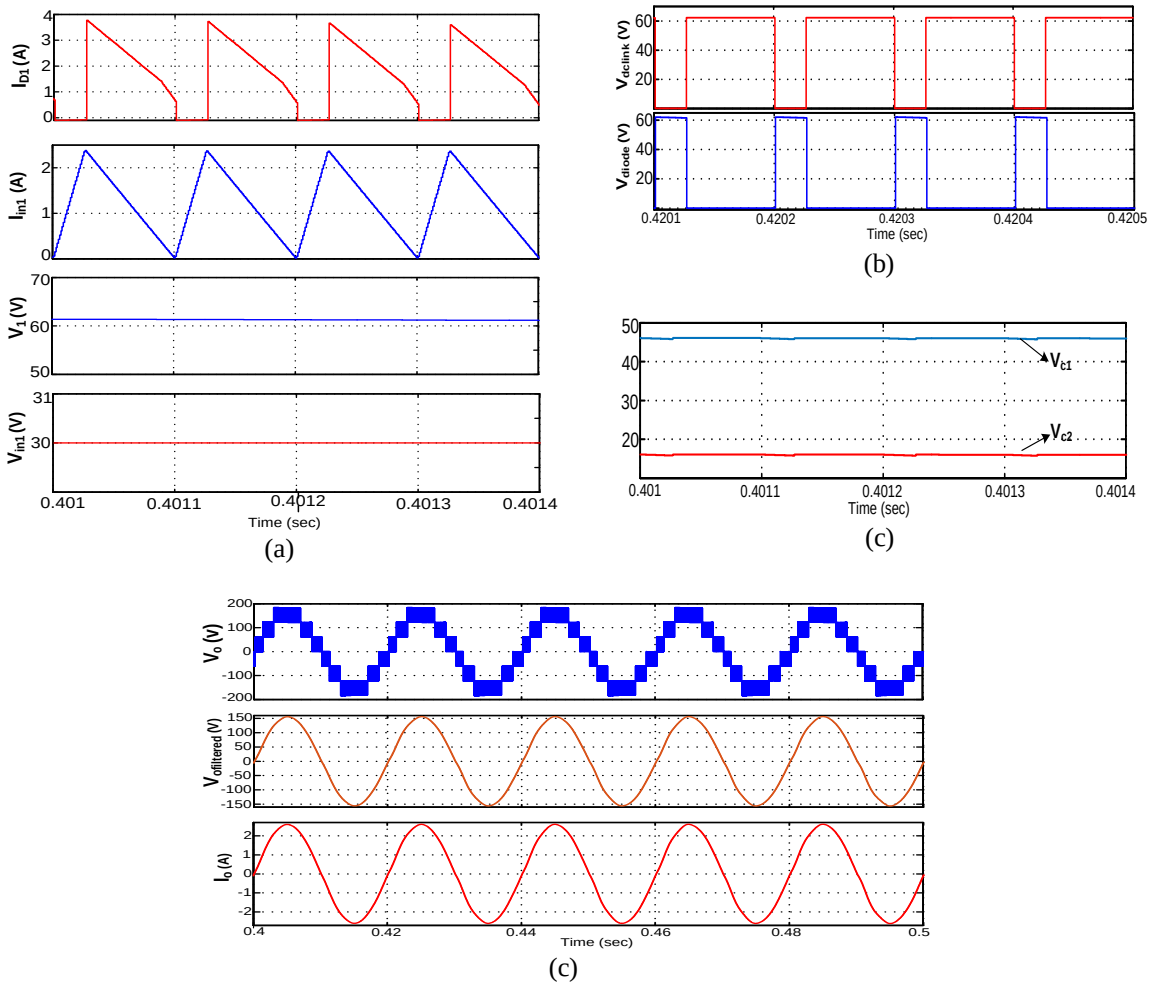


Figure 4. Simulated waveforms of (a) Input voltage, input current, diode current and dc bus voltage (b) dc link voltage and diode voltage (c) Capacitor voltages of qZs I (d) Inverter output voltage, Filtered output voltage and output current

4.2. Experimental Verification

A low-scale experimental prototype is developed as a proof-of-concept for a capacity of 200 W in the laboratory as shown in Figure 5. The gating pulses for the switches are generated using Xilinx system generator blocks in Matlab software with Atlys Spartan-6 LX45 FPGA processor. The switches IRF640N Mosfet, Schottky diode MBR20200CT are used in qZs networks, CT60 IGBT module for seven-level inverter. The TLP250 optocoupler acts as the driver circuit and provides the necessary isolation from the power circuit. Two regulated dc sources are used as input voltage sources for testing the model. The experimental results are captured using Tektronix DPO 3034 with the help of Differential probe TMDP0200 and Current Probe TCP0030.

The experimental results of the input voltage, input current, diode current and dc bus voltage of qZs I are shown in Figure 6(a). It can be noticed that during the shoot-through period, the input current increases linearly while the current through the diode is zero. From Figures 6(b) and (c), it can be observed that the dc link voltage is pulsating in nature and the capacitor voltages are boosted based on the shoot-through duty cycle and are constant in steady state. Figure 6(d) shows the waveforms of the inverter output voltage,

filtered output voltage and output current. It is evident that all the experimental results are in good agreement with the simulation results.

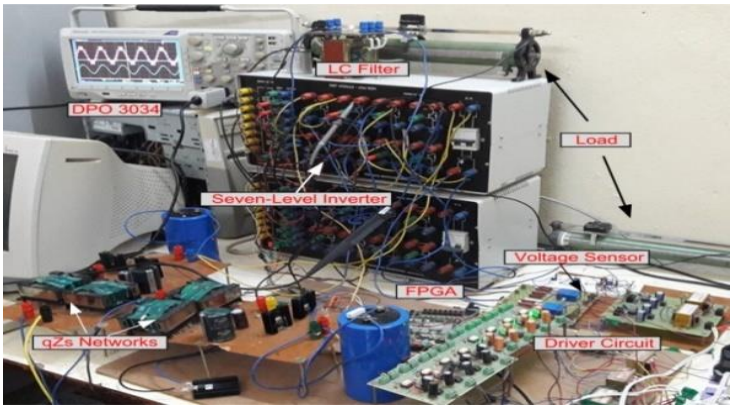


Figure 5. Experimental Setup of the Proposed Inverter

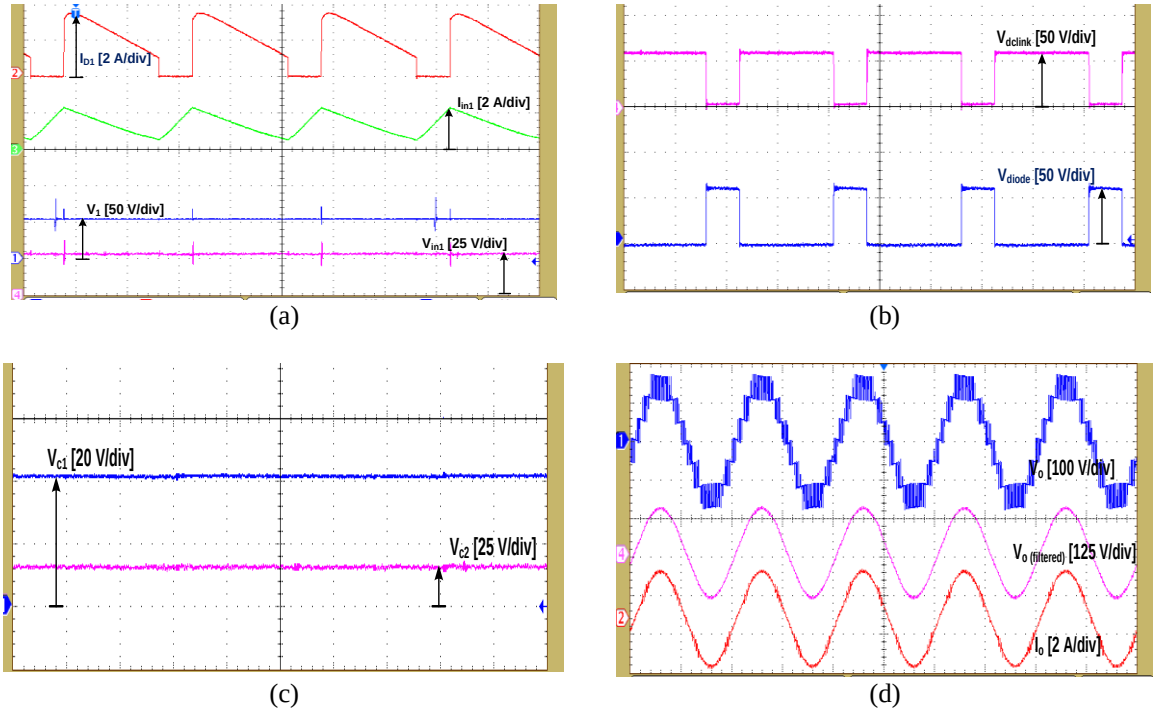


Figure 6. Experiemental waveforms of (a) Input voltage, input current, diode current and dc bus voltage (b) dclink voltage and diode voltage (c) Capacitor voltagesof qZs I (d) Inverter output voltage, Filtered output voltage and output current

5. CONCLUSION

A single-phase multistring seven-level quasi Z-source based asymmetrical inverter is presented for the grid-connected photovoltaic system. The proposed inverter is an upgrade of quasi Z-source dc-dc converter and seven-level asymmetrical inverter with features of reduced switch count, modularity, high efficiency and simple control. A brief comparative study is made to showcase the merits of the proposed inverter. The steady state performance of the model is tested and verified in simulation and experimentation, and the results are presented.

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