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# Transformerless High Gain Boost Converter for Low Power Applications with Feedback Control

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***Abstract***

*A transformer-less boost converter which provides high voltage gain without utilizing transformer or coupled inductorsandextreme duty cycle is discussed in this paper. Also it is able to cancel the ripples in the input current at a preselected duty cycle, without increasing the number of components. The converter combines the features of boost converter and a three switch high voltage converter. At the input side, two inductors are interleaved for cancelling the input current ripple and at the output side switched capacitor voltage multiplier is used to increase the voltage gain. Feedback control is used to make the output voltage constant in spite of variation in the input or load or both i.e. both line and load regulation is accompanied. This converter configurationeliminate the input current ripple and provides voltage deregulation for low power applications.*

***Keywords:*** *high gain boost converter, input current ripple cancellation, line and load regulation*



## 1. Introduction

Renewable energy sources are gaining momentum for the generation of electricity due to the rapid depletion of fossil fuel reserves. Also continuous consumption of traditional fossil energy sources leads to global warming. The voltage obtained from these renewable energy sources is usually low in amplitude; hence a boost converter is needed to step up the voltage to the required level and also to drain a continuous current with minimum ripple. Line and load regulation is also an important factor in the low power applications. Therefore this converter is more feasible for these applications.

Several other topologies have been proposed which includes the use of a coupled inductor and/or transformer, switched capacitor converter, zeta converter, bridge converter etc. The use of couple inductors sometimes induces high voltage spikes across the switch, because of the resonance between leakage inductance and parasitic capacitance which is caused by the leakage inductance energy [1]. A clamp circuit is used to recycle the leakage inductance energy in the coupled-inductor boost converter reducing the voltage stress on the switch [2]. In the capacitor-diode clamped circuit, the leakage energy is recycled in the similar way without utilizing an additional switch [3]. The use of ZCS and/ ZVS technique with coupled-inductors and transformers is presented in [4]. In this switches turned on at zero voltage and turned off at zero current. The paper presented in [5], uses coupled-inductor and voltage lifting technique to achieve a high voltage gain. In [6], a switched coupled-inductor boost converter is presented where the leakage energy is recycled by a series diode in parallel with the basic boost converter diode. The converter presented in [7] uses coupled inductor and switched capacitor technique for a flyback converter. The coupled-inductor transfers the energy to load or capacitor and leakage energy is recycled. The switched-capacitor increases the voltage gain. Similar technique is used in [8]. The converter in [9] is a non-isolated high gain boost converter based on half bridge converter; it combines features of boost converter and a half bridge converter with voltage doubler rectifier. In [10] integrated coupled-inductor and voltage doubler technique is used to achieve a high voltage gain. Converters with only switched-capacitors (without coupled-inductors) are suitable for low power applications mainly because of switching frequency limitation and current spikes in the capacitors.The interleaving of inductors also increases the gain of the boost converter as presented in [11]. Converters presented in [12] and [13] which are based on Switched-capacitor achieve a high voltage gain. For high power applications,

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converters which do not use transformer or coupled-inductor are presented in[14], [15], and [16] which are based on switched-capacitor concept. Switched-capacitor with complete charge interchange presented in [17], is not used in voltage regulation since it compromises the converters efficiency. Switched-capacitor with complete charge interchange and Pulse width modulation presented in [18] provides voltage regulation. In renewable energy applications, converter must also drain continuous current with minimum ripple in the current. The efficiency of the converter can be maximized by using soft switching technique as presented in [19].

The converter presented combines complete charge interchange – switched capacitor with a boost converter into a single converter. Herein, the input current ripple is removed by interleaving two inductors at the input side and voltage gain is increased by using switched-capacitor multiplier at the output. A small inductor is used to limit the peak current due to switching process which minimizes the current spikes in the circuit. Feedback control is used to control the duty ratio of the switches make the output voltage constant in spite of variation in the input or load or both i.e. to provide both line and load regulation.

## 2. Converter Circuit and Operation

### 2.1. Description of the Converter Circuit

The circuit diagram of the converter is shown in Figure 1. The high gain boost converter consists of two switches S1 and S2, three diodes D1, D2 and D3, three capacitors C1, C2, C3 and C4, and two inductors L1 and L2 and a small inductor L3 to limit peak current. L3 is chosen very small typically 50 times smaller than L1.

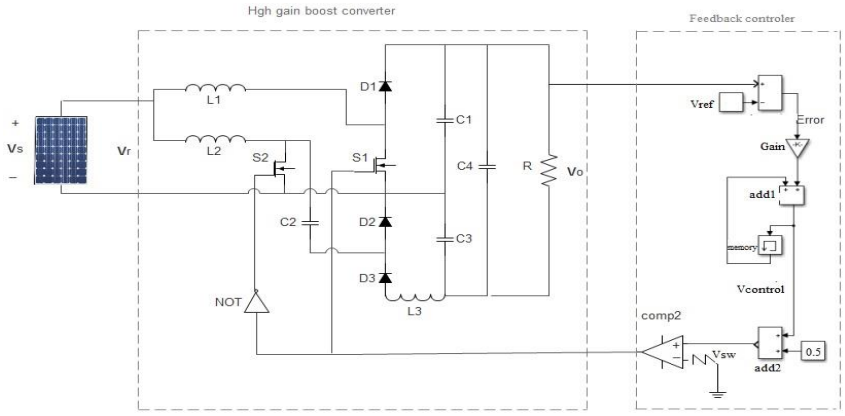


Figure 1. transformerless high gain boost converter with feedback controller

### 2.2. Principle of Operation

In order to illustrate the operation of the converter, several assumptions are made:

1) All switches are ideal.
2) The two inductors L1 and L2are large enough to be consideredas a constant current source during a switching period.
3) The output capacitor $C_4$ is large enough to be considered as a constant voltage source of Vin/( D * (1 – D)).
4) All the switches are MOSFETs with parasitic diodes.

The two switches S1 and S2 are complementarily, i.e. when S1 is ONN, S2 is OFF and when S2 is ONN, S1 is OFF. The switching time is Ts, and D is the duty ratio for S2. Therefore S2 is conducting for a period DTs and S1 for (1 – D)Ts.

**Mode 1**: When the switch S1 is on i.e. during (1 – DTs) period, the equivalent circuit is shown in Figure 2. Inductor L1 starts charging with negative polarity at diode D1 thus reverse biasing the diode D1 and blocking voltage across capacitor C1. Current through L1 rises with a slope $V_{IN}$/L1. Also diode D3 is reverse biased blocking voltage across C3. Since the switch S2 is open, L2 forces the diode D2 to turn on. Current through L2 discharges at the rate ($V_{IN}$ - $V_{C2}$)/L2 charging capacitor C2.

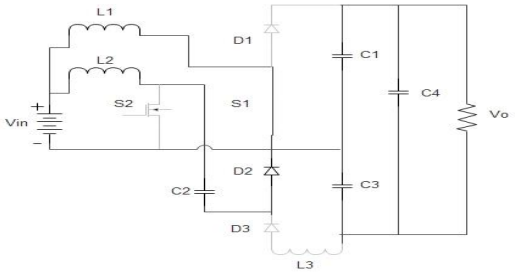


Figure 2. Equivalent circuit when S1 is conducting

**Mode 2:** When S2 is ON (and S1 is OFF) during DTs period, the equivalent circuit is shown in Figure. During this period, L1 forces diode D1 and D3 to turn on. Current through L1 discharges at the rate ($V_{IN}$ - $V_{C1}$)/L1 charging capacitor C1. While S2 is conducting D2 is turned off, inductor L2 stores energy and current through L2 rises with a slope $V_{IN}$/L2 since S2 is ON.During this period, capacitor C2 and C3 are connected in parallel forming a switched capacitor type circuit. Therefore L3 is used to limit the peak current in the circuit.

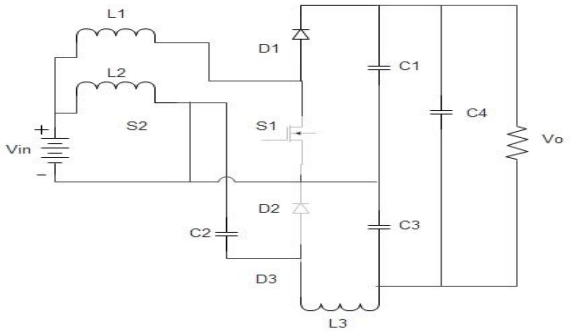


Figure 3. Equivalent circuit when S2 is conducting

Clearly, from the operation of the converter topology, the input current is sum of currentsthrough L1 and L2. Since L1 and L2 charge and discharge complimentary, the size of the inductors are chosen such that the input current is ripple free at a selected duty cycle.

When the load is connected to the converter, the output voltage also varies with the change in the load. Hence feedback is provided to maintain constant voltage across the load in spite of variation in load.

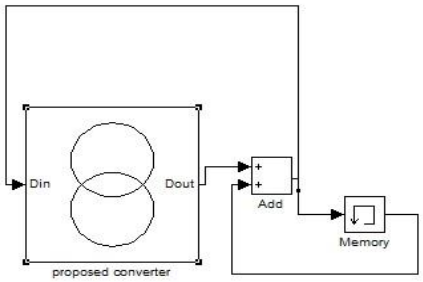


Figure 4. SimCoupler control loop model

The Feedback is given to the Psim model of the converter as shown in Figure 5.

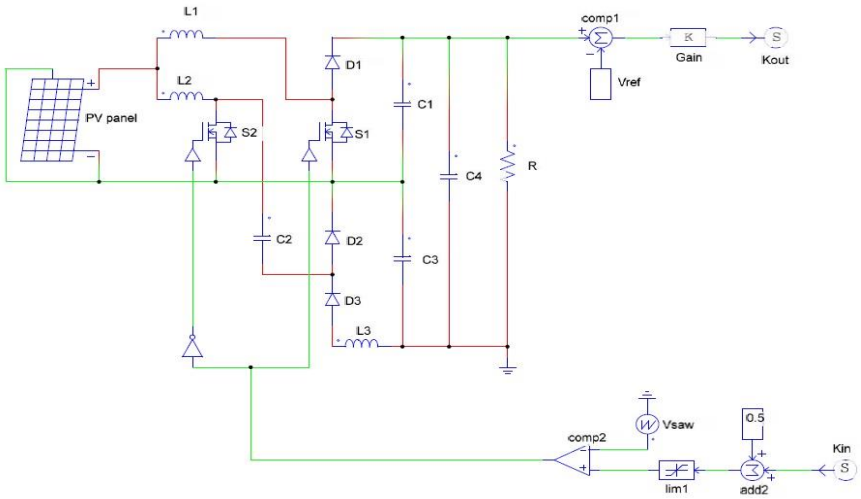


Figure 5. PSIM model of the converter

**Feedback controller:** The output voltage is compared with a reference voltage, by comp1 and the error is multiplied with a gain and it is given to the outlink of PSIM model, Kout. In the MatLab, Simcoupler function is used to integrate the PSIM model with Simulink model. The error received from outlink of PSIM model, Kout is given to the sum block add1. The other input to the add1 is its previous value from the memory block memory1 which is zero initially. The sum of add1, Vcontrol is given to the inlink, Kin of the PSIM model which is fed to the sumblock add2. The other input to add2 is a constant value 0.5. The output of add2 is given to non-inverting terminal of the comparator comp2 after passing through the limiter lim1. To the inverting terminal of the comparator a reference saw-tooth voltage is given. Upon comparing the two signals the comparator generates a unity magnitude voltage pulse whenever the input at non-inverting terminal is higher than inverting terminal. This voltage pulse is given to the switch S1 directly and the inverted pulse is given to switch S2.

Thus the duty cycle of the switches is controlled to provide output voltage regulation if the output voltage changes due to variation in load or line.

### 2.3. Design and Analysis

For the analysis, converter's duty ratio d(t) is defined as percentage of time over the switching period that switch S2 is closed,

$$d(t) = \frac{1}{Ts}\int_{t}^{t+Ts} q2(\tau)d \quad (2)$$

Ts – switching period

q2 switching function - is equal to one when S2 is closed and zero when S2 is open.

Voltage across L1 and L2, neglecting ESR is given by:

$$L1\frac{diL1}{dt} = d(vin - vc1) + (1-d)vin \quad (3)$$

$$L2\frac{diL2}{dt} = d(vin) + (1-d)(vin - vc2) \quad (4)$$

Under steady state average voltage across inductor is zero.

Equating LHS of (3) and (4) to zero.

$$Vc1 = \frac{1}{D}Vin \quad (5)$$

$$Vc2 = \frac{1}{(1-D)}Vin \quad (6)$$

Clearly from the above equations, Vc1 and Vc2 are proportional to each other,

$$Vc1 = \frac{1-D}{D} Vc2 \quad (7)$$

$$Vc2 = \frac{D}{(1-D)} Vc1 \quad (8)$$

Current through capacitor C1 is given by:

$$C1 \frac{dvc1}{dt} = diL1 - (\frac{vc1+vc3}{R}) \quad (9)$$

In steady state, average current through capacitor is zero. Equating LHS of 9 to zero, we get:

$$IL1 = \frac{1}{D}\left(\frac{vc1+vc3}{R}\right) \quad (10)$$

Since C2 and C3 form an switched capacitor type circuit, therefore average dynamics is not be applied. Average Current through L2 is calculated by considering input-output power balance.

$$IL2 = \frac{1}{(1-D)}\left(\frac{vc1+vc3}{R}\right) \quad (11)$$

Since C2 and C3 form an switched capacitor type circuit C2 clamps the voltage across C3, and both feature same voltage.

$$Vc2 = Vc3 \quad (12)$$

The output voltage is:

$$Vo = Vc1 + Vc3 \quad (13)$$

Substituting (5), (6) and (12) in (13) we get:

$$\frac{Vo}{Vin} = \frac{1}{D(1-D)} \quad (14)$$

Substituting (7) and (8) in (10) and (11), IL1 and IL2 can be given by:

$$IL1 = (1 + \frac{D}{1-D}) \frac{1}{D} \frac{Vc1}{R} = \frac{1}{D(1-D)}) \frac{Vc1}{R} \quad (15)$$

$$IL2 = (1 + \frac{1-D}{D}) \frac{1}{1-D} \frac{Vc2}{R} = \frac{1}{D(1-D)}) \frac{Vc2}{R} \quad (16)$$

The voltage gain for various values of duty cycle has been performed and is shown in Figure 6. Clearly from the graph, voltage gain is minimum at D=50% and increases as D varies from 50%.

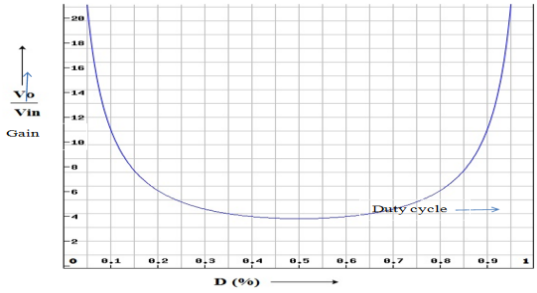


Figure 6. voltage gain vs duty cycle

### 2.3.1. Inductor L1 and L2 Sizing

When S1 is closed i.e. during (1 – D)Ts, voltage across L1 is equal to Vin.

$$VL1 = Vin$$
$$L1\ \frac{diL1}{dt} = Vin$$
$$\frac{\Delta iL1}{\Delta t} = \frac{Vin}{L1}$$
$$\Delta iL1 = \frac{Vin}{L1}(1 - D)Ts \quad (17)$$

When S2 is closed i.e. during (DTs), voltage across L2 is equal to Vin.

$$VL2 = Vin$$
$$L2\ \frac{diL2}{dt} = Vin$$
$$\frac{\Delta iL2}{\Delta t} = \frac{Vin}{L2}$$
$$\Delta iL2 = \frac{Vin}{L2} D\ Ts \quad (18)$$

The input current ripple is the difference between the two inductors current ripple.

$$\Delta i\ in = \frac{Vin}{Fs}\left(\frac{D}{L2} - \frac{(1-D)}{L1}\right) \quad (19)$$

The input current ripple can be eliminated by making LHS of (19) to zero, we get:

$$L2 = L1\frac{D}{1-D} \quad (20)$$

### 2.3.2. Peak Current Limiting Inductor L3 Sizing

When S1 is open, D3 connects C2 and C3 in parallel, hence a inductor is needed to limit the current. The average current through diode is same as load current but shape may be undesirable, hence it has to be controlled. When S2 is closed C2 and C3 are connected in parallel and both will have same voltage. Let this be Vc.0. when S2 is opened for (1 – D)Ts period, they are no longer connected and C3 discharges following the load current and C2 charges following current through L2. Let final voltages across C2 and C3 be Vc2.1 and Vc3.1 can be expressed as:

$$Vc2.1 = Vc.0 + Vc2 = Vc.0 + \frac{IL2}{C2}(1 - D)Ts \quad (21)$$

$$Vc3.1 = Vc.0 - Vc3 = Vc.0 - \frac{Io}{C3}(1 - D)Ts \quad (22)$$

At the end of (1 – D)Ts, the voltage difference between C2 and C3 is given by:

$$Vdiff = \Delta vc2 + \Delta vc3 = \left(\frac{IL2}{C2} + \frac{Io}{C3}\right)(1 - D)Ts \quad (23)$$

In the absence of peak limiting inductor in series with D3, peak current would be Vdiff over resistance in the loop, on state resistance of S2 and D3 and ESR of C2 and C3. This has been shown in Figure 7(a).

This may lead to high current that rises above the peak current limit and may destroy the other devices in the circuit. Hence L3 has to be introduced with proper design. Ceq is capacitance of series C2 and C3. Since L3 is very small it charges and discharges completely in a switching cycle limiting the peak current as shown in Figure 7 (b). It generates peak resonant at a frequency fo given by:

$$fo = \frac{\omega o}{2\pi} = \frac{1}{2\pi\sqrt{(L3Ceq)}} \quad (24)$$

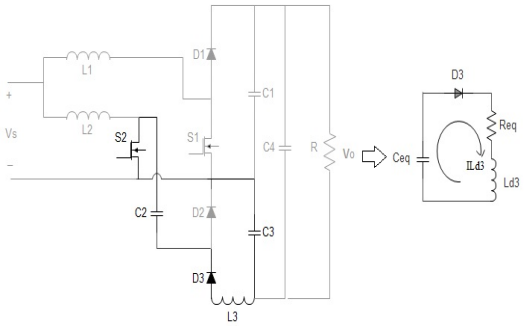


Figure 7(a). Equivalent circuit

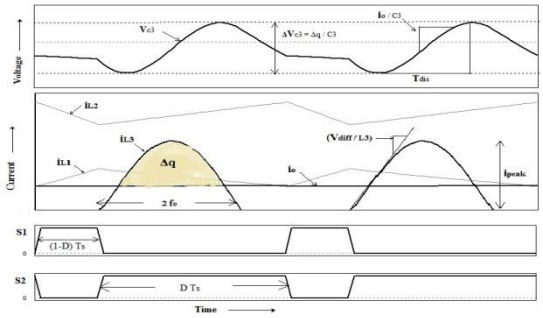


Figure 7(b). Waveform for reactive components

The converter operates at a duty cycle D> 50%, hence L3 should be selected such that fo>Fs. Fs – switching frequency

The peak current through L3 is given by:

$$\text{iL3} = \frac{Vdiff}{\omega o\ Ld3} \tag{25}$$

### 2.3.3. Capacitor:

When S1 is closed, current through C1 follows load current, therefore

$$\Delta vc1 = \frac{Io}{C1}(1 - D)Ts \tag{26}$$

When S1 is closed, C2 charges following current through L2, therefore

$$\Delta Vc2 = \frac{IL2}{C2}(1 - D)Ts \tag{27}$$

When the current through L3 rises above load current then C3 starts charging with increased voltage $\Delta Vc3$ given by $\Delta q/c3$. The time while C3 is charging is the time when io <iL3(t). C3 discharges through the remaining time of the switching period, therefore:

$$Tdis = Ts - (\frac{1}{2fo} - \frac{2}{\omega o} arcsin\left(\frac{io}{iL3}\right) \tag{28}$$

Tdis – time in which C3 discharges. During this period, C3 follows load current hence:

$$\Delta vc3 = \frac{Io}{C3} Tdis \tag{29}$$

## 3. Results and Analysis

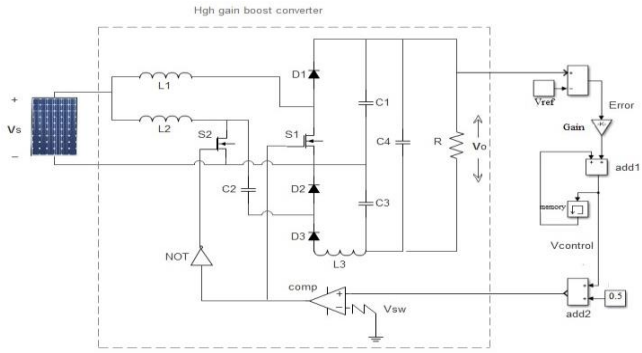


Figure 8. Psim model of the high gain boost converter with feedback controller

The Psim model of the converter integrated with Matlab Simulink control loop is shown in Figure 8. The simulation of the Model using Matlab 2008 and Psim 9.1 is discussed in this chapter in various sections.

The converter is simulated for a period of 0.2 second with the following parameter values.

Table 1. Simulation Parameters

| Parameter | Value |
|---|---|
| PV panel | 30W, Vos=21V, Vpm=17.5, Isc=2.1A, Ipm = 1.77A |
| Duty cycle, D | 82.5% |
| L1, L2 | 1000uH |
| L3 | 25uH |
| C1, C2 & C3 | 10 uF |
| C4 | 100uF |
| Fs | 10 kHz |

The duty cycle, D is chosen 50%, and L1 is selected 1000uH, from (20), we get L2 = 1000uH

The peak limiting inductor L3 is very small. Therefore L3 = 25uH is selected.

a) For 50Ω load

A resistive load of 50Ω is connected at the output capacitor c4 and the input voltage measured is shown in Figure 9. The gate signal to MOSFET switches is shown in Figure 10.

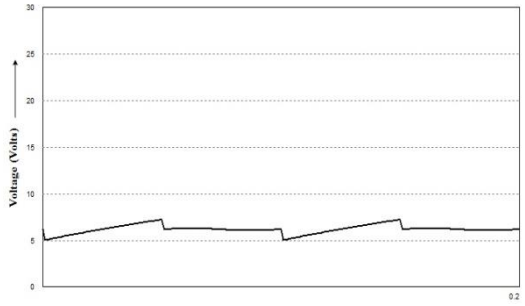


Figure 9. Input voltage, Vin

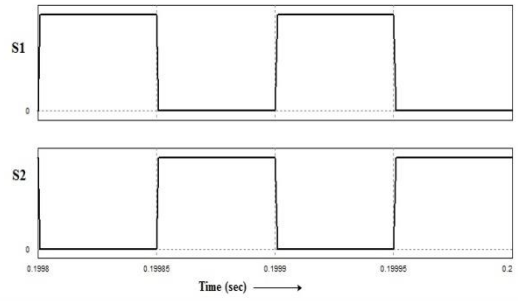


Figure 10. Pulse signals to MOSFET switches

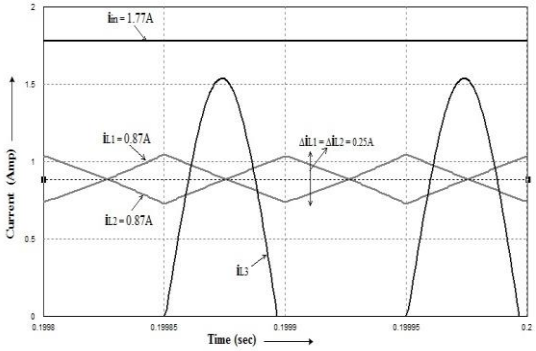


Figure 11. Various current waveforms

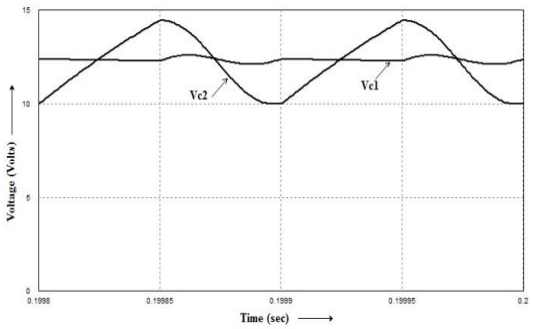


Figure 13. Voltage across capacitors

The input current corresponds to the sum of current through L1 and L2. The inductors are selected such that both inductors are charged with same voltage. Since L1 and L2 charge/discharge in a complementary manner, the input current is ripple free as shown in Figure 11. A small inductor L3 is used to limit the peak current when C2 and C3 are connected in parallel. The waveforms for input current and current through L1, L2 and L3 is shown in Figure 11. The waveforms for voltage across capacitor C1 and C2 is shown in Figure 12.

The output voltage Vo given by (19) is sum of voltage across C1 and C3, is shown in Figure 14(a). Vo is measured to be 24V.A output filter capacitor C4 = 100 uF, is used to remove the ripples from the output voltage.

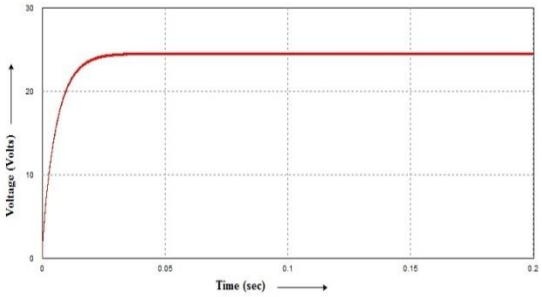


Figure 14(a). Output voltage

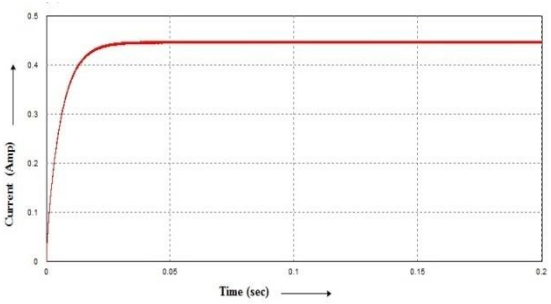


Figure 14(b). Load current

A resistive load R = 50 Ω is connected across capacitor C4. Current drawn by the load is shown in Figure 14(b). With the feedback, R can be varied between 10 to 70. If the output voltage falls or rises above the required reference value then the duty cycle is controlled using the feedback to the converter so that output voltage remains constant at 24V.

The resistive load is now changed to 5Ω, the feedback controller adjusts the duty ratio of the controller to maintain constant voltage across the load. The duty ratio of the MOSFET switches is shown in Figure 15(a) and the output voltage is shown in Figure 15(b).

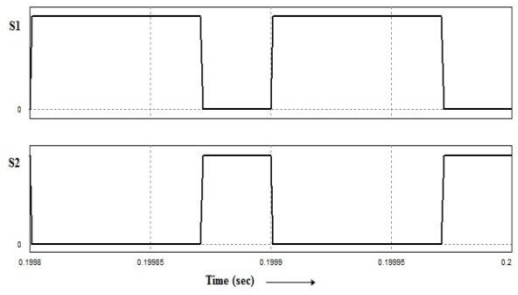


Figure 15(a). Pulse signals to MOSFET switches for 5Ω load

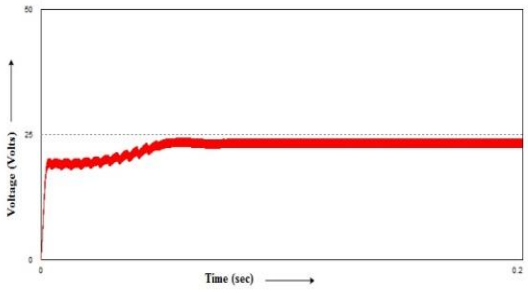


Figure15(b). Output voltage for 5Ω load

Thus the feedback controller controls the duty ratio of the switches to maintain constant output voltage.

### 3.1. Applications

1) Can be ssed in street LED lightening, 18-24V.
2) Can be used in SMPS power supplies for Desktop, LED TV, LCD displays.
3) Can be used in Industrial control and Process control instrument set up.

### 3.1.1. Hardware Model of the Converter

A picture of the prototype developed is shown in Figure 16.

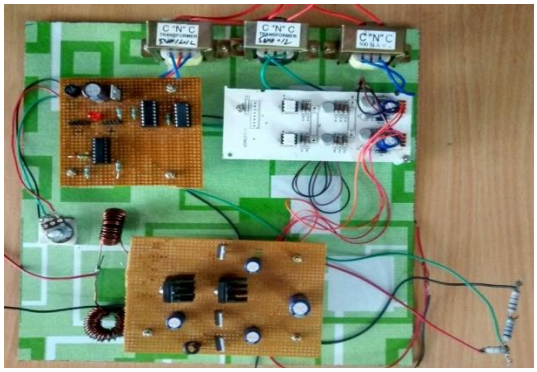

Figure 16. Developed prototype

The variables and parameters during the experiment tests are, 30W solar panel, Vos=18V, Vpm = 17.5V, Isc=2.1A, Ipm=1.7A, L1= L2=100mH, L3=10mH, C1=C2=C3=10uF, C4=100uF, fs=10kHz, D=50%. The output voltage and the gate signals are measured in the CRO and are shown in the pictures below. We can see from the pictures below that the duty cycle of the switches is controlled to maintain constant voltage of 18V across the load. The output voltage and MOSFET gate signals are measured using a Digital CRO.

Y-axis (Output voltage)

1 division = 20v

*X – axis (Time)*

### 3.1.2. For Resistive Load of 100 Ω

The gate signal to MOSFET switches for 100Ω load is shown in Figure 17 and the output voltage is shown in Figure 18, Vo is 18v.

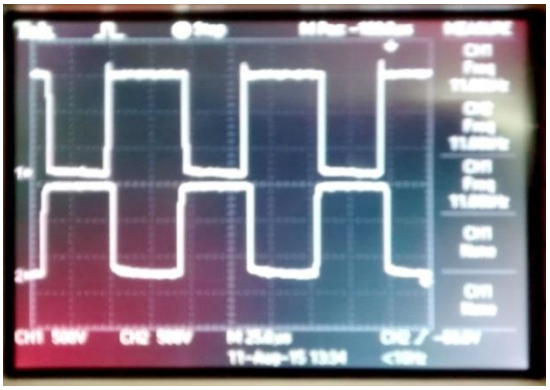

Figure 17. Gate pulse at S1 and S2 for 100Ω

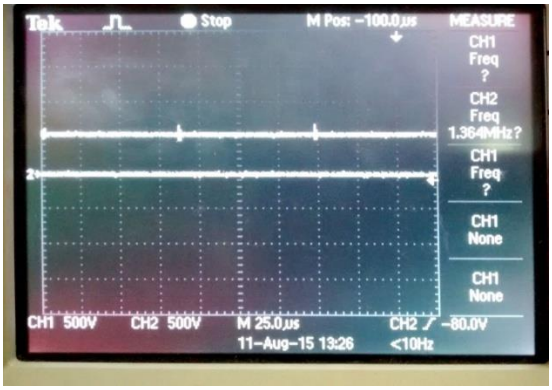


Figure 18. Output voltage for 100Ω

### 3.1.3. For Resistive Load of 50Ω

If the voltage changes due to change in load then the duty ratio is controller to maintain constant output voltage. Gate signals for S1 and S2 for 50Ω resistive load is shown in Figure 19 and the output voltge is shown in Figure 20, Vo is 17v

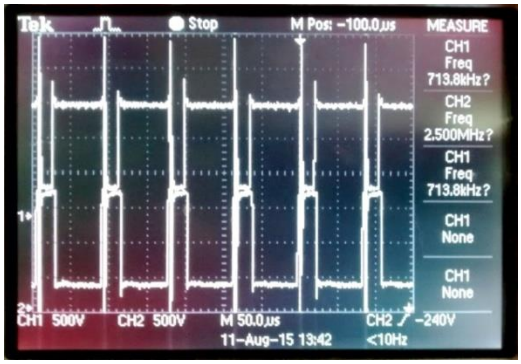


Figure 19. Gate pulses at S1 and S2 50 Ω resistive load

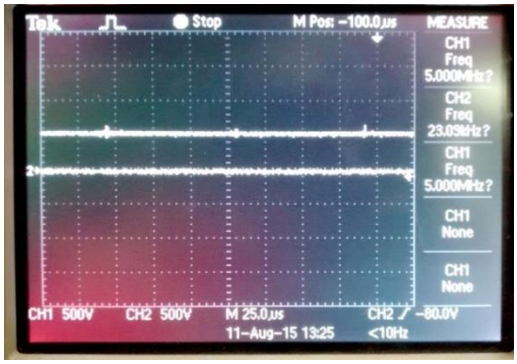


Figure 20. Output voltage for 50Ω resistive load

## 4. Conclusion

The converter uses solar energy as input and achieves a high voltage gain without utilizing extreme duty cycle. Also the converter is able to remove the input current ripple at a preselected duty cycle. Furthermore with the feedback, the converter is able to maintain constant output voltage if the output voltage changes due to change in the load i.e. load regulation. Also in this converter, smaller reactive components are used which has more advantages compared to the use of transformers.

The converter is able to achieve zero ripples in the input current at a preselected duty cycle; it can be improved by designing optimal size of the inductors for a wide range of duty cycle. Also load can be changed from resistive to inductiveload. The closed loop controller can be changed to fuzzy logic controller, neural network controller, DSPcontrollers etc.

## References

[1] B Axelrod, Y Berkovich, A Ioinovici. Switched capacitor/ switched-inductor structures for getting transformerless hybrid DC–DC PWM converters. *IEEE Trans. Circuits Syst. I, Reg. Papers*. 2008; 55(2): 687-696.

[2] YP Hsieh, JF Chen, TJ. Liang, LS Yang. Novel high step-up DC–DC converter for distributed generation system. *IEEE Trans. Ind.Electron.* 2013; 60(4): 1473-1482.

[3] SM Chen, TJ Liang, LS Yang, JF Chen. A cascaded high step-up DC–DC converter with single switch for microsource applications. *IEEE Trans. Power Electron.* 2011; 26(4): 1146-1153.

[4] BR Lin, JY Dong, JJ Chen. Analysis and implementation of a ZVS/ZCS DC–DC switching converter with voltage step-up. *IEEETrans. Ind. Electron.* 2011; 58(7): 2962-2971.

[5] TJ Changchien, SK Liang, JF Chen, LS Yang. Step-up DC–DC converter by coupled inductor and voltage-lift technique. *IET Power Electron.* 2010; 3(3): 369-378.

[6] Y Berkovich, B Axelrod. Switched-coupled inductor cell for DC–DC converters with very large conversion ratio. *IET Power Electron.* 2011; 4(3): 309-315.

[7] TJ Liang, SM Chen, LS Yang, JF Chen, A Ioinovici. *A single switch boost-flyback DC–DC converter integrated with switchedcapacitor cell.* In Proc. 8th Int. Conf. Power Electron. ECCE Asia. 2011: 2782-2787.

[8] YP Hsieh, JF Chen, TJ Liang, LS Yang. Novel high step-up DC–DC converter with coupled-inductor and switched-capacitor techniques. *IEEE Trans. Ind. Electron.* 2012; 59(2): 998-1007.

[9] KB Park, GW Moon, MJ Youn. Non-isolated high step-up stacked converter based on boost-integrated isolated converter. *IEEETrans. Power Electron.* 2011; 26(2): 577-587.

[10] Amir Mahmood Soomro, Xulingyu, Shahnawaz Farhan Khahro, Liao Xiaozhong. High Output Voltage Based Multiphase Step-Up DC-DC Converter Topology with voltage doubler rectifiers. *TELKOMNIKA Indonesian Journal of Electrical Engineering.* 2013; 11(2): 1063-1068.

[11] Nivetha V, G Vijaya Gowri, Elamathy A. An Advanced High Performance Maximum Power Point Tracking Method with Ant Colony and Particle Swarm Optimization Method Using Interleaved Boost Converter.*TELKOMNIKA Indonesian Journal ofElectrical Engineering*. 2015; 14(3): 376-380.

[12] SC Tan, S Bronstein, M Nur, YM Lai, A Ioinovici, CK Tse. Variable structure modeling and design of switched-capacitor converters. *IEEE Trans. Circuits Syst. I, Reg. Papers*. 2009; 56(9): 2132-2142.

[13] SC Tan, S Kiratipongvoot, S Bronstein, A Ioinovici, YM Lai, CK Tse. Adaptive mixed on-time and switching frequency control of a system of interleaved switched-capacitor converters. *IEEE Trans. PowerElectron.* 2011; 26(2): 364-380.
[14] AA Fardoun, EH Ismail. Ultra step-up DC–DC converter with reduced switch stress. *IEEE Trans. Ind. Appl.* 2010; 46(5): 2025-2034.
[15] S Choi, VG Agelidis, J Yang, D Coutellier, P Marabeas. Analysis, design and experimental results of a floating-output interleaved-input boost-derived DC–DC high-gain transformer-less converter. *IET Power Electron.* 2011; 4(1): 168-180.
[16] B Axelrod, Y Berkovich, S Tapuchi, A Ioinovici. Single-stage single-switch switched-capacitor buck/buck-boost-type converter. *IEEETrans. Aerosp.Electron. Syst.* 2009; 45(2): 419-430.
[17] D Gu, D Czarkowski, A Ioinovici. *A large DC-gain highly efficient hybrid switched-capacitor-boost converter for renewable energy systems*. In Proc. IEEE Energy Convers. Congr.Expo. ECCE. 2011: 2495-2500.
[18] S Ben-Yaakov. Behavioral average modeling and equivalent circuit simulation of switched capacitors converters. *IEEE Trans. Power Electron.* 2012; 27(2): 632-636.
[19] Alireza Kaviani-Arani, Alireza Gheiratmand. Soft Switching Boost Converter Solution for Increase the Efficiency of Solar Energy Systems. *TELKOMNIKA Indonesian Journal of Electrical Engineering*. 2015; 13(3): 449-457.