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A 45 nm 6 Bit Low Power Current Steering Digital to Analog Converter Using GDI Logic

Bharat H. Nagpara
C.U.Shah College of Engineering and Technology, Wadhwancity, Gujarat, India
E-mail: bharatnagpara83@gmail.com

Abstract

In this paper, the design and implementation low power current steering digital to analog converter in 45 nm technology using GDI Logic using TANNER TOOL V15 is presented. This architecture gives the most optimized results in terms of speed, resolution and power. The designed 6-bit DAC operates with two supply voltages, 1 V and 3.3 V. The simulation result shows the transient analysis waveforms of current steering DAC. The average power dissipation is 364.06 µW. The tool used for simulation is Tanner S-Edit and T-Spice. Comparisons show that using GDI logic consists low power as compare to the CMOS logic.

Keywords: *CMOS, current-source, TANNER TOOL*

1. Introduction

GDI Logic in CMOS technologies has been used for low power applications; also submicron processes have allowed CMOS to achieve low power. In a wireless system the quality of the communication link is main criteria, for long distance transmission it is necessary to convert analog signal into digital signal at input side, same as convert digital signal into analog signal at output side. In this paper current steering DAC using 45nm technology are presented. CMOS technology dissipates less power compare to other design. CMOS architecture can be easily scaled down for the major three factors: 1) Area 2) Speed 3) Power [1].

Energy performance requirements are forcing designers of next-generation systems to explore approaches to lease possible power consumption. Power consumption is majorly affected by power supply voltage. Scaling of power supply voltage is major factor to reduce power Consumption. The technique to achieve ultra-low power is to operate the circuit with supply voltage less than threshold voltage. The region where supply voltage is less than threshold voltage is called sub threshold region. Ultra-low power consumption can be achieved by operating digital circuits at sub threshold region. Here proposed sub threshold circuit is based on GDI (Gate Diffusion Input) technique. GDI technique allows reducing power consumption, delay, area of the digital circuit while maintaining low complexity of logic design as compared to other CMOS (Complementary Metal Oxide Semiconductor) circuits [2].

Scaling of power supply voltage is major factor to reduce the power consumption. Sub threshold operation has gained a lot of attention due to ultralow-power consumption applications requiring low to medium performance. It has also been shown that by optimizing the device structure, power consumption of digital sub threshold logic can be further minimized while improving its performance.

To accomplish this task circuit with lower frequency should be operated in the weak inversion region or sub threshold region. Sub threshold circuits are very sensitive to process variations and temperature fluctuation. These, and other factors, have to be taken into consideration when designing circuits for sub threshold operation.

The architectural technique described in this paper suggests a design to minimize area and capacitance by using Gate Diffusion Input (GDI) multiplexer. As feature size of the CMOS (Complementary Metal Oxide Semiconductor) technology continues to scale down, leakage power has become an ever-increasing important part of the total power consumption of a chip.

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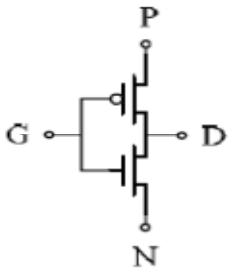

Figure 1. GDI Basic Cell [4]

The GDI method is based on the simple cell shown in Figure 1. A basic GDI cell contains four terminals - G (the common gate input of the nMOS and pMOS transistors), P (the outer diffusion node of the pMOS transistor), N (the outer diffusion node of the nMOS transistor) and the D node (the common diffusion of both transistors). P, N and D may be used as either input or output ports, depending on the circuit structure. Simpler gates, lower transistor count, and lower power dissipation in many implementations, as compared with standard CMOS and PTL design techniques. Multiple-input gates can be implemented by combining several GDI cells. The buffering constraints, due to possible VTH drop, are described in detail in, as well as technological compatibility with CMOS and SOI [2].

Table 1. Some logic functions that can be implemented with a single GDI cell [4]

N	P	G	D	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

2. DAC Architecture

The Segmented Current- Steering architecture is shown in Figure 2. The architecture is a combination of two parts, the MSB is going through the thermometer coded architecture and the LSB is going through the Binary Weighted architecture. The input n-digital codes are sent into buffer to get enough amplitude and synchronized with the clock. Then the (N-B) bits MSBs are decoded by thermometer decoder to reduce the glitch and achieve well matching of current sources. The B Bits LSB is given to the LSB Delay. The signal after decoding will be controlled by latch to put into current switch array or not, which decides the output current direction [3-4].

The binary weighted architecture is very simple, but less accurate. The thermometer coded architecture is very accurate, but the circuit complexity is very high, and is comparatively slow.

The 3-bit LSB are implemented using binary weighted architecture, thus requires only three current sources. The 3-bit MSB is implemented using thermometer coded architecture, which requires 7 current sources. So, total 10 current sources are needed to implement 6-bit DAC, which is quite low as compared to fully thermometer coded architecture. The binary weighted current source is also similar, but to compensate the delay of row-column decoder in thermometer coded current sources, the dummy combination logic is provided, which ensures that the digital input in both binary weighted and thermometer coded current source reaches at the switches at the same instant.

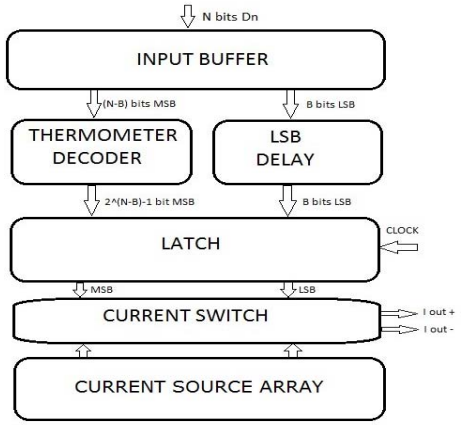

Figure 2. Segmented Current Steering Digital to Analog Converter

The main building blocks in this prototype are the unit current cells, Latches and the thermometer decoder design.

3. Cascode Current Source with Thick Oxide Layer Cascoded Switches

The current cell configuration used here is a thick oxide layer transistor for the switch Cascode [5]. The low voltage headroom problem in 45-nm technology can be solved using a thick oxide layer transistor for the switch cascade [5]. This thick oxide layer transistor can operate with a higher supply voltage up to 3.3 V. Hence the voltage headroom is increased significantly. Care should be taken to prevent the voltage at the drain of the switching transistors from increasing beyond the maximum supply voltage in 45-nm technology i.e. beyond 1 V. Methods used to keep the voltage at the drain of the switching transistor below 1 V are explained below. The drain voltage of the switching transistor can be held constant by using a voltage regulator. The voltage regulator (Zener diode) is connected in parallel such that the voltage at the drain remains below 1 V, but its unknown leakage current flows through the output of the DAC. The output current of the current steering DAC should be proportional to the input code [5].

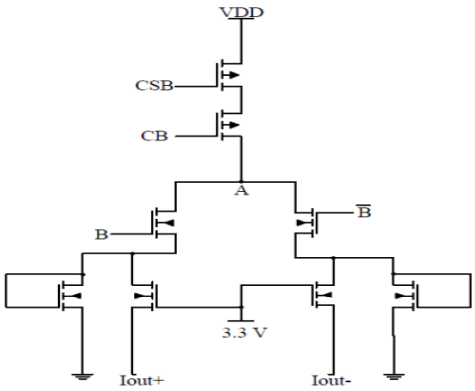

Figure 3. Cascode Current Source with Thick Oxide Layer Cascoded Switches [5]

A novel implementation of a GDI DFF is shown in Figure 4. It is based on the Master-Slave connection of two GDI D-Latches. Each latch consists of four basic GDI cells, resulting in a simple eight-transistor structure. The components of the circuit can be divided into two main categories:

(a) *Body gates* – responsible for the state of the circuit.

These gates are controlled by the Clk signal and create two alternative paths: one for transparent state of the latch (when the Clk is low and the signals are propagating through PMOS transistors), and another for the holding state of the latch (when the Clk is high and internal values are maintained due to conduction of the NMOS transistors).

(b) *Inverters* (marked by ×) – responsible for maintaining the complementary values of the internal signals and the circuit outputs. An additional important role of inverters is buffering of the internal signals for swing restoration and improved driving abilities of the outputs.

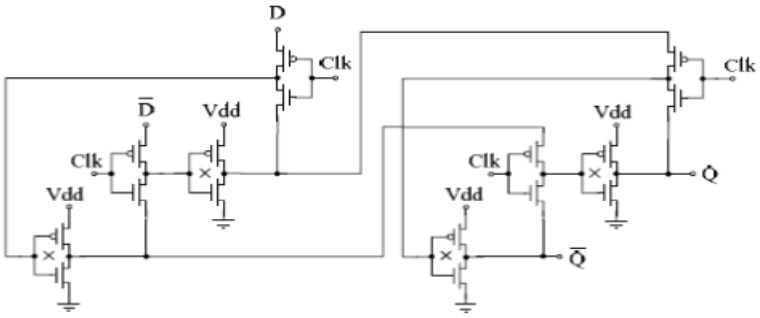

Figure 4. GDI D-Flip-Flop implementation

This partition to categories can be helpful for understanding of circuit operation and optimization. As can be seen, in body gates the transmission of the signal is performed through the diffusion nodes of the GDI cells. It might cause a swing drop of VTH in the output signals. This problem is solved by the internal inverters in their buffer role. Performance optimization of the proposed circuit can be performed by adjusting the transistor sizes (as sweep parameter in simulation) to obtain a minimal power delay product. This procedure is iterative and contains a sequence of separate size adjustments:

(a) First, the same scaling factor is obtained for all transistors of the circuit (body gates and inverters).

(b) Secondly, iterative size optimizations are applied separately to inverters and body gates (mostly by opposite shifting of the scaling factors around the “operation point” found in (a)), while targeting the minimal power-delay product.

(c) For high load requirements, an additional optimization can be separately performed on the inverter of the Slave latch.

The relatively compact structure of the proposed DFF, containing 18 transistors (with the inverter for complementary value of D), makes it an efficient alternative for obtaining the combination of low area and high performance [6].

4. Binary-to-Thermometer Decoder

The Binary to thermometer decoder is used to convert N bit binary input into 2^N – 1 Thermometer coded output lines.

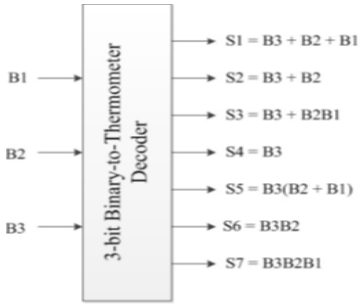

Figure 5. 3-bit Binary to Thermometer Decoder

In this implementation, 3 bits are converted into the 7 bit thermometer code. The 3 bit binary to 7 bit thermometer bit decoder are shown in figure. It requires two input and three input AND gate and OR gate for Implementation. This logic gates are Implemented using GDI Logic [7].

Figure 6 show the reconstructed sine wave of the segmented DAC and Figure 7 shows its FFT spectrum from Figure 7, the measured SFDR is 77 dB. The measured average power dissipation is 364.06 µW.

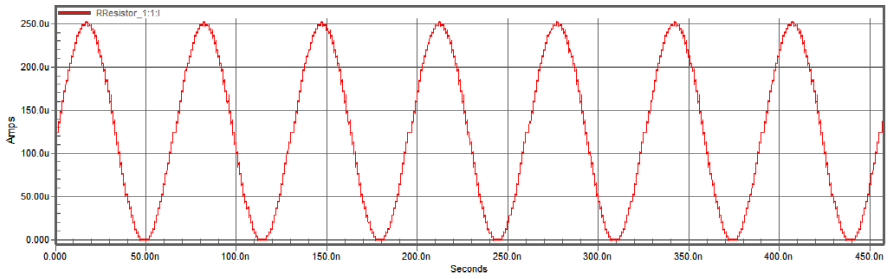

Figure 6: Sine Wave Output of 6-bit DAC

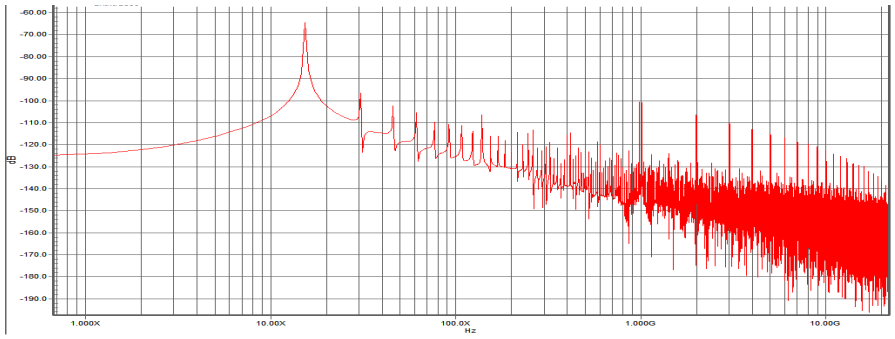

Figure 7. Fast Fourier Transform of Sine wave output of 6-bit DAC

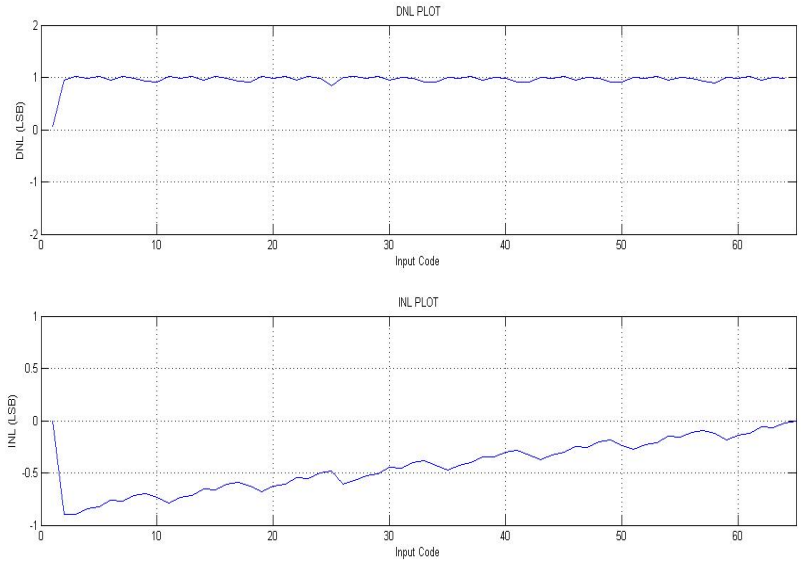

Figure 8. DNL & INL Plots of 6-bit DAC

The measured response time is 672 ps and settling time is 72 ps. Figure 8 shows the DNL and INL plots. As shown, the measured DNL and INL are 1.0 LSB and 0.8 LSB, respectively, which is quite acceptable in terms of monotonicity condition. Table 2 summarizes and compares the simulation results of 6-bit segmented DAC with previous implementations. It shows that DAC is using GDI logic implementation Consume low power then the DAC using CMOS

Table 2. Summary and comparison of simulation results of 6-bit dac designs

Parameter	This Implementation (GDI LOGIC)	Chen *et al* [8]
Resolution	6 bit	6 bit
Technology	45 nm-GDI	90nm CMOS
DNL	1.0 LSB	0.05 LSB
INL	0.8 LSB	0.07 LSB
SFDR	77 dB	41.54 dB
Average power Consumption	364.06 uW	8.32mW
Supply Voltage	1 v & 3.3 v	1.2 v & 2.5 v
Response Time	672 ps	--
Settling Time	72 ps	--

5. Conclusion

This implemented DAC provides desired level of accuracy with very low power consumption. In any applications with the requirement of high speed and accuracy, this DAC can be used. Some Compromise with the DNL & INL then the CMOS is observed but using some special Current Calibration Technique it can be removed.

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