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A sub-1V high PSRR OpAmp based β-multiplier CMOS bandgap voltage reference with resistive division

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ABSTRACT

A sub-1V opamp based β-multiplier CMOS bandgap voltage reference (BGVR) with high power supply rejection ratio (PSRR) and low temperature coefficient (TC) is proposed in this paper. A current mode regulator scheme is inserted to isolate the supply voltage of the operational amplifier (opamp) and the supply voltage of the BGVR core from the supply voltage source in order to reduce ripple sensitivity and to achieve a high PSRR. The proposed circuit is designed and simulated in 0.18-μm standard CMOS technology. The proposed voltage reference delivers an output voltage of 634.6mV at 27°C. Tthe measurement temperature coefficient is 22,3ppm/°C over temperature range -40°C to 140°C, power supply rejection ratio is -93dB at 10kHz and -71dB at 1MHz and a line regulation of 104μV/V is achieved over supply voltage range 1.2V to 1.8V. The layout area of the proposed circuit is 0.0337mm2. The proposed sub-1V bandgap voltage reference can be used as an internal voltage reference in low power LDO regulators and switching regulators.

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1. INTRODUCTION

Many analog and mixed integrated circuits, such as low dropout (LDO) regulators [1], switching regulators [2], analog-to-digital converters, digital-to-analog converters, smart sensors and other precise industrial control systems require a fixed voltage reference to be compared to for the sake of reliability and accuracy. This voltage reference also called bandgap voltage reference is a circuit used to generate a fixed voltage, VREF, that is in theory independent of the power supply voltage VDD (where VREF<VDD), temperature and process variations. The classical design of BGVR circuits has commonly an output voltage VREF around 1.25V (close to the theoretical 1.17V bandgap voltage of silicon at 0 K) [3]-[6].

As the technology scales less than 350 nanometers, so do the supply voltages. Recently, the supply voltages tend to be in the range of 0.6V-1.2V. The supply voltage scales with the technology, but the threshold voltage of the transistors does not scale at the same rate. This makes it difficult to incorporate classical design of bandgap voltage reference to operate properly in the low supply voltages. For the low voltage bandgap reference design many approaches have been proposed; resistive divider networks [7-9], current summing and a voltage summing circuits [10], transimpedance amplifier [11], dynamic threshold mosfets [12] and other work [13].

Recent applications such as image sensors using LDO regulators require an accutare voltage refrence with very large PSRR value not only in the low frequencies but also in the high frequencies.

To achieve this performance, various works has been proposed [14-18], but the performances of these works are limited in terms of PSRR, especially in the high frequencies.

This work propose a novel technique to improve the value of PSRR of sub-1V bandgap voltage reference circuit which provides an output voltage reference VREF with low TC and high PSRR in wide frequency range compared with related works previously mentioned.

2. CONVENTIONAL SUB-1V BANDGAP VOLTAGE REFERENCE

The sub-1V bandgap voltage reference is an analog circuit that provides a stable output voltage less than 1V. This is achieved by adding a voltage, which is proportional to the absolute temperature (PTAT), to a base-emitter voltage of diode connected Bipolar Junction Transistor (BJT) NPN or PNP type which is a complementary to the absolute temperature (CTAT) in order to compensate for its first-order temperature dependency [19].

The conventional sub-1V bandgap voltage reference suitable for low power supply voltages is shown in Figure 1 [7]. He use an OpAmp based β-multiplier architecture with resistive division, where the operational amplifier (OpAmp) will form an inverted feedback loop to enforce the two input nodes X and Y of this OpAmp having the same voltages.

The current mirror is formed by the PMOS transistors M1, M2 and M3 having identical size, so that the currents flowing through this three transistors are the same. The β-multiplier consists of two diode connected NPN transistors Q1 and Q2, with their emitter area ratio being 1:K to provide the required temperature dependent voltage to make the voltage reference circuit.

The output voltage reference VREF is expressed as:

$$V_{REF} = \frac{R_3}{R_2}.(V_{BE_1} + \frac{R_2}{R_1} V_T \ln K + \frac{R_2}{R_1} V_{OS}) \quad (1)$$

Where, V_{BE_1} is the base-emitter voltage of BJT Q_1 witch has a negative temperature coefficient and represents the CTAT voltage, and V_T is the thermal voltage (V_T=25.9mV at 300K) expressed as :

$$V_T = \frac{k_B T}{q} \quad (2)$$

Where k_B is the Boltzmann's Constant ($k_B = 1.381\times10^{-23}$J.K^{-1}), q is the electron's charge ($q = 1.602\times10^{-19}$C) and T is the absolute temperature.

V_{OS} presents the input offset voltage of the OpAmp.

V_T has a positive temperature coefficient and represents the PTAT voltage. If we neglect the value of V_{OS}, the (1) becomes:

$$V_{REF} = \frac{R_3}{R_2}(V_{BE_1} + \frac{R_2}{R_1} V_T \ln K) \quad (3)$$

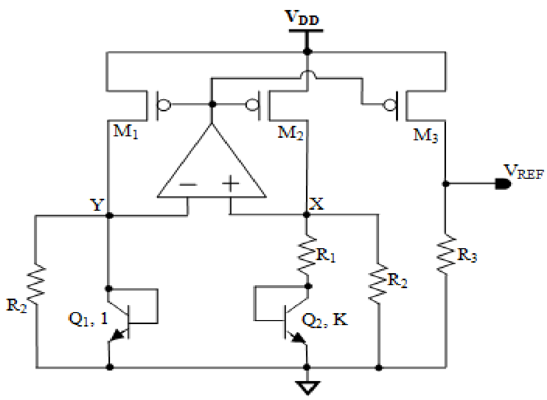

Figure 1. Schematic of Conventional sub-1V BGVR

The temperature behavior of the V_{REF} is:

$$\frac{\partial V_{REF}}{\partial T} = \frac{R_3}{R_2}\left[\frac{\partial V_{BE_1}}{\partial T} + \frac{R_2}{R_1}\ln K\left(\frac{\partial V_T}{\partial T}\right)\right] \tag{4}$$

A voltage reference independent of the absolute temperature is obtained if $\frac{\partial V_{REF}}{\partial T} = 0$, then:

$$\frac{R_2}{R_1}\ln K = -\frac{\partial V_{BE_1}/\partial T}{\partial V_T/\partial T} \tag{5}$$

Noted that $\frac{\partial V_{BE_1}}{\partial T} < 0$ and its value depends on the CMOS technology used and can be extracted by simulation, while $\frac{\partial V_T}{\partial T} > 0$ and it value can easily be calculated.

The conventional sub-1V BGVR using opamp β-multiplier architecture ensures a low temperature coefficient for V_{REF} but remains very limited in terms of PSRR caused by the input offset voltage problem of the opamp, although some modifications have been proposed to improve the PSRR.

3. PROPOSED SUB-1V BANDGAP VOLTAGE REFERENCE

The schematic of proposed sub-1V BGVR is shown in Figure 2. A current mode regulator scheme is inserted to isolate a supply voltage of the opamp and supply voltage of the BGVR core from a supply voltage source V_{DD} in order to reduce ripple sensitivity and to achieve a high PSRR.

The schematic of the opamp used is shown in Figure 3. A self biased cascode current mirror load is adopted to achieve a high gain [20]. This opamp needs a network compensation to achieve a sufficient phase margin in order to guarantee closed-loop stability. The supply voltage of the opamp is V_{REG} which is equal to regulate source-drain voltage of M_5. The proposed sub-1V BGVR needs a start-up circuit shown in Figure 4 to fix it at the proper operation point.

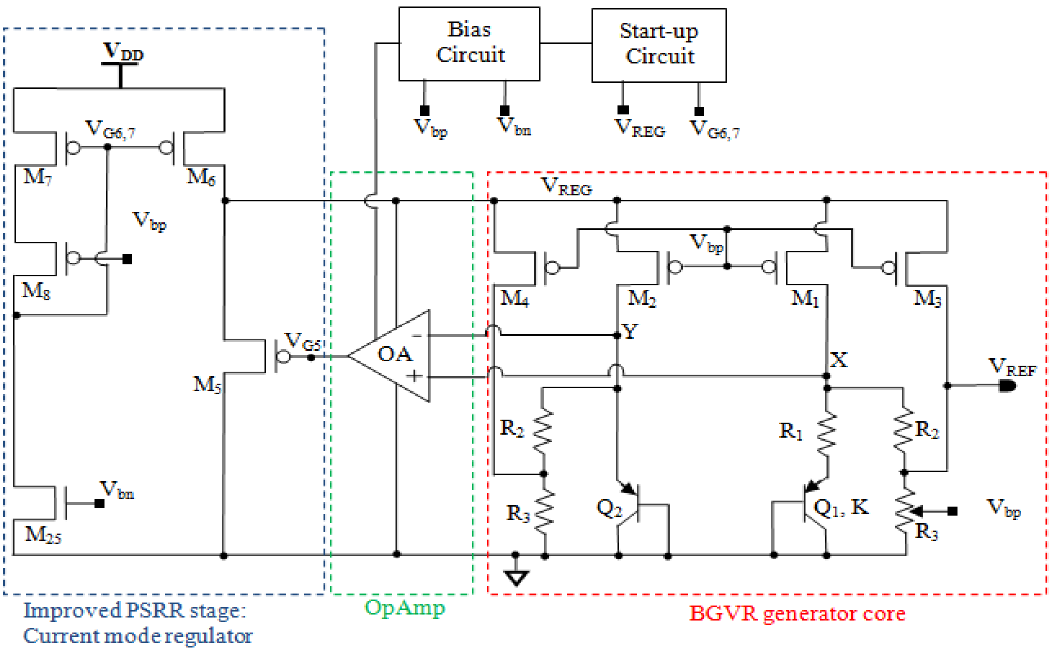

Figure 2. Schematic of proposed sub-1V BGVR

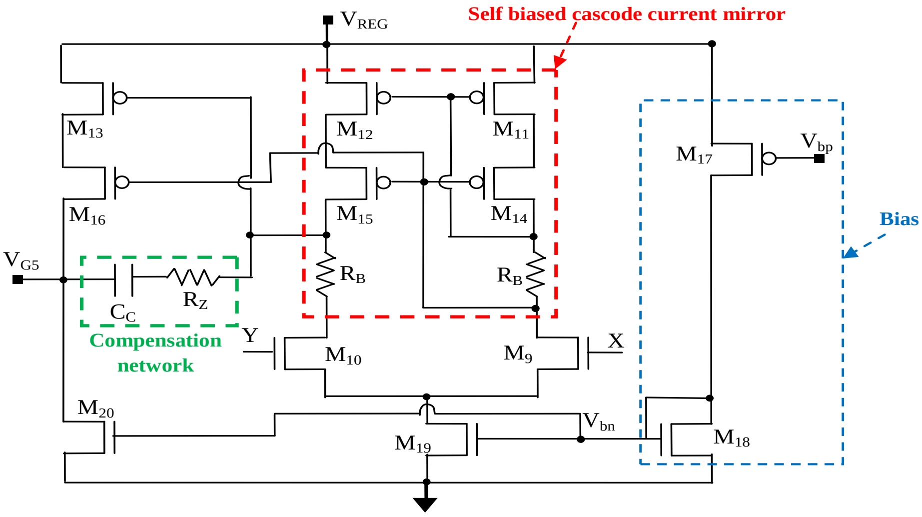

Figure 3. Schematic of opamp and his Bias circuit

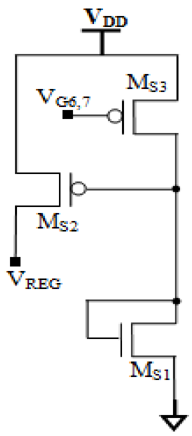

Figure 4. Schematic of start-up circuit

3.1. Analysis and Design of Proposed BGVR Core

The core of the proposed BGVR uses the same principle of the conventional scheme with some modifications on the resistive voltage divider in order to compensate the error introduced by the input offset voltage of the OpAmp and consequently to have the same voltage level in the X and Y nodes.

The PMOS transistors M1, M2, M3 and M4 have identical size, such that the currents flowing through this four transistors are the same as $I_{D_1} = I_{D_2} = I_{D_3} = I_D$. The β-multiplier consists of two diode connected PNP transistors Q1 and Q2, with their emitter area ratio being K:1 to provide the required temperature dependent voltage to construct the voltage reference circuit.

Let us establish the literal expression of the reference voltage VREF generated, we have:

$$V_{REF} = R_3 I_{R_3} \tag{6}$$

Where I_{R_3} is the current flowing through the resistor R3, it is expressed as:

$$I_{R_3} = I_{R_2} + I_D \tag{7}$$

Where I_{R_2} is the current flowing through the resistor R2, it is expressed as:

$$I_{R_2} = \frac{V_{R_2}}{R_2} \tag{8}$$

Where V_{R_2} is the voltage across the resistor R2.
We also have:

$$I_D = I_{R_1} + I_{R_2} \tag{9}$$

And,

$$R_1 I_{R_1} + V_{EB_1} = V_{EB_2} \tag{10}$$

Where V_{EB_2} is the base-emitter voltage of PNP transistor Q2, it is expressed as:

$$V_{EB_2} = V_T \ln\left(\frac{I_{C_2}}{I_{S_2}}\right) \tag{11}$$

Where I_{S_2} is the transport saturation current of Q_2, expressed as:

$$I_{S_2} = J_{S_2} A_{E_2} \tag{12}$$

Where J_{S_2} is the saturation current density of Q_2 and A_{E_2} is the emitter area of Q2 and V_{EB_1} is the base-emitter voltage of PNP transistor Q_1, expressed as:

$$V_{EB_1} = U_T . \ln\left(\frac{I_{C_1}}{I_{S_1}}\right) \tag{13}$$

Where I_{S_1} is the transport saturation current of Q_1, expressed as:

$$I_{S_1} = J_{S_1} A_{E_1} \tag{14}$$

Where J_{S_1} is the saturation current density of Q_1 and A_{E_1} is the emitter area of Q_1.
We have:

$$A_{E_1} = K A_{E_2} \tag{15}$$

The transistors Q_1 and Q_2 have the same transport saturation current, as a result, the saturation current density J_{S_1} is K times larger than the saturation current density J_{S_2}. By substituting (11), (12), (13), (14) and (15) in (10), we find:

$$I_{R_1} = \frac{V_T \ln K}{R_1} \tag{16}$$

Note that the current I_{R_1} forms the PTAT current and is usually symbolized by I_{PTAT}.
We also have:

$$V_{R_2} = V_{EB_2} - V_{REF} \tag{17}$$

By substituting (7), (8), (9) and (17) in (6), we find:

$$V_{REF} = K_R (V_{EB_2} + \frac{R_2}{2R_1} V_T \ln K) \tag{18}$$

With,

$$K_R = \frac{2R_3}{R_2 + 2R_3} \tag{19}$$

If we take into account the input offset voltage V_{OS}, we have $V_X = V_Y + V_{OS}$. Thus the expression of V_{REF} becomes:

$$V_{REF} = K_R (V_{EB_2} + \frac{R_2}{2R_1} V_T \ln K + \frac{R_2}{2R_1} V_{OS}) \tag{20}$$

As shown in (20) showns that the factor amplifying the input offset voltage is reduced in half in proposed circuit compared to that of the conventional scheme see (1).

Differentiating (19) with respect to absolute temperature yields:

$$\frac{\partial V_{REF}}{\partial T} = K_R [\frac{\partial V_{EB_2}}{\partial T} + \frac{R_2}{2R_1} \ln K (\frac{\partial V_T}{\partial T})] \tag{21}$$

To achieve a near-zero TC of VREF, $\frac{\partial V_{REF}}{\partial T} = 0$. Thus,

$$\frac{R_2}{2R_1} \ln K = -\frac{\partial V_{EB_1} / \partial T}{\partial V_T / \partial T} \tag{22}$$

For the CMOS technology used in our design, $\frac{\partial V_{EB_2}}{\partial T} \approx 1.89\ \text{mV}/\ ^\circ\text{C}$, and by using (2), we have $\frac{\partial V_T}{\partial T} = \frac{k_B}{q} \approx 0.0862\ \text{mV}/\ ^\circ\text{C}$, from where we get:

$$\frac{R_2}{2R_1} \ln K = 21.9 \tag{23}$$

The value of K is set to 8, thus:

$$R_2 = 21 R_1 \tag{24}$$

Note that the final values of the resistances calculated by the hand must be adjusted during the design of the circuit to obtain an optimal value of the temperature coefficient of V_{REF} over the required temperature range.

The minimum supply voltage to ensure proper operation of the proposed circuit and obtain an output voltage reference V_{REF} less than 1 V with a small variation in the required temperature range is such that the following two constraints are met:

$$V_{DD} \geq V_{REF} + V_{SD_{sat3,4}} + V_{SD_{sat6,7}} \tag{25}$$

And,

$$V_{DD} \geq V_{EB_2} + V_{SD_{sat1,2}} + V_{SD_{sat6,7}} \tag{26}$$

Where $V_{SD_{sat3,4}}$ is the overdrive voltage of M_3 and M_4, $V_{SD_{sat1,2}}$ is the overdrive voltage of M_1 and M_2 and $V_{SD_{sat6,7}}$ is the overdrive voltage of M_6 and M_7.

3.2. PSRR Analysis

In order to reduce ripple from the supply voltage which directly influences the performance of the PSRR, a pre-regulation stage is added to isolate the supply voltage VDD from both the supply voltage of the operational amplifier and the supply voltage of the BGVR core generator.

To establish the expression of the PSRR, the high frequency small signal model of the proposed circuit is realised see Figure 5. For the calculation of the PSRR, a similar method to that adopted in [21], is applied. The body effect is ignored and both Q1 and Q2 BJT transistors can be considered as short-circuited.

The voltage vdif shown in Figure 5 is the small signal part of the differential input voltage of the OpAmp.

We have:

$$\mathrm{PSRR}(s) = \frac{v_{dd}(s)}{v_{ref}(s)} \tag{27}$$

Where $v_{dd}(s)$ is the high frequency small signal part of V_{DD}, $v_{ref}(s)$ is the high frequency small signal part of V_{REF} and s is the complex variable of Laplace.

We can write that:

$$\mathrm{PSRR}(s) = \frac{v_{dd}(s)}{v_{reg}(s)} \times \frac{v_{reg}(s)}{v_{ref}(s)} \tag{28}$$

Where $v_{reg}(s)$ is the high frequency small signal part of V_{REG}. For a simple notation the variable s is omitted in the voltages symbols.

In the node D_3, the Kirchhoff's Current Law gives:

$$(g_{m_3} + Y_3)\, v_{reg} + R_2^{-1} v_{d1} = (Y_3 + Y_{11} + R_2^{-1})\, v_{ref} \tag{29}$$

Where, v_{d1} is the high frequency small signal part of V_{D1}, and,

$$Y_3 = g_{03} + C_{ds3}s \tag{30}$$

$$Y_{11} = R_3^{-1} + C_{gd3}s \tag{31}$$

In the node D_1, the Kirchhoff's Current Law gives:

$$v_{d1} = \frac{(g_{m_1} + Y_1)}{(Y_1 + Y_{10} + R_2^{-1})} v_{reg} + \frac{R_2^{-1}}{(Y_1 + Y_{10} + R_2^{-1})} v_{ref} \tag{32}$$

Where,

$$Y_1 = g_{01} + C_{ds1}s \tag{33}$$

$$Y_{10} = R_1^{-1} + C_{gd1}s \tag{34}$$

By substituting (32) in (29), we obtain:

$$\frac{v_{reg}}{v_{ref}} = \frac{N_1(s)}{D_1(s)} \tag{35}$$

Where,

$$N_1(s) = (g_{m3} + Y_3).(Y_1 + Y_{10} + R_2^{-1}) + R_2^{-1}.(g_{m1} + Y_1) \tag{36}$$

$$D_1(s) = (Y_3 + Y_{11})(Y_1 + Y_{10} + R_2^{-1}) + R_2^{-1}(Y_1 + Y_{11}) \tag{37}$$

In the node D_6, the Kirchhoff's Current Law gives:

$$N_4(s)v_{reg} = Y_4 v_{d4} + Y_1 v_{d1} + Y_3 v_{ref} + (g_{m5} + Y_6)\, v_{dd} + (g_{m6} + C_{gd6}s)\, v_{g6} + (g_{m5} + C_{gs5}s)\, v_{g5} \tag{38}$$

Where,

$$N_4(s) = [g_{mT} + Y_T + g_{m5} + Y_5 + Y_6 + (C_{gd6} + C_{gs5} + C_4)s] \tag{39}$$

$$g_{mT} = g_{m1} + g_{m2} + g_{m3} + g_{m4} \tag{40}$$

$$Y_T = Y_1 + Y_2 + Y_3 + Y_4 \tag{41}$$

$$Y_2 = g_{02} + C_{ds2}s \tag{42}$$

$$Y_4 = g_{04} + C_{ds4}s \tag{43}$$

$$Y_5 = g_{05} + C_{ds5}s \tag{44}$$

$$Y_6 = g_{04} + C_{ds6}s \tag{45}$$

$$C_4 = C_{gs1} + C_{gs2} + C_{gs3} + C_{gs4} + C_{bs1} + C_{bs2} + C_{bs3} + C_{bs4} \tag{46}$$

And, v_{d4} is the high frequency small signal part of V_{D4}, v_{g5} is the high frequency small signal part of V_{G5} and v_{g6} is the high frequency small signal part of V_{G6}.

In the node D_4, the Kirchhoff's Current Law gives:

$$v_{d4} = \frac{(g_{m_4} + Y_4)}{(Y_1 + Y_9)} v_{reg} \tag{47}$$

Where,

$$Y_9 = (R_2 // R_3)^{-1} + C_{gd4}s \tag{48}$$

In the node G_5, the Kirchhoff's Current Law gives:

$$v_{g5} = \frac{A_v}{r_{out}[Y_{out} + (C_{gd5} + C_{gs5})s]} v_{d1} + \frac{C_{gs5}s}{[Y_{out} + (C_{gd5} + C_{gs5})s]} v_{reg} \tag{49}$$

Where, A_v is the open-loop gain of the opamp, r_{out} is its output resistance, C_{out} is all capacitance connected from the output of the opamp to ground and,

$$Y_{out} = r_{out}^{-1} + C_{out}s \tag{50}$$

In the node G6, the Kirchhoff's Current Law gives:

$$[Y_b + (C_1 + C_{gd6})s]v_{g6} = C_1 s v_{dd} + C_{gd6} v_{reg} + (g_{m8} + Y_8) v_{s8} \tag{51}$$

Where, v_{s8} is the high frequency small signal part of V_{S8} and,

$$Y_b = R_b^{-1} + C_{gd8}s \tag{52}$$

Where R_b represent the output resistance of current source bias network and,

$$C_1 = C_{gs6} + C_{gs7} + C_{bs6} + C_{bs7} \tag{53}$$

$$Y_8 = g_{08} + C_3 s \tag{54}$$

$$C_3 = C_{ds8} + C_{gd7} \tag{55}$$

In the node S_8, the Kirchhoff's Current Law gives:

$$v_{s8} = \frac{(g_{m7} + Y_7)}{(g_{m8} + Y_8 + Y_7 + C_2 s)} v_{dd} + \frac{(Y_8 - g_{m7})}{(g_{m8} + Y_8 + Y_7 + C_2 s)} v_{g6} \tag{56}$$

Where,

$$C_2 = C_{gs8} + C_{ds8} \tag{57}$$

By substituting (56) in (51), we obtain:

$$v_{g6} = \frac{N_2(s)}{D_2(s)} v_{dd} + \frac{N_3(s)}{D_2(s)} v_{reg} \tag{58}$$

Where,

$$N_2(s) = C_1 s(g_{m8} + Y_7 + Y_8 + C_2 s) + (g_{m8} + Y_8)(g_{m7} + Y_7) \tag{59}$$

$$N_3(s) = C_{gd6} s(g_{m8} + Y_7 + Y_8 + C_2 s) \tag{60}$$

$$D_2(s) = [Y_b + (C_1 + C_{gd6})s)](g_{m8} + Y_8 + Y_7 + C_2 s) + (g_{m7} - Y_8)(g_{m8} + Y_7) \tag{61}$$

By substituting (32), (35), (47), (49) and (58) in (38), we obtain:

$$\frac{v_{reg}}{v_{dd}} = \frac{(g_{m5} + g_{m6} + Y_6 + C_{gd6}s) N_2(s) D_3(s) D_1(s)}{D_4(s) - [D_5(s) + D_6(s) + D_7(s) + D_8(s)]} \tag{62}$$

Where,

$$D_3(s) = [Y_{out} + (C_{gd5} + C_{gs5})s](Y_1 + Y_{10} + R_2^{-1}) r_{out} \tag{63}$$

$$D_4(s) = N_4(s) D_3(s) D_1(s) D_2(s) \tag{64}$$

$$D_5(s) = D_1(s)D_3(s)\left[\frac{D_2(s)Y_4(g_{m4}+Y_4)}{(Y_4+Y_9)} + N_3(s)(g_{m6}+C_{gd5}s)\right] \tag{65}$$

$$D_6(s) = D_1(s)D_2(s)Y_1(g_{m1}+Y_1)r_{out}[Y_{out}+(C_{gd5}+C_4)s] \tag{66}$$

$$D_7(s) = D_1(s)D_2(s)(g_{m5}+C_4s)[A_V(g_{m1}+Y_1)+r_{out}(Y_1+Y_{10}+R_2^{-1})C_4s] \tag{67}$$

$$D_8(s) = N_1(s)D_2(s)\left\{r_{out}Y_1R_2^{-1}[Y_{out}+(C_{gd5}+C_4)s]+Y_3D_3(s)+(g_{m5}+C_4s)A_vR_2^{-1}\right\} \tag{68}$$

Note that g_{mi} represents the small signal source-drain conductance of the MOSFET M_i and Y_i represents the equivalent admittance for the shunt connection of the impedance of the capacitor and a resistor.

By substituting (35) and (62) in (28), we obtain:

$$PSRR(s) = \frac{(g_{m5}+g_{m6}+Y_6+C_{gd6}s)N_2(s)D_3(s)N_1(s)}{D_4(s)-[D_5(s)+D_6(s)+D_7(s)+D_8(s)]} \tag{69}$$

The expression of the PSRR(s) shows that its transfer function has 7 poles and 7 zeros, and consequently the transient response is convergent and the proposed circuit system is stable.

The expression of low frequency PSRR is obtained by replacing s=0 in all the terms containing the complex variable s. Thus,

$$PSRR(0) = \frac{(g_{m5}+g_{m6}+g_{06})N_2(0)D_3(0)N_1(0)}{D_4(0)-[D_5(0)+D_6(0)+D_7(0)+D_8(0)]} \tag{70}$$

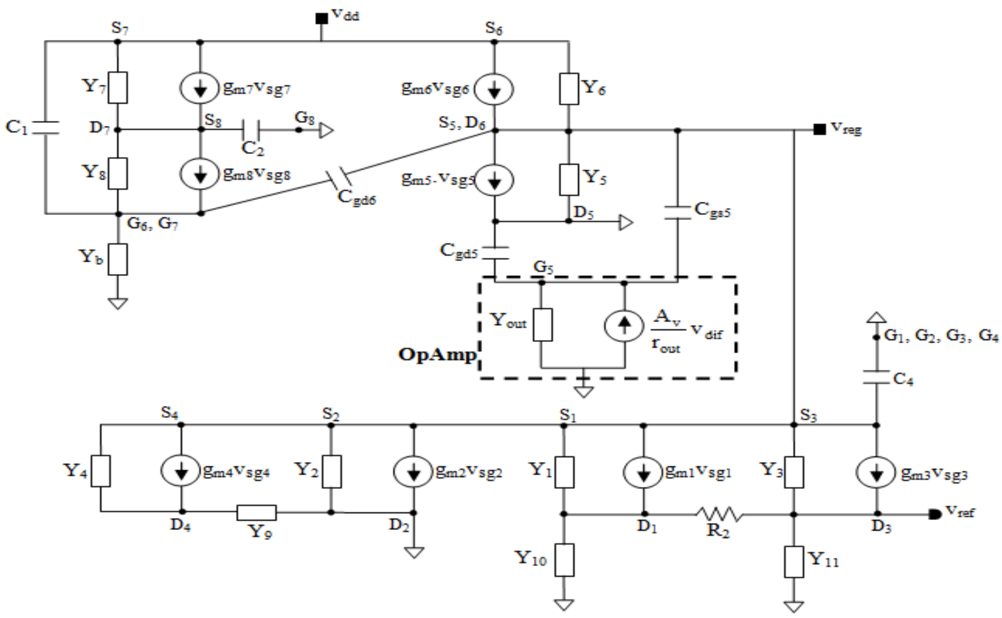

Figure 5. High frequency small signal model of proposed sub-1V BGVR

4. SIMULATION RESULTS AND DISCUSION

The proposed design of sub-1V bandgap voltage reference using the opamp based β-multiplier with resistive division configuration was simulated in 0.18-μm standard CMOS technology using Cadence Virtuoso Spectre Simulator. The proposed circuit generates an output voltage reference VREF of 634.6mV at 27°C when the supply voltage is set to 1.8V. Figure 6 showns the variation of the output voltage reference over temperature range -40°C to 140°C for different values of the supply voltage VDD, the maximum value of the temperature coefficient of VREF is less than 36ppm/°C with a minimum supply voltage of 1.2V. As it is shown in Figure 7, the DC value of PSRR is -93dB whene the supply voltage is 1.8V. The measurement line regulation of VREF is 104µV/V as is it shown in Figure 8. As it is shown in Figure 9, the two input voltages of the opamp have exactly the same value witch is equal to 0.6255 V whene the supply volage varies from 1.2 V to 1.8 V and therefore the error introduced by the input offset voltage of the opamp is eliminated.

The layout of the proposed sub-1V bandgap voltage reference circuit is shown in Figure 10. For resistors implementation, the non-silicide P+ poly-resistor type is chosen wich has a very low temperature coefficient in order to ensure robustness of the circuit to variations in temperature and voltage. The layout area is 0.0337 mm2.

Table 1 summarizes performance characteristics of the proposed sub-1V BGVR and comparison with related works is given. As it is shown in Table 1, the proposed circuit provides a high value of the PSRR at high frequencies ranging from 1MHz up to 10MHz, which is significantly higher than the value found in the related work see Table 1.

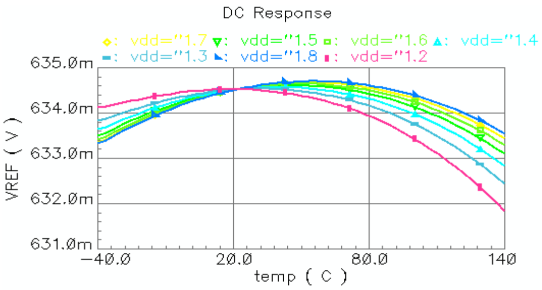

Figure 6. Simulated temperature dependence of output voltage reference for different values of power supply voltage

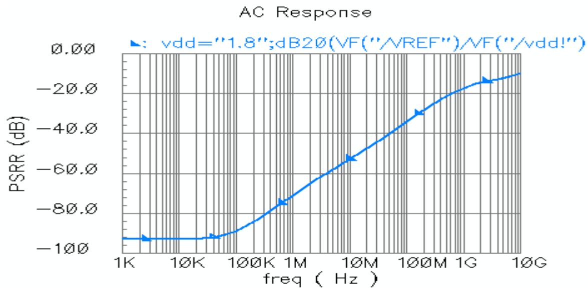

Figure 7. Simulated PSRR of the proposed sub-1V BGVR

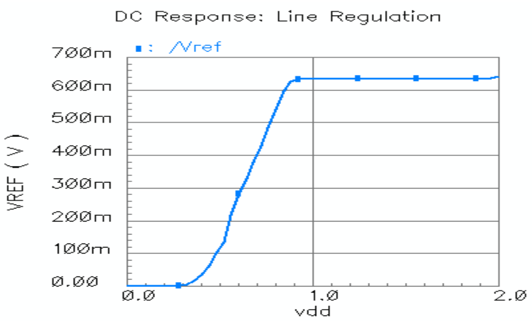

Figure 8. Simulated line regulation of the proposed sub-1V BGVR

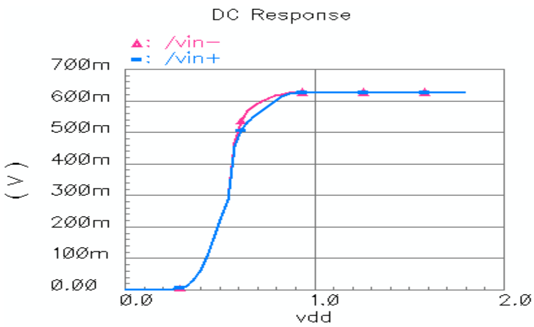

Figure 9. Simulation of the error introduced by input offset voltage of the OpAmp in proposed sub-1V BGVR

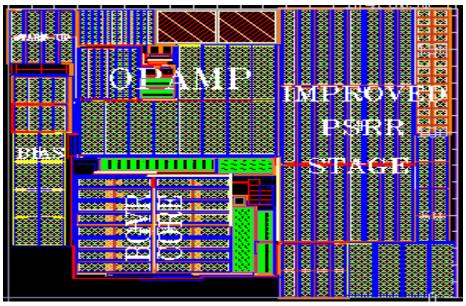

Figure 10. Layout of proposed sub-1V BGVR reference

Table 1. Performance of Proposed Sub-1V BGVR and Comparison

Performance	[14]	[15]	[16]	[17]	[18]	This work
Technology (CMOS)	0.09 μm	0.13 μm	0.18 μm	0.18 μm	0.5 μm	0.18 μm
Area (mm^2)	0.0137	0.054				0.037
$V_{DD,min}$ (V)	2.7	0.93	1.2	2.5	1.2	1.2
$V_{DD,max}$ (V)	3.6	2.0	10	6	3.6	1.8
V_{REF} (V)	0.21398	0.594	0.681	1.194	0.561	0.6346
TC (ppm/°C)	6.07	18.2	2.235	6.51		22.3
Temperature operation range (°C)	-20 to 120	-30 to 80	-50 to 115	-25 to 80	-20 to 120	-40 to 140
Line regulation (μV/V)	16,67	35		1143		104
PSRR DC	-82.7 dB at 100 Hz	-103 dB at 100 Hz	-102.5 dB at 10 Hz	-125 dB at 10 Hz	-70 dB at 1kHz	-93 dB at 10 kHz
PSRR@ 1MHz			>-20dB	-40 dB	>-20 dB	-71 dB
PSRR@ 10MHz						-52.8 dB

5. CONCLUSION

In this paper, a novel design of sub-1V bandgap voltage reference circuit with opamp based β-multiplier and resistive divider architecture is proposed. The important contribution of this work is the obtaining of an accurate voltage reference with a high value of the PSRR in a very wide frequency range. The proposed architecture of the voltage divider has made it possible to elimlate the undesirable effect of the input offset voltage of the opamp in order to obtain a very accurate value of the output voltage reference and to improve the DC value of the PSRR. In order to reduce ripple from the supply voltage which directly influences the performance of the PSRR, an improved PSRR scheme is added to isolate the supply voltage source from the supply voltage of the operational amplifier and also the supply voltage of the BGVR core generator which allows improving the value of the PSRR in high frequency. The proposed voltage reference can be used as an internal comparison voltage in LDO regulators.

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