

Design and simulate a doherty power amplifier using GaAs technology for telecommunication applications

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ABSTRACT

In this paper, a Doherty power amplifier was designed and simulated at 2.4 GHz central frequency which has high efficiency. A Doherty power amplifier is a way to increase the efficiency in the power amplifiers. OMMIC ED02AH technology and PHEMT transistors, which is made of gallium arsenide, have been used in this simulation. The Doherty power amplifier unique feature is its simple structure which is consisting of two parallel power amplifiers and transmission lines. In order to integrate the circuit, the Doherty power transmission amplifier lines were implemented using an inductor and capacitive components. Also, the Wilkinson power divider is used on the chip input. To improve the efficiency, the auxiliary amplifier dimensions is selected enlarge and the further input power is allocated it by the power divider. A parallel R-C circuit has been used at the input of transistors to improve their stability. Simulation results show that the Doherty power amplifier has 17.2 dB output power gain, 23 dBm maximum output power, and its output power $P_{1dB} = 22.6$ dBm at compression point -1 dB, also, its maximum efficiency is 55.5%.

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1. INTRODUCTION

The Power Amplifier (PA) is an essential component to build a successful wireless communication system, and usually, it is a block in the radio frequency (RF) transmitter portion that consumes the most power [1]. The power amplifier has different classes, by moving from A class towards other classes the efficiency and the linearity increases and decreases, respectively [2, 3]. In addition, the modulation has become increasingly complex by developing the telecommunication systems [4]. Also, in these modulation types, it is usual to use the variable envelope modulation method in which case the modulated signal needs linear amplification. Otherwise, if the power amplifier operates in non-linearity, the spectral expansion occurs, which is also problematic. Therefore, the goal of power amplifier designers is to design it with high efficiency without losing its linearity. One of the best and the easiest ways, to increase the power amplifier efficiency, is using the Doherty power amplifier structure. The Doherty power amplifier is the increasing efficiency method that increases the amplifier's efficiency before the saturation area [2].

Therefore, Doherty power amplifier designing and simulation according to the wireless communication standards such as WCDMA and OFDM, which utilize complex modulations such as QPSK and QAM, is very suitable [5]. The increasing growth of wireless communication technology has increased demand for wireless transmitter and receiver networks in order to achieve lower costs, smaller size and other characteristics. One of several remaining blocks, which is not yet successfully integrated, is the power amplifier (PA). Power amplifiers are main blocks for constructing wireless communication systems. Also,

radio frequency power amplifiers are one of challenging blocks in designing RF transceivers, this is due to non-linear behavior of power Amplifiers that leads to inter-modulation distortion. The rapid growth of mobile telecommunication services has increased demand for low- cost, high-efficiency, and compact equipment. Generally, power amplifier (PA) is one of the most important subsystems for radio frequency (RF) transmitters [6]. Power Amplifiers (PA) are very indispensable components in the design of numerous types of communication transmitters employed in microwave technology [7].

In recent years, due to the increasing demand for communication with high rates of transmission and receiving data, new generations and standards have been developed for data transmission that require low - energy, low - volume, low - performance standards. In high performance analog integrated circuits, operational transconductance amplifier with very high DC gain and high unity gain frequency are needed to meet both accuracy and fast settling requirements of the systems [8]. Due to the limitations of CMOS technology, a linear power amplifier is a challenging issue. Another issue in the discussion of modern wireless communication systems is battery life [9]. Power amplifiers require accurate design due to high power consumption. The common feature among most power amplifiers is that the maximum power efficiency is achieved only when the amplifier has the maximum output power [10]. Lately, several power amplifiers based on Gallium Arsenide (GaAs) technology were reported in the literature [11-15]. The pursued aim in this paper is to design a high-efficiency Doherty power amplifier for modern and digital telecommunication applications. In this research, a systematic approach is presented to design a Doherty power amplifier as integrated. In the designing process, first, the ideal elements are used, then in the final stage, we replace the actual components of the ED02AH technology with compressed elements. The available transistors in this technology were made Gallium Arsenide and in the fact, most of the previously reported compilations have used 0.18 μm CMOS technology.

2. BACKGROUND OF RESEARCH

2.1. The Doherty Power Amplifier

The power amplifiers are usually classified into different classes based on their performance and bias. In each class, amplifiers are different in their linearity, conductivity degree, efficiency, and so on features. In general, power amplifiers have two major problems. First, when they use the entire RF power range, they lose their linearity, and second, the maximum efficiency is achieved only in a power level which is usually near to the amplifier maximum input power [1, 3]. There are several ways to increase efficiency that have been proposed up to date. The Doherty power amplifier is the best option [2].

2.1.1. Methods used in Two Hertz Amplifiers

Crypts load line method: The conjugate matching method is not used to match the power amplifier output. They use the load-line matching method. In the Doherty Amplifier, because increasing efficiency was our aim, we have used the conjugate matching method at the output port and also, we have used the load line matching method in the input port [2].

Active Levon pulls Method: in the Doherty amplifier, the active Levon pull method is used. Its concept is to adjust the load impedance which is seen by a source via a second current source that the second current source is placed parallel to the first source.

The transmission Line $\frac{\lambda}{4}$ or Quarter wave transformer: Quarter wave transformer is a simple and useful circuit to match a resistive load with the transmission line input resistance. When the resistance load is matched to the source impedance, the maximum power is transmitted to the load. The quarter wave transformer is also called impedance transformer. Because due to the transmission line impedance characteristic, if the one side of the transmission line impedance is increased, the other side impedance decreases [16].

2.1.2. The Doherty Amplifier Configuration and Advantages

The Doherty power amplifier is mainly constructed by two sub-amplifiers. The classical Doherty amplifier structure comprises a major amplifier and an auxiliary amplifier. The main power amplifier is usually B class amplifier or AB class amplifier, and the auxiliary power amplifier is usually a C class amplifier [17].

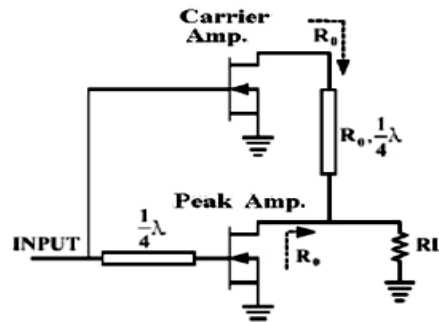


Figure 1. The Doherty power amplifier confirmation [2]

2.1.3. Main performance and step by step Doherty amplifier

a) First area: Output signal with low input power level

In this area, the input signal is not sufficient to illuminate the auxiliary amplifier and the auxiliary amplifier is off. So, in this stage, the amplifier output impedance is infinite.

b) Third area: Output signal with high input power level

This area is posing when the operating input signal level has reached its maximum value. In this case, the auxiliary amplifier is also saturated.

c) Second area: Output signal with medium input power level

In this area, the amplifier operates between the first and third regions. This region begins when the auxiliary amplifier starts to direct and the main amplifier output voltage has been saturated.

2.2. Transistors With Heterogeneous Connection

2.2.1. The Gallium Arsenide Benefits to the Silicon

Table 1. GaAs and Si Physical and Electronic Properties Comparison [18]

Properties	unit	GaAs	Si
electrons Intrinsic mobility at 300 K	cm ² V ⁻¹ s ⁻¹	8500	1500
The electron saturation velocity	cms ⁻¹	1.3 × 10 ⁷	9 × 10 ⁶
The cavity intrinsic mobility at 300 K	cm ² V ⁻¹ s ⁻¹	400	450
Heat conductivity coefficient at 300 K	Wcm ⁻¹ K ⁻¹	0.46	1.5
Dielectric constant		12.9	11.9
The electrical resistor at 300K	Ω cm	10 ³	3.7 × 10 ⁸
The forbidden band at 300 K	eV	1.424	1.12

2.2.2. High-electron Mobility Transistors

One of the most promising devices for RF power amplifier and high-voltage switching applications is the high-electron mobility transistor (HEMT). In HEMT transistors, the layers are designed in a way that the channel free electrons are separated from the electron donor atoms, which leads to increase the electrons mobility by reducing the scattering phenomenon. This advantage and other elegant advantages of this structure have created significant improvement in these components efficiency in comparing to the MOSFET components. One way to increase the HEMT's efficiency is to replace its GaAs channel with InGaAs. The benefits of this action can be summarized as follows:

- a) Increasing the electron transfer InGaAs characteristic compared to GaAs characteristic which is more mobile than GaAs due to the smaller electron mass in InGaAs.
- b) The carriers most constraint in the quantum well channel due to the two heterogeneous connection existence
- c) The passband great gap in the AlGaAs / InGaAs interface (due to the greater difference in bandwidth), which increases the loads surface density and it leads to an increase the Idss and gm [19].

This structure components are called Pseudomorphic HEMT. Today, heterogeneous connection transistors are used in telecommunication systems, including cell phones and satellite TVs worldwide. HEMT devices are designed and built with very high cut-off frequencies up to FT =94GH and their output power about 7000 MW and there is more searching and trying to take place with a much faster acceleration that lead to increase the cut-off frequency, the gain of gm, and especially to increase the output power [20, 21].

2.2.3. Conclusion

The heterogeneous transistors structure, such as HEMT and PHEMT, are different from other FETs types and they are able to present a much better performance than the standard FETs. Gallium arsenide devices are also suited for high power applications due to their better efficiency and better linearity than silicon devices. HEMT further development and improvement is known as PHEMT. HEMT and PHEMT are rapidly replacing FETs technology in military and commercial applications that require low noise, high output power, and low distortion, especially at the millimeter frequency ranges. Using PHEMT is a popularity for power amplifying with high efficiency.

2.3. Reported Doherty Power Amplifiers

Reviewing Reported Designs in Articles: In [22], 2.8 GHz Doherty power amplifier is designed with an active balun on the chip. In this design, 0.18 μm CMOS technology has been used. The presented active balun at the Doherty amplifier input is actually replaced instead of the required power divider in the Doherty structure. The Cascade structure has been used for two amplifiers. N_1 and N_2 are the main amplifier structure, N_3 and N_4 are also auxiliary amplifier structure. These two amplifiers Cascade structure reduce the probability of the transistor connection breaking, and that lead to obtain high output power and better isolation. In addition, the $L_1, L_2, L_3, C_1, C_2, P_1,$ and N_1 components are forming the active balun structure which is used in this paper. In [23], 2.4 GHz Doherty power amplifier is presented which has been fully integrated. In this amplifier, a Cascade structure and a common source-common gate have been used as the main amplifier and the Cascade structure, and a common source-common source has been used as an auxiliary amplifier. In Figure 3, it is visible that the Doherty power amplifier is presented.

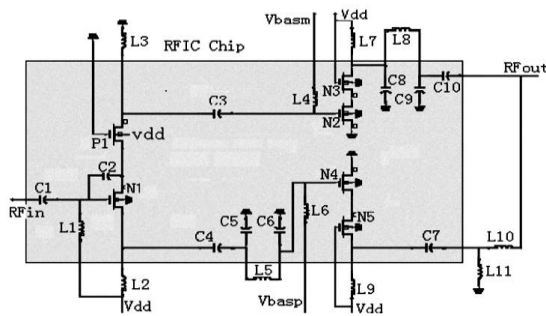


Figure 2. Doherty amplifier with active Balun input [22]

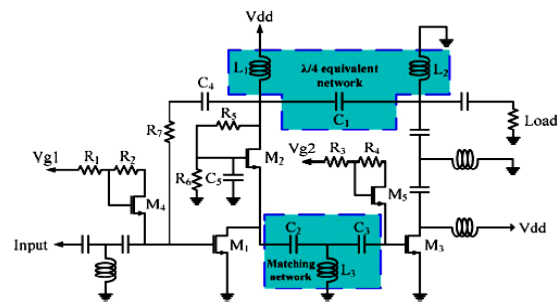


Figure 3. Doherty cascade-cascade power amplifier structure [23]

Paper [24] presents a broadband Doherty power amplifier structure to WiMAX applications. In this paper, an integrated Doherty power amplifier is simulated in 0.18 μm CMOS technology. In Figure 4 and Figure 5, the power amplifier configuration is shown. In this paper [25], a Doherty power amplifier with adaptive bias circuit has been designed and implemented. The Doherty power amplifier is working at 2.4 GHz frequency and it has been simulated in the 0.15 μm CMOS technology.

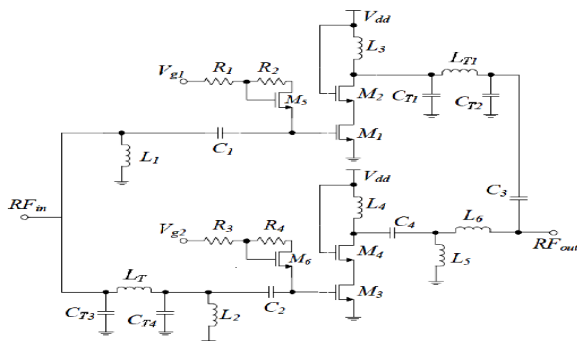


Figure 4. The Doherty power amplifier Simple structure [26]

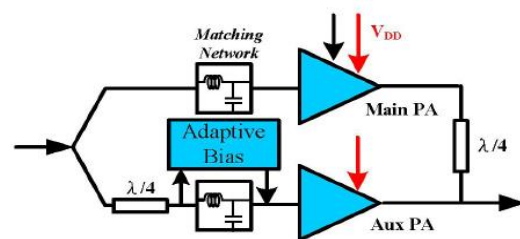


Figure 5. A doherty power amplifier structure with adaptive bias circuit [27]

3. RESEARCH METHOD

3.1. Initial Design And Simulations Stages

3.1.1. Simulation Technology

OMMIC ED02AH technology is used in this research. OMMIC is a manufacturer which is making a Monolithic Microwave Integrated Circuit (MMIC). This manufacturer uses (GaAs, GaN, InP) materials to make epitaxial wafers and devices. The used technology in this study is ED02AH which is specifically developed for microwave applications and millimeter wave. abbreviation of ED02AH is meaning as follows:

E: Enhancement mode transistors (OFF) D: Depletion mode transistors (ON) A: A type OMMIC process
 H: Pseudo-layer of HEMT (PHEMT) 02: Gate transistor length 0.2 μm (in fact, it is 0.18 μm)

3.1.2. Main Power Amplifier Design

Designing the main and auxiliary amplifier is very similar to the conventional amplifier design. A section of the signal power amplifier is large because it has nonlinear behavior near the saturation area. Many device makers do not offer a large signal model for their devices, and often the small signal model, such as S parameters or voltage static curves (IV), is only provided. Because S parameters are only applicable to small signal levels, and it does not present good viewpoint about the amplifier designing at the maximum RF output power. To design the power amplifier, the first step is the load line method. In this method, the voltage-current device curves are used to calculate the load signal line impedance. This is the optimal impedance which must be seen using the matching circuit in the device drain.

Generally, in order to increase the amplifier stability, a small resistor and a small capacitor are placed in parallel in its input. It improves stability but it causes a little decreasing in the power amplifier gain. The transistor is usually biased by an inductor with a V_{DD} power supply.

3.1.3. Auxiliary Amplifier Design

To design an auxiliary amplifier which is biased in C-Class, it should be noted that this amplifier starts to turn on and amplify when the main amplifier has been saturated. When the input power level is low, this amplifier remains still due to its negative bias, and its observed impedance at its output is very large. Therefore, it does not play a role in the main amplifiers and when it begins to turn on the main amplifier is saturated. In order to match this amplifier's input and output we are performing like the main amplifier, i.e., in the input, we are using the conjugate matching, and in its output, the Levon pull method is used so that in its output an optimized impedance is observed.

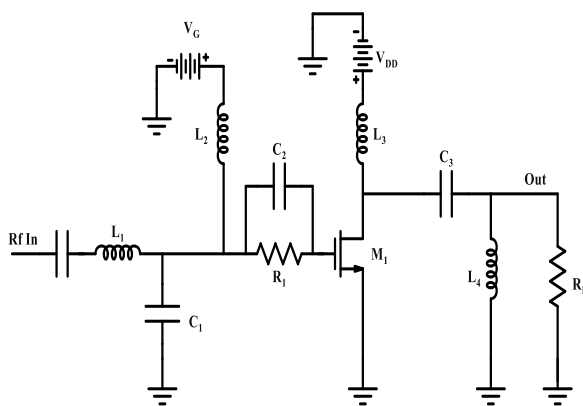


Figure 6. Main amplifier structure in doherty amplifier

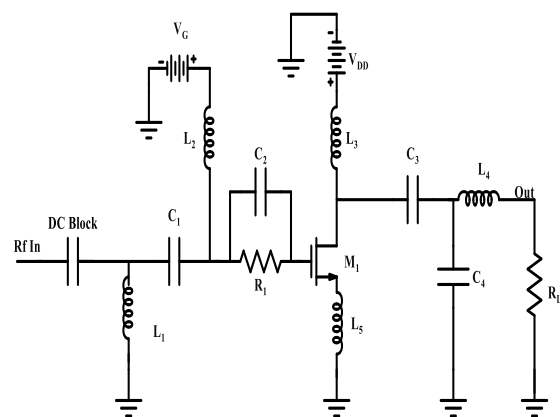


Figure 7. Auxiliary amplifier structure in doherty amplifier

3.2. The Power Amplifier Design and Simulation

Designed Doherty power amplifier structure: Figure 8 shows the designed power amplifier in which capacitors $C_1, C_2, C_3,$ and C_4 are coupler capacitors. These capacitors prevent DC circuits from power loss. The chip input and output resistances are considered 50 Ω according to the antennas standard. Also, in this amplifier, a Wilkinson power divider is used to divide power. The reason to use this power divider is to prevent two signal sources using in the circuit.

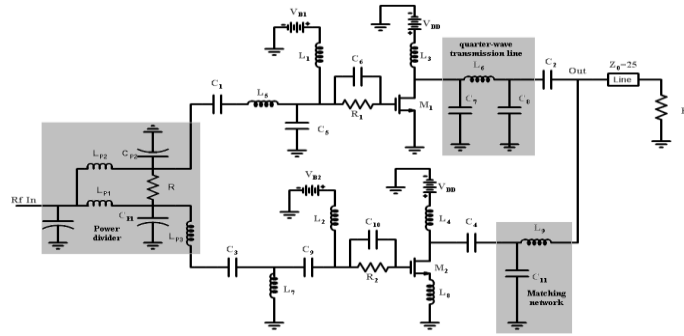


Figure 8. Doherty power amplifier structure

The L_1 and L_2 inductors prevent the AC signal losing and also that are effective in the input matching and C_{gs} capacitor is effective in the M_1 and M_2 transistors neutralization. These inductors also obtain a path to provide gate bias voltage. The L_3 and L_4 inductors, in addition to supply the drain bias voltage path, prevent the AC signal loss. The L_9 inductor and the C_{11} capacitor are also used to match the auxiliary power amplifier output impedance. There is a quarter wave transformer in the Doherty power amplifier. In this circuit, C_7 , and C_8 capacitors and L_6 inductor replaced the quarter wave transformer. This transformer has a 90-degree phase transition, and its impedance characteristic is twice greater than the impedance which was found in the output node.

The high-pass network (L_2 - C_9 - L_7), in addition to its input matching role, it also causes a 90-degree phase difference, and in the reality, it causes their combination to take place in both the main and auxiliary amplifier signals that were coherent in the output and at the best mode [4].

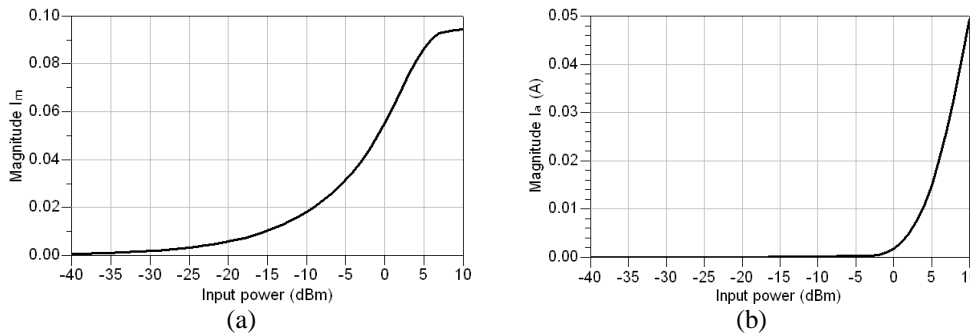


Figure 9. The current main component (a) The main amplifier component, (b) the auxiliary amplifier component in terms of input power

If the power ratio between port 2 and 3 is defined as $K^2 = \frac{P_3}{P_2}$, then to continue the designing the following equations should be followed [16].

$$Z_{03} = Z_0 \sqrt{\frac{1+K^2}{K^3}} \tag{1}$$

$$Z_{02} = K^2 Z_{03} = Z_0 \sqrt{K(1+K^2)} \tag{2}$$

$$R = Z_0 \left(K + \frac{1}{K} \right) \tag{3}$$

To complete the circuit monolithic, the transmission lines are also implemented with the compact elements model (inductor/capacitor) as mentioned in the preceding chapters, and the inductor and capacitor values are also calculated according to (3). In the performed design, we consider the power ratio of the port 3 to port2 equal to ($K^2=1/2$) and we made the design according to it.

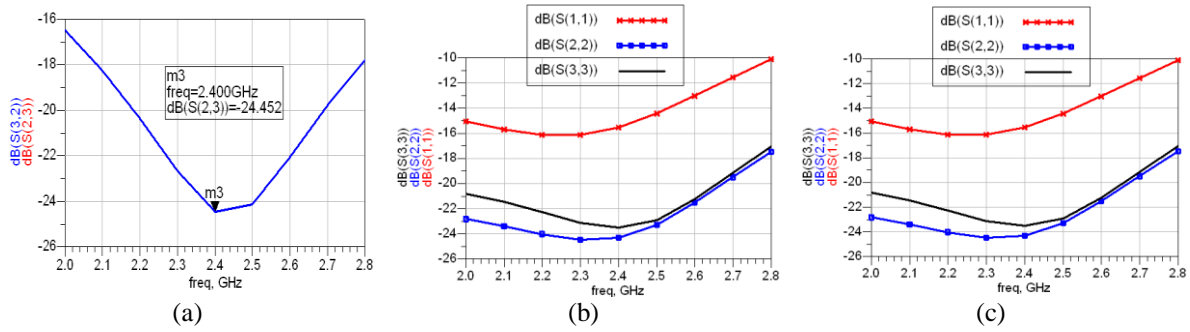


Figure 10. Unequal wilkinson power divider S parameters

Table 2. The Designed Doherty Power Amplifier Elements Values in the Figure 10

Element	Value	Element	Value	Element	Value
C ₁	8 pF	C ₁₁	1.7 pF	L ₆	1.65 nH
C ₂	12 pF	C _{P2}	0.85 pF	L ₇	0.7 nH
C ₃	8 pF	C _{P3}	1.88 pF	L ₈	0.5 nH
C ₄	2 pF	R	100.45 Ω	L ₉	2.2 nH
C ₅	1.1 pF	R ₁	50Ω	L _{P2}	5.1 nH
C ₆	3 pF	L ₁	4.2 nH	L _{P3}	4.2 nH
C ₇	2.65 pF	L ₂	3.2 nH	M ₁	nbd=6, wu= μ 65m, L _g =0.2 μm
C ₈	2.65 pF	L ₃	7.3 nH	M ₂	nbd=6, wu= μ 80m, L _g =0.2 μm
C ₉	0.7 pF	L ₄	6 nH	R _L	50 Ω
C ₁₀	1 pF	L ₅	5.3 nH	R ₂	9Ω

4. RESULTS

4.1. Simulation Results

In this section, the designed Doherty power amplifier results are presented. Simulations were performed by the 2009 ADS software. Also, to simulate this amplifier, as mentioned earlier, MOMMIC ED02AHμ2 / 0 technology was used. The designing and simulation were performed at a 2.4GHz central frequency by using a 3V voltage source. The simulation results are considered by non-ideal and real elements, such as an inductor coil in the technology. In this section, output power, power gain, and power added efficiency (PAE) diagrams will be shown. In addition, the S parameters are investigating and examining twice times.

In Figure 11(a), as shown, the power amplifier gain is shown in terms of input power. The power amplifier gain is 17.3 dB, but as it is known that its amount has slightly increased somewhere in the input power. To have a better efficiency on the auxiliary amplifier dimensions, we can also send additional input and input power to it. so, by using this method, efficiency has been improved, but it makes it difficult to keep the power amplifier transistor in the low input power range. the reason for this increase is also the start of an auxiliary power amplifier. Figure 11(b) shows the amplifier output power in terms of input power. According to Figure 11(b), the output power is linearly increased up to the input power in which the input power amount is 7dBm. Thus, in the 7 dBm input power its compression point takes place. The output power at this compression point is P1dB=22. 6dBm. Also, for power input 9 dBm, the maximum output power is equal to Psat= 23.2dBm.

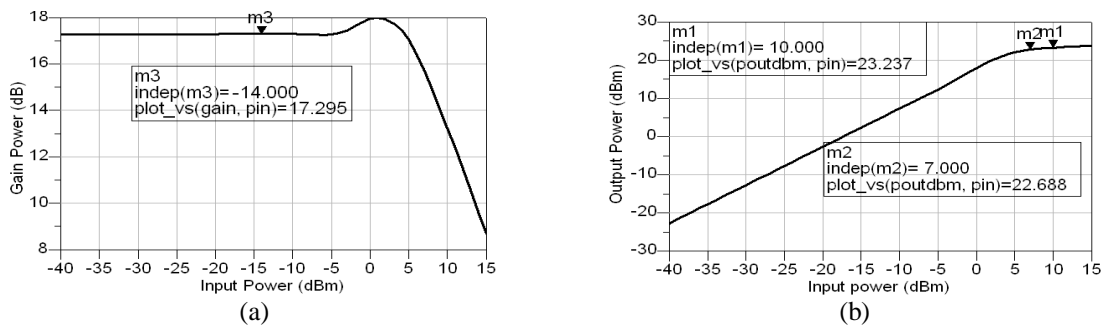


Figure 11. (a) power efficiency and (b) output power, in terms of input power

Figure 12 represents PAE (%) in terms of input power. The power additional efficiency increases by increasing the input power, we have not been able to achieve maximum efficiency only at the maximum input power (P_{sat}), but in Woody's powers we have a high productivity, between these two maximum efficiency points, because the auxiliary amplifier receives more input power, it has rapidly improved the main component of the current and, therefore, the efficiency loss is not significant and has almost reached the P_{sat} value. As it is distinct, the power additional efficiency with input power 4 dBm to 5 dBm are attending to its maximum value of 55.4% and then it increases slightly after a slight decreasing. The input power P_{1dB} the power added efficiency is 54.6% and at its maximum input power, it is again at its highest level. After investigating the Doherty power amplifier S parameters, in Figure 14 we plotted the stability coefficient (K) and the μ coefficient in a wide frequency band, which is shown in Figure 13, it has a $K > 1$ and $\mu > 1$. Although these parameters are usually not presented in power amplifiers, if these parameters are greater than 1, then unconditional stability will be maintained for the power amplifier. In Figure 15, it is observed the first and second harmonics output power ($f_2 = 4.8\text{GHz}$) and third harmonic ($f_3 = 7.2\text{GHz}$). The second harmonic ramp is two times greater than the first harmonic and the third harmonic ramp is three times greater than the first harmonic. The harmonics output power is specified with the P_{1dB} input power. The second and third output power harmonics is calculated in terms of the original or carrier harmonics. The difference between the output of the second harmonic is -20.57 dBc and the difference between the third harmonic output power in terms of the carrier is -28.4 dBc.

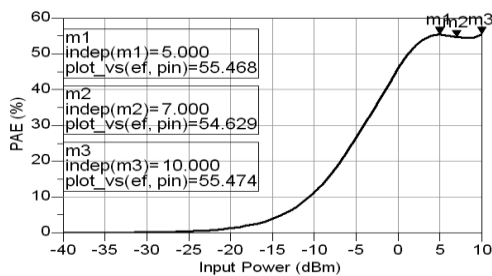


Figure 12. Power amplifier E in terms of input power

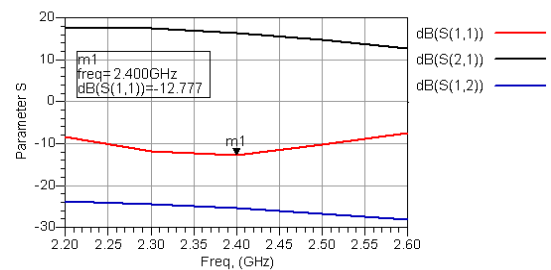


Figure 13. Doherty power amplifier s parameters

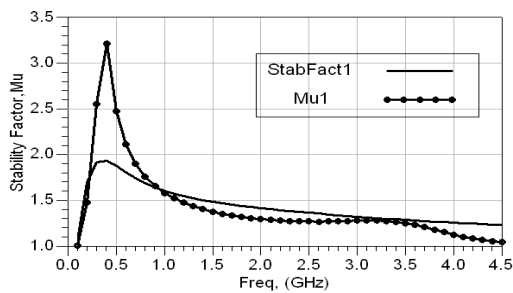


Figure 14. Doherty power amplifier stability coefficients

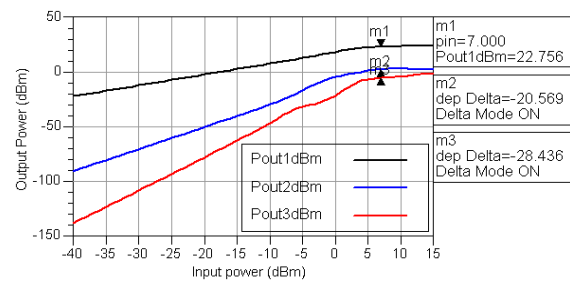


Figure 15. The Doherty amplifier first, second and third output power harmonic

4.2. Monte Carlo Analysis

To analyze the designed power amplifier, in a difficult situation as there are some problems with the circuit and it leads that the circuit has some inconsistency, this analysis is performed. To analyze this analysis, we selected 15 data randomly. Then, with 0.01 standard deviation, these values are summed up with the various components which are used in the designed amplifier nominal value and each time the simulation is performed. In fact, we simulate all the components in the circuit, including inductors, capacitors, and transistor gate widths, we have summed up 0.01 randomly data with their nominal value then we have simulated and written down the results [26].

According to the results, it is observed that the results are not very sensitive to random issues and the important design parameters have not changed significantly. In addition, by comparing the obtained data in this analysis with the original design results, it can be observed that the design was almost in the best situation.

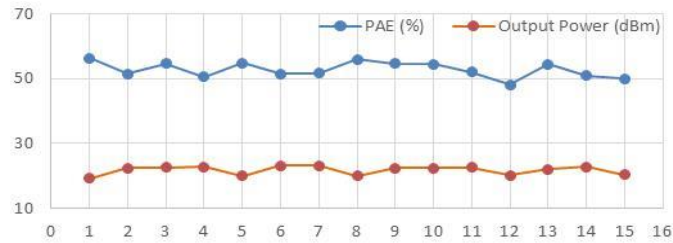


Figure 16. The obtained results from monte carlo analysis

4.3. Conclusion

By comparing the performed design, we find that the designed Doherty amplifier has higher efficiency than other amplifiers, which are mostly designed with CMOS technology, while this amplifier also provides appropriate output power and power gain. As a result, the gallium arsenide devices using to design a power amplifier over silicon devices has some advantages that are the higher output power and the higher efficiency. But this design disadvantages can be the existence of a large power divider at the entrance, which basically occupies a lot of space on the chip.

Table 3. Comparison between the Designed Amplifier with the Presented Amplifiers

Work type	Frequency (GHz)	Voltage Source (V)	PAE@Psat [%]	PAE@P1dB [%]	Psat [dBm]	P1dB [dBm]	Power gain (dB)	Technology [μm]	design
Making	2.4	2	26.7	23	20.5	17.5	16	90nm- CMOS	[27]
Design	2.45	3.3	47.6	45	22.4	21.3	20	0.18μm- CMOS	[22]
Making	2.4	3.3	15	14	22	21	12	0.18μm -CMOS	[23]
Design	2.5	3	41	33	24	22	11	0.18μm -CMOS	[24]
Making	2.4	3	34	33	22.6	21.4	10.6	0.18μm- CMOS	[25]
Design	2.4	3	53	51	20.9	19	17	0.18μm- CMOS	[28]
Design	2.4	3	43.6	40	25	24	10	GaAs -HEMT	[29]
Design	2.4	3	55.4	54.6	23.2	22.7	17.2	0.2μm -PHEMT	In this study

5. CONCLUSION

The Doherty power divisor simulation was performed by the elements in technology and coil inductors. In order to improve the Doherty amplifier efficiency, the auxiliary amplifier dimensions are selected larger and the Wilkinson divider is designed unequal to send more input power to the auxiliary amplifier. By this method, not only the efficiency at the two points of input power reaches its maximum, but at the same time between the two points, there has been no significant drop in efficiency. To match both the auxiliary amplifier and the main amplifier output phases, in the auxiliary amplifier entrance, the quarter wave transformer was not used, but it is used like as inductive and capacitive high pass network, that is used in its entrance to match and bias to compensate the phase difference. The designed power amplifier has 17.2 dB power gain, 23 dBm power output, and $P_{1dB} = 22.6$ dBm, and with a maximum output of 55.5%.

In this amplifier structure, the simple methods such as active Levod pull method are used and there is not any the envelope control complex circuits usage, such as removing and rebuilding the envelope. Hence, it is much simpler than other methods to increase efficiency. But its disadvantages include: the Doherty Amplifier is suitable for narrow-band applications and it is not a broadband amplifier. But in modern wireless communications applications and digital modulations, a narrow bandwidth amplifier is also used, which is not a serious weakness for the Doherty power amplifier. Another problem with Doherty amplifier is ant modality distortion which caused by the auxiliary amplifier low bias.

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