

## Investigation of the static current gain for InP/InGaAs single heterojunction bipolar transistor

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### ABSTRACT

Heterojunction Bipolar Transistors are being used increasingly in communication systems due to their electrical performances. They are considered as excellent electronic devices. This paper presents an investigation of the static current gain  $\beta$  based on two technological parameters related to the device geometry for InP/InGaAs Single Heterojunction Bipolar Transistor (SHBT). These parameters are the base width  $W_b$  and the emitter length  $L_e$ . We used Silvaco's TCAD tools to design the device structure, and to extract the static current gain  $\beta$  from I-V output characteristics figures. According to this investigation, we determined the optimal values of the examined parameters which allow obtaining the highest static current gain  $\beta$ .

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## 1. INTRODUCTION

Communication and information technologies had been developed thanks to the use of the semiconductor devices. Semiconductor materials of the group III-V are characterized by excellent properties, among them a direct bandgap and a high electronic mobility. Electronic devices based on III-V semiconductor materials can operate at high frequencies [1].

The transistor is a semiconductor device, and it was invented in 1947 by scientific researchers John Bardeen, William Shockley and Walter Brattain of Bell laboratories. It is considered as one of the greatest inventions of the 20<sup>th</sup> century. Transistors are outstanding devices for systems of communication which contain a high data rate, they are also used for applications which require high gain [2].

The heterojunction is defined as a junction between two layers with different gaps, and it is opposed to a homojunction. It was firstly proposed by William Schokley in 1951, the use of the heterojunction aims to improve the electrical performance of semiconductor devices [3].

Heterojunction bipolar transistors are made of not less than two different semiconductors. As a consequence, the energy bandgap can be different in the emitter, the base and the collector. Furthermore, inside each region a gradual change of the material can be done. It is not about an added complication, but the advantage of the heterojunction is allowing an additional degree of freedom, and this is found in vastly enhanced devices in comparison to the homojunction bipolar transistors [4].

In this context, Heterojunction Bipolar Transistors (HBTs) fabricated using semiconductor materials Indium Phosphide (InP) and Indium Gallium Arsenide (InGaAs) are excellent devices for microwave and high speed applications [5], [6]. The low width of InGaAs bandgap of base layer is the main cause of the

HBT's high frequency performance. In the base layer, there is a high mobility of electrons, and as a result electrons cross the base with very short times [6], [7].

For the static study of HBT, it can be characterized by the static current gain which is extracted from the  $I_c - V_{ce}$  figure. For AC parameters of HBT, they can be characterized by figures of merit such as maximum frequency of oscillation, cut-off frequency and emitter coupled logic gate delay [8].

The objective of this work is to investigate the impact of two technological parameters on the electrical performances of the InP/InGaAs SHBT in terms of the static current gain  $\beta$ . These parameters are: the base width  $W_b$ , and the emitter length  $L_e$ .

InP/InGaAs SHBT is composed of two alloys, a binary alloy for InP, and a ternary alloy for InGaAs. According to literature, the fabrication process of the InP/InGaAs SHBT was done in the past by using the Metal Organic Chemical Vapor Deposition (MOCVD) for the growth of the epitaxial layers, but after this technique the Molecular Jet Epitaxy (MBE) technique was used. MBE was considered better than MOCVD, because the materials of MBE are grown at lower temperature ( $\sim 450$  °C) in comparison to the materials of MOCVD ( $\sim 750$  °C), the temperature is an important parameter for the growth of layers, and it has an effect on the device performance [9].

For the Molecular Jet Epitaxy (MBE) technique, it is used on Fe-doped semi-insulating (100) InP substrates [10] and the growth low temperature of  $\sim 420$  °C, and it used stoichiometric conditions for both materials the Phosphide and the Arsenide [9].

## 2. THE PROPOSED METHOD

### 2.1 TCAD - Silvaco [11]

**Silvaco** (Silicon Valley Corporation) is a company that provides software tools which can be used for device process, device development, for analog/mixed-signal, power IC and memory design.

**TCAD** (Technology CAD or Technology Computer Aided Design) designates the use of computer simulations to improve and to optimize semiconductor processing technologies and devices.

Silvaco provides TCAD tools for various markets as power electronics, photonics, analog and HSIO design, library and memory design, advanced CMOS process and IP development, as shown in Figure 1.

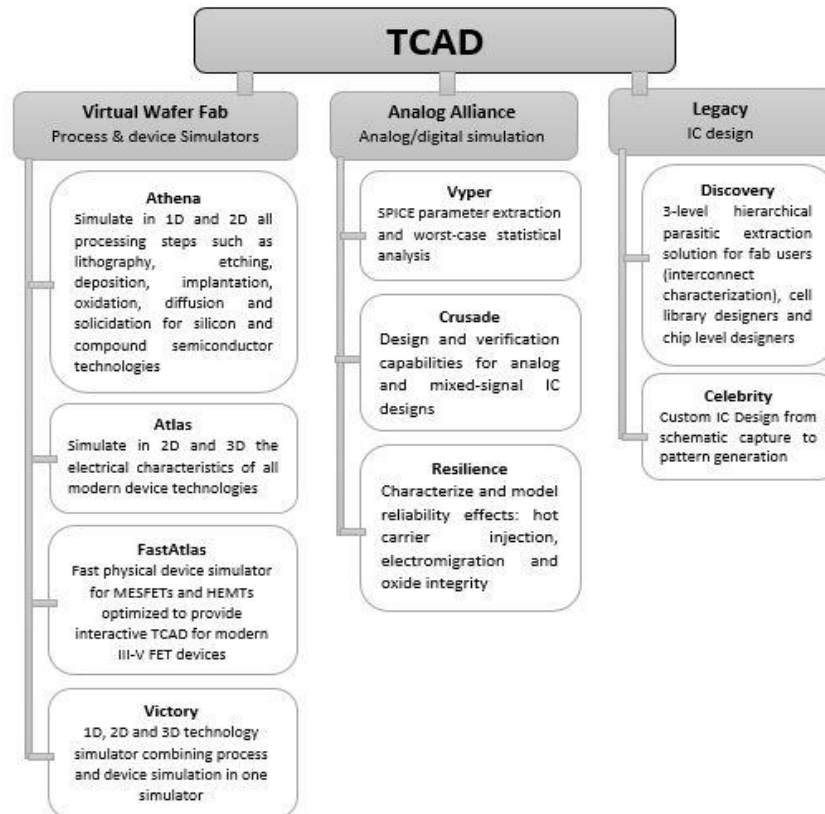


Figure 1. Silvaco's TCAD tools [11], [12]

## 2.2 Atlas [13]

Atlas is a two-dimensional modeling simulator which predicts the electrical characteristics of semiconductor devices under continuous, transient or frequency conditions. It is composed of two parts:

- 1) A digital processing part which contains the integration method, the discretization.
- 2) A part formed of the physical models occurring within semiconductor devices as the models of recombination, impact ionization, mobility, carrier statistics, tunneling.

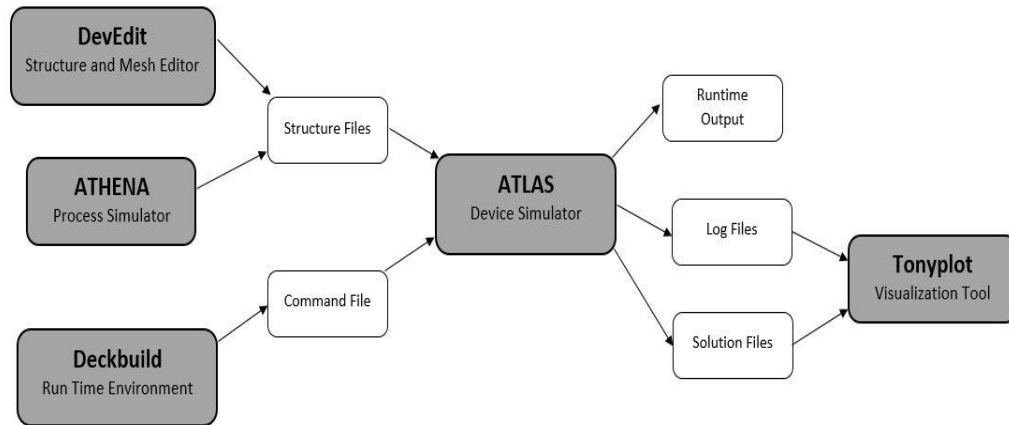


Figure 2. Atlas inputs and outputs [11]

As shown in the Figure 2, Atlas has inputs and outputs. It uses two types of input files: a command file that contains the commands of the simulator, and a structure file that defines the structure to be simulated. Atlas produces three types of output files: the runtime output which shows errors and warning messages as the simulation proceeds, the log file which stores voltages and currents, and the solution file which stores 2D and 3D data related to the solution variables values.

### Deckbuild [11]:

It is an interactive tool, it is considered the environment where the simulation program is defined through specific commands.

### DevEdit [14]:

It is the structure editing tool which allows the creation of new structures or the modification of the existing structures. The user can define meshes or refine the existing meshes.

### ATHENA [15]:

It is a process simulation tool which provides general possibilities for the simulation of processes used in the semiconductor industry: diffusion, oxidation, ion implantation, etching, lithography, deposition processes.

### Tonyplot [11]:

It is an environment where the simulation results are displayed (the device structure, the distributions of various quantities in it, or the electrical characteristics.)

## 2.3 Method for the Optimization of the Static Current Gain

To optimize the static current gain  $\beta$  of the studied electronic device, we propose to do the steps mentioned in the Figure 3. We started first of all by designing the studied device structure by the integration of material properties, thicknesses, doping profiles..., after that we modelled physically and numerically this device. We simulated the I-V electrical characteristics and we extracted the static current gain  $\beta$ . We then selected two technological parameters which are the base width  $W_b$  and the emitter length  $L_e$ , we then examined the impact of these parameters on the static current gain  $\beta$ . Afterwards, we determined the optimal values of these parameters which allow obtaining a higher static current gain in comparison to that of the first studied device. Finally, we defined an improved device. The details of these steps are found in the sections 3 and 4 of this paper.

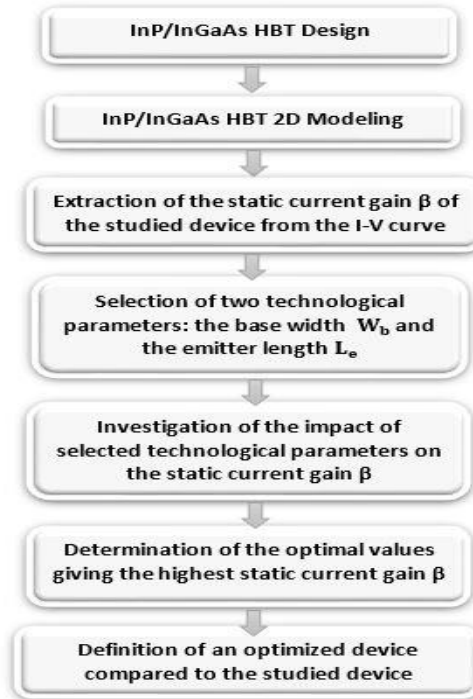


Figure 3. Proposed method to optimize the static current gain  $\beta$

### 3. 2D MODELLING FOR INP/INGAAS SHBT

#### 3.1 Device Structure Description

In this paper, the studied electronic device is principally based on papers [6], [16]. It is an NPN Single Heterojunction Bipolar Transistor. For its epitaxial layers, InP and InGaAs are used, the contacts are made from the material Gold.

The device structure is composed from the top of: n-In<sub>0.47</sub>Ga<sub>0.53</sub>As Cap layer (135 nm,  $n = 1 \times 10^{19} \text{ cm}^{-3}$ ), n-In<sub>0.47</sub>Ga<sub>0.53</sub>As Emitter 1 layer (135 nm,  $n = 1 \times 10^{17} \text{ cm}^{-3}$ ), n-InP Emitter 2 layer (40 nm,  $n = 1 \times 10^{17} \text{ cm}^{-3}$ ), In<sub>0.47</sub>Ga<sub>0.53</sub>As Spacer layer (5 nm, intrinsic), p-In<sub>0.47</sub>Ga<sub>0.53</sub>As Base layer (65 nm,  $p = 1.5 \times 10^{19} \text{ cm}^{-3}$ ), n-In<sub>0.47</sub>Ga<sub>0.53</sub>As Collector layer (630 nm,  $n = 1 \times 10^{16} \text{ cm}^{-3}$ ), n-In<sub>0.47</sub>Ga<sub>0.53</sub>As Sub-collector layer (500 nm,  $n = 1 \times 10^{19} \text{ cm}^{-3}$ ), In<sub>0.47</sub>Ga<sub>0.53</sub>As Buffer layer (10 nm, intrinsic). The emitter surface is equal to  $5 \times 5 \mu\text{m}^2$ . To design it, we used the structure editor DevEDIT [14].

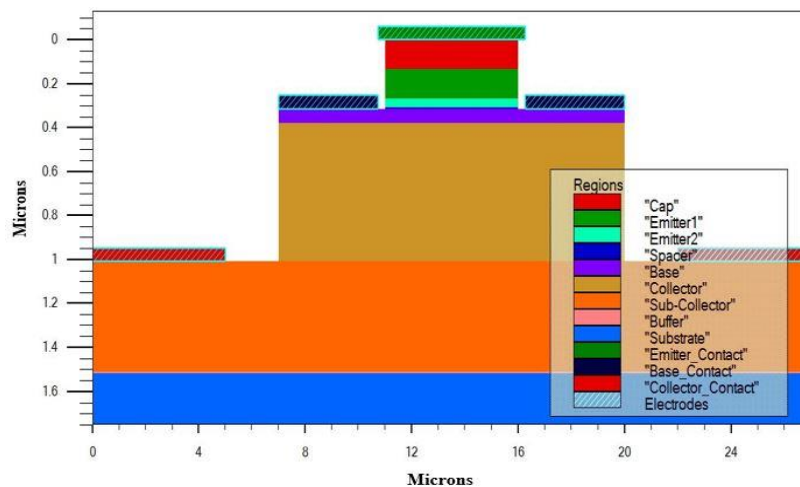


Figure 4. Illustrated epitaxial layers of InP/InGaAs SHBT

The Figure 4 shows the different regions of the studied device structure in two-dimensional illustration of the simulated InP/InGaAs SHBT in the interactive visualization tool Tonyplot. According to device geometry, this SHBT is symmetrical and it is composed of a single emitter contact, two base contacts and two collector contacts.

Figure 5 illustrates the different doping regions for each epitaxial layer of the InP/InGaAs SHBT. The net doping option of the simulator allows to show the doping regions p-type and n-type, and also the diffusions of the dopings for the intrinsic layers, as the spacer layer which is under the influence of the diffusion of the p-doped base region.

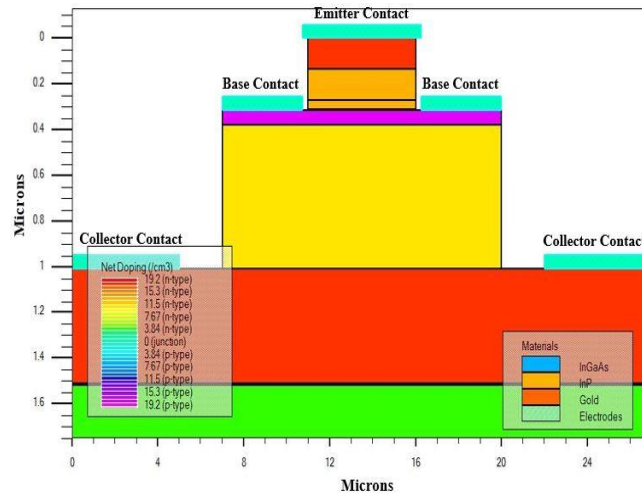


Figure 5. Simulated doping regions of InP/InGaAs SHBT

### 3.2 Integrated Physical Models for SHBT

In the simulation program, we have considered the doping effect on both of charge carriers the electrons and the holes. In each region of the device, the effective mobility of electrons and holes is defined by Caughey-Thomas equation as follows [16], [17]:

$$\mu = \mu_{\min} \left( \frac{T_L}{300} \right)^\beta + \frac{\mu_{\max} \left( \frac{T_L}{300} \right)^\delta - \mu_{\min} \left( \frac{T_L}{300} \right)^\beta}{1 + \left( \frac{T_L}{300} \right)^\gamma \left( \frac{N}{N_C} \right)^\alpha} \quad (1)$$

Where,

$\beta$ ,  $\delta$  and  $\gamma$  are the temperature dependent coefficients,  $T_L = 300$  K.

We added in the simulation the physical models [13] integrated inside the simulator. Among these models, we cite the carrier statistical model (BGN), the recombination model (SRH), the Selberherr's model of the impact of ionization (IMPACT SELB), the Tunnel effect model (BBT.STD), and the Optical model of recombination (OPTR)

**SRH Model (Shockley-Read-Hall):** it is an essential model of recombination, it allows the use of fixed lifetime of the minority carriers.

**OPTR model:** it is an optical recombination model, it is a band-band recombination. This model is only used for direct materials.

**BGN Model (Bandgap Narrowing):** it is a statistical model of the carriers. It is considered crucial in regions which are heavily doped, and also critical for the bipolar gain.

**Band-to-band model (BBT.STD):** it is considered as a part of tunnel models and carrier injection models. It is proposed for direct transitions with very high fields.

**Selberherr's model (IMPACT SELB):** it is the impact ionization model. It is suggested in the simulation for most cases. It integrates the parameters depending on the temperature.

### 3.3 Numerical Modelling

For the numerical modelling of the studied electronic device, the Newton method was used to solve numerically a serie of semiconductor equations in a mathematical model. The solved equations

as the Poisson's equation, the carrier continuity equations, the transport equations are more detailed in the paper [18].

#### 4. RESULTS AND DISCUSSION

Figures and tables below present the simulation results for InP/InGaAs SHBT at room temperature ( $T=300$  K). We simulated I-V output characteristics for the studied SHBT using the simulator TCAD to extract its static current gain  $\beta$ . We then evaluated the effect of two technological parameters, the base width  $W_b$  and the emitter length  $L_e$  on its electrical performance in terms of the static current gain  $\beta$ . Finally, we defined an optimized electronic device according to the investigated parameters giving the highest static current gain  $\beta$ .

##### 4.1 I-V Output Electrical Characteristics

The static current gain  $\beta$  of the SHBT is defined as follows [19]:

$$\beta \propto \frac{D_{nB}}{D_{pE}} \frac{L_{pE}}{W_B} \frac{N_{CB}}{N_{CE}} \frac{N_{VB}}{N_{VE}} \frac{N_D}{N_A} \exp\left(\frac{\Delta E_g}{KT}\right) \quad (2)$$

Where,

- $D_{nB}$  is the diffusion coefficient for electrons in the base, and  $D_{pE}$  is the diffusion coefficient for holes in the emitter,
- $L_{pE}$  is the diffusion length for holes in the emitter, and  $W_B$  is the base width,
- $N_{CB}$  and  $N_{CE}$  represent the conduction band density of states respectively for the base and emitter materials,
- $N_{VB}$  and  $N_{VE}$  represent the valence band density of states respectively for the base and emitter materials,
- $N_D$  and  $N_A$  are the doping concentrations respectively for the emitter and the base,
- $\Delta E_g$  is the energy bandgap difference of the emitter and the base materials,
- $K$  is the Boltzmann constant,
- $T$  is the Temperature in Kelvin (K).

Figure 6 presents I-V curve of the InP/InGaAs SHBT. The function  $I_c = f(V_{ce})$  was plotted for four values of  $I_b$ , 5  $\mu A$ , 10  $\mu A$ , 15  $\mu A$  and 20  $\mu A$ . An offset in turn-on voltage ( $V_{ce0}$ ) is observed when the voltage  $V_{ce}$  is varied from 0 to 2V, it is equal to 50 mV, it is because of the difference between the voltages of the base-emitter diode (heterojunction) and the base-collector diode (homojunction), this result is different from what is usually observed on silicon bipolar transistors. The static current gain is around 80.24.

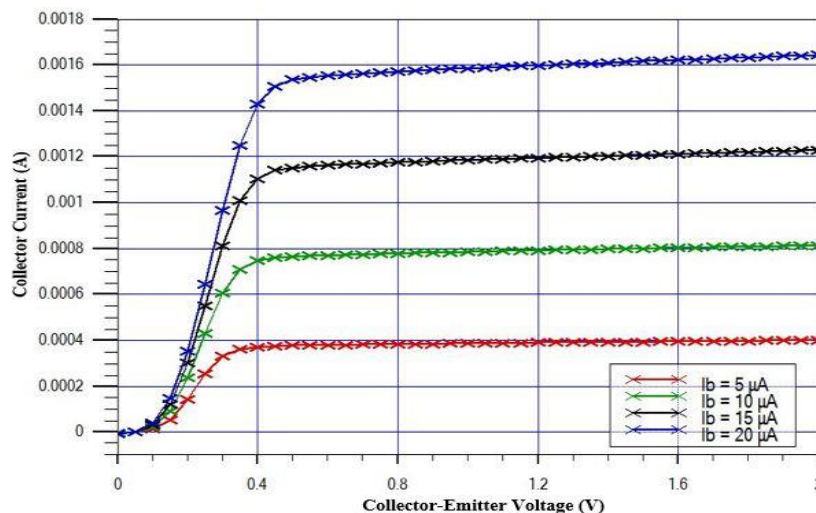


Figure 6. Simulation results for  $I_c$  -  $V_{ce}$  Characteristics of the InP/InGaAs SHBT

Through Figure 7, different values of base width were investigated, from 45 nm to 85 nm with a step equal to 10 nm. We observe that the base width  $W_b$  has a great impact on the static current gain  $\beta$ , because when we decrease the base width the static current gain increases.

Among the evaluated values, and in particular for a base width  $W_b$  equal to 45 nm, the static current gain  $\beta$  is around 197.33, and it is the highest gain obtained. Therefore, the optimal value for base width is 45 nm. The calculated improvement in comparison to the reference device is about 145.92%.

If we choose the base width equal to 45 nm, the device structure will be reduced in size. According to the state of art, smaller devices are required for various reasons, and semiconductor devices have over and over been scaled down in size. The work presented in the paper [20] had discussed scaling as a solution to improve and to optimize the performances of semiconductor devices.

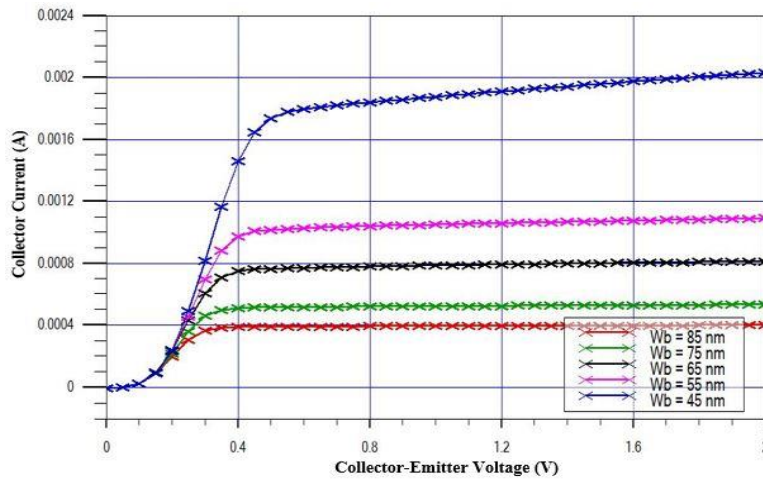


Figure 7. Output Characteristics  $I_c = f(V_{ce})$  for different base widths  $W_b$  at  $I_b = 10 \mu A$

Figure 8 presents an investigation of emitter length impact on the static current gain  $\beta$  at fixed current base  $I_b = 10 \mu A$ . According to the investigated values of emitter length  $L_e$ , from  $4 \mu m$  to  $7 \mu m$  with a step equal to  $1 \mu m$ , we observed that the static current gain increases slightly when we increase the emitter length. For an emitter length  $L_e$  equal to  $7 \mu m$ , the static current gain  $\beta$  is equal to 85.41, it is the highest current gain obtained for the examined values. Therefore, for the optimal value of  $L_e$ , the improvement in comparison to the reference device is equal to 6.44%. This improvement is slight, the parameter emitter length doesn't have a great effect on the static current gain.

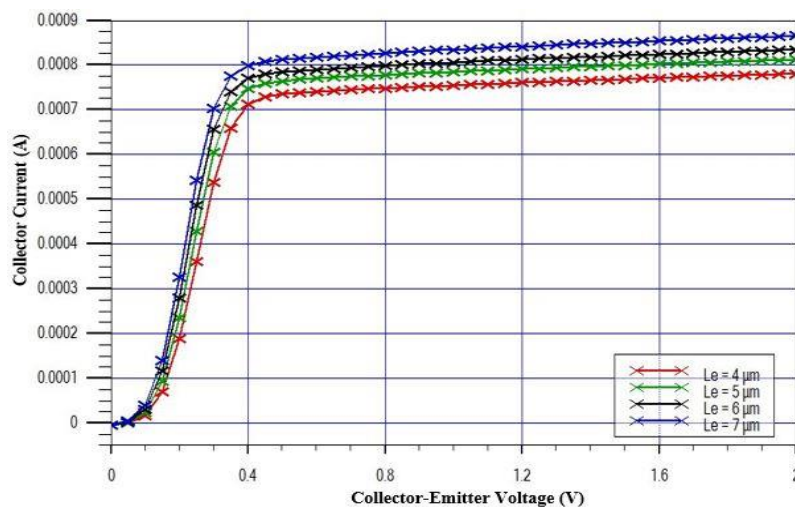


Figure 8. Output Characteristics  $I_c = f(V_{ce})$  for different emitter lengths  $L_e$  at  $I_b = 10 \mu A$

From the Figure 8, we have determined the optimal values of the investigated technological parameters in order to define an improved device which has the highest static current gain  $\beta$ . Afterwards, we simulated the optimized device for a base width equal to 45 nm, and an emitter length equal to 7  $\mu\text{m}$ .

Figure 9 shows the output characteristics for the optimized device. We plotted the function  $I_c = f(V_{ce})$  for four values of base current  $I_b$ . When  $V_{ce}$  is varied from 0 to 2V, we noticed that the offset in turn-on voltage ( $V_{ceo}$ ) is equal to 50 mV. According to the curve of the improved electronic device SHBT based on optimal values, we found that the static current gain  $\beta$  is around 207.18. The obtained gain is greater than that of the reference device, the improvement is about 158.20%.

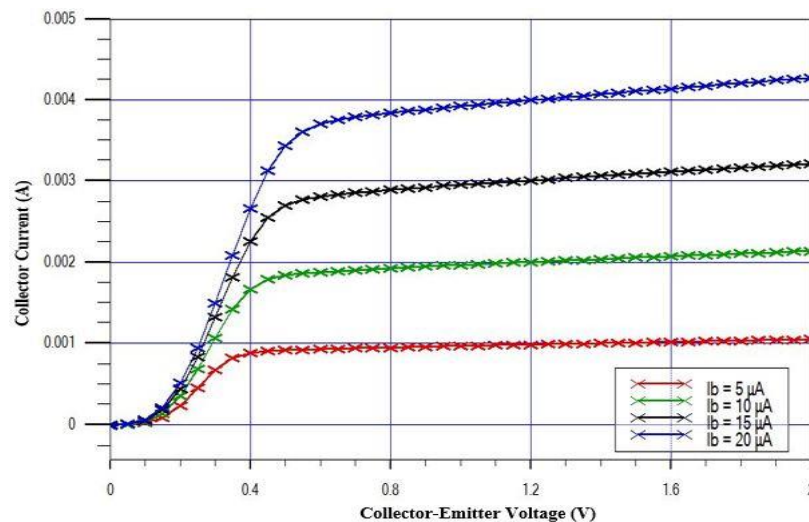


Figure 9. Output Characteristics  $I_c = f(V_{ce})$  for the optimized device SHBT

#### 4.2 Comparison with other work

Table 1 presents the comparison between our work without and after optimization and device performance in other research work [16].

Table 1. Comparison between the obtained gain and other work

Ref	$V_{ceo}$ (mV)	$I_b$ ( $\mu\text{A}$ )	$I_c$ (mA)	Current gain $\beta$ (A/A)
Other work [16]	150	10	0.90	90
Our work without optimization	50	10	0.8024	80.24
The proposed work after optimization	50	10	2.0718	207.18

According to the summarized results listed in the Table 1, we can observe that we reached a good electrical performance with the optimized device, because we obtained an important static current gain equal to 207.18 in comparison to the other work.

#### 5. CONCLUSION

In this present paper, a two-dimensional modelling was done for InP/InGaAs SHBT using Silvaco's TCAD tools. We added the physical models (SRH, BGN, BBT.STD....) in the simulation program to consider the physical mechanisms and phenomena happening within the electronic device. For the numerical modelling, Newton method was integrated. Firstly, we simulated I-V output characteristics of the reference device in order to determine its static current gain  $\beta$ , we found that it is equal to 80.24. Secondly, we evaluated the effect of two technological parameters, the base width  $W_b$  and the emitter length  $L_e$  of the studied device on its static current gain  $\beta$ . Finally, we simulated an optimized device based on the optimal values of the investigated parameters giving the highest current gain  $\beta$ , in particular for a base width equal to 45 nm and an



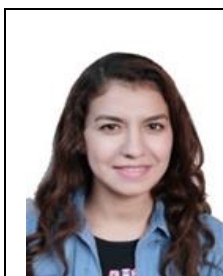
emitter length equal to 7  $\mu\text{m}$ . The improved device has a static current gain equal to 207.18, it is greater than that of the reference device which is equal to 80.24, and the improvement is around 158.20%.

For our future investigation, we intend to evaluate the doping concentration of critical regions of this electronic device, and to extend this study for AC parameters.

## REFERENCES

- [1] T Gonzalez Sanchez, J E Velazquez Pérez, P M Gutiérrez Conde and D Pardo Collantes, "Electron trans Berrichi Yamina, Ghaffour Kherreddine," Modelling Electronic Characteristic port in InP under high electric field conditions", *IOP science*, pp.31-36, 1992.
- [3] Rashmi Singh, Rajesh Mehra, " Qualitative Analysis of Darlington Feedback Amplifier at 45nm Technology," *Bulletin of Electrical Engineering and Informatics*, Vol. 7, No. 1, pp. 21-27, 2018.
- [4] Bart Van Zeghbroeck, e-book "Principles of electronic devices", University of colorado (2007).
- [5] C. H. Li, H. L. Lu, Y. M. Zhang, M. Liu, and X. H. Zhao, "Proton-Induced Degradation of InP/InGaAs HBTs Predicted by Nonionizing Energy Loss Model", *IEEE Transactions On Nuclear Science*, VOL. 62, NO. 3, pp.1336-1340, JUNE 2015.
- [6] J.Sexton and M.Missous, "Annealing Experiments On Inp/Ingaas Single And Double Hbts Grown By Molecular Beam Epitaxy", in *Electron Devices for Microwave and Optoelectronic Applications.EDMO 2002.The 10<sup>th</sup> IEEE International Symposium on*, pp.300-305, 2002.
- [7] Subhra Chowdhury and Sukla Basu, "Analytical Modelling of Base Transit Time and Early Voltage of InP/InGaAs Heterojunction Bipolar Transistor for Nonuniform Base Doping Profile", *Proceeding of the 2011 IEEE Students' Technology Symposium*, IIT Kharagpur, 14-16 January 2011.
- [8] Engelin Shintadewi Julian, "Silicon Germanium Heterojunction Bipolar Transistor for Digital Application," *TELKOMNIKA*, Vol.10, No.3, pp. 493-498, September 2012.
- [9] M. Missous, "Optical and electrical properties of InO.48(AlxGa(1-x))0.52P grown by Solid Source MBE using a GaP Decomposition Source," *EDMO 2001*, (Cat. No. 01TH8567). IEEE, pp. 1-8, 2001.
- [10] J. Sexton, T. Tauqeer, M. Mohiuddin and M. Missous, "GHz Class Low-Power Flash ADC for Broadband Communications," *ASDAM 2008, The Seventh International Conference on Advanced Semiconductor Devices and Microsystems*, October 12-16, 2008, Smolenice Castle, Slovakia, pp. 235-238.
- [11] www.silvaco.com
- [12] P. Michalopoulos, "A novel approach for the development and optimization of state-of-the-art photovoltaic devices using Silvaco," M.S. Thesis, Naval Postgraduate School, Monterey, California, March 2002.
- [13] ATLAS User's Manual, Device Simulation Software, Silvaco International, September 3, 2010.
- [14] DevEdit User's Manual, SILVACO INTERNATIONAL, 2006.
- [15] ATHENA User's Manual, 2d Process Simulation Software, Silvaco International, July 20, 2005.
- [16] T. Tauqeer, J. Sexton, F. Amir and M. Missous, "Two-Dimensional Physical and Numerical Modelling of InP-based Heterojunction Bipolar Transistors", in the *7<sup>th</sup> International Conference on Advanced Semiconductor Devices and Microsystems*, 12-16 Oct. 2008, pp.271-274.
- [17] Caughey DM, Thomas R E. Proc IEEE; 52; 2192; 1967.
- [18] Jean-Luc Polleux, Member, IEEE, Laurent Paszkiewicz, Anne-Laure Billabert, Member, IEEE, Jacques Salset, and Christian Rumelhard, Fellow, IEEE, "Optimization of InP-InGaAs HPT Gain: Design Of An Opto-Microwave Monolithic Amplifier", *IEEE Transactions On Microwave Theory And Techniques*, Vol. 52, No. 3, March 2004, pp. 871-881.
- [19] Jean-Christophe MARTIN, "Etude des mécanismes de dégradation des Transistors Bipolaires à Hétérojonction sur substrat InP destinés aux communications optiques", *University of Bordeaux I*, Ph.D Thesis, 2004.
- [20] Engelin Shintadewi Julian, Rudy S. Wahjudi, " Scaling Model for Silicon Germanium Heterojunction Bipolar Transistors, " *TELKOMNIKA Indonesian Journal of Electrical Engineering*, Vol. 14, No. 1, pp. 103 – 109, April 2015.

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