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Side Effects in a HEMT Performance with InAlN/GaN

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Abstract

We present a simulation of a HEMT (high electron mobility transistor) structure. We extract the device characteristics through the analysis of DC, AC and high frequency regimes, as shown in this paper. This work demonstrates the optimal device with a gate length of 30 nm, and InAlN/GaN heterostructure for minimizing side effects. The simulated with Silvaco software of the HEMT devices with the materials InAlN show very good scalability in different application. We have demonstrated an excellent current density, as high as 644 mA/mm, a peak extrinsic transconductance of 710 mS/mm at V_{DS}=2 V, and cutting frequency cutoffs of 385 GHZ, maximum frequency of 810 GHz, maximum efficiency of 23% for x-Band, maximum breakdown voltage of 365 V, and an ON/OFF current density ratio higher than 8 x 10^8. These values were determined through the simulation by hydrodynamics models, which makes that optimize the design is the future of this technology.

Keyword: *HEMT, InAlN/GaN, silvaco, side effect, power electronics devices, semiconductors devices*

1. Introduction

Devices HEMT is considered nowadays as being excellent models is allowing studying fundamental physics, technology and understanding function electrical performance resulting to support the development of simulators that would allow us to chart the future of this technology. With high mobility and high saturation velocity they are useful for high frequency and low power consuming applications [1].

And InAlN is a new material used today for potential successor to AlGaN [2]. It takes advantage of the interesting material properties of the III-nitrides, such as a wide band gap, high breakdown electric field and excellent thermal conductivity, conduction interface.

Consequently, there is still room for improvement of InAlN/GaN HEMT power performance. Indeed, InAlN/GaN transistors can have a sheet carrier density twice higher than that of conventional AlGaN/GaN HEMTs, enabling the use of a thinner barrier layer while keeping a high sheet carrier concentration at the heterointerface [3].

More recently, HEMTs on an InAlN/GaN material structure to demonstrate superior performance and constitute an alternative to commercially available AlGaN/GaN devices, since it particularly for the trend in the semiconductor industry is to reduce the size of the device for better speed performance. But as the gate size reduced, we have either in the short channel or for hot electron effects and poor carrier transport efficiency creep are contained. As a result it becomes utmost important to find solutions for these problems for more speed and less power consumption [4].

However, aside from keeping the parasitic low in device, it is imperative to improve the intrinsic gm in ultra scaled devices with the best possible electrostatic control, which can be potentially realized in quantum-well InAlN/GaN/AlN structures [5].

In this work, we have demonstrated a HEMT InAlN / GaN is possible to produce excellent properties with the best possible while minimizing side effects. Through the optimization of the device design and quality control of doping implant, even if the adoption of several analytical models to simulate the devices highly scaled analysis characteristics [6-7], deep level dopant such as AlN is also intentionally used in the buffer [8-9], to reduce the effect of buffer traps on the 2-DEG transport behavior [10], in order to intentionally underestimate phenomena unwanted until they become almost negligible to suppress buffer leakage and these effects.

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A hydrodynamic model approach must be used to deliver accurate results for such structures [11-12]. We propose this model that accounts for the peculiarities of the GaN material system. The models are implemented in our Silvaco simulation and carefully calibrated. A device from a recent generation of transistors was simulated using the ATLAS calibrated setup [1315]. A high accuracy for all relevant characteristics was achieved.

2. Structure of Device

As illustrated in Figure 1(a), we see a cross section of the structure, it is located over the layer of substrate (4H-SiC), we find that the color blue region corresponds to the electrodes (i.e. the source, drain and gate), the color brown corresponds to layers of the channel and cap layer, the color red corresponds to layers of a donor and Schottky, the buffer and spacer layers corresponds to green color and finally yellow color regions correspond to thesubstrate. And the performance simulation of this device is realized by Silvaco. We use two steps for simulated this device and the process sequence is as follows:

a) The first step focused to create a structure in the framework DevEdit.
b) The second step focuses to analyze this structure in the framework Atlas system.

The device contact Schottky used Gold "Au" for T-gate electrode. Then, source/drain electrodes were formed by "Au" (250 nm) is chosen for ohmic contacts, the device design features a heterostructure InAlN/GaN, where the periphery oxide Al_2O_3 of the Gate is a difference with conventional designs [13], and the SiN passivation dielectric that minimizes surface leakage and creates a high density of shallow traps at the surface [16].

As a result, after a doping cap layer is eliminated leakage current density in the device, and This gives rise to a conduction band shape for the barrier that in an InAlN barrier is undoped [17], the same sheet carrier concentration based on the model Fujitsu [14], the Hall mobility and sheet carrier concentration were 1300 cm^2 V^{-1} s^{-1} and 1 × 10^{13} cm^{-2}. The heterojunction features a sheet charge density of 1.85x 10^{13} cm^2. Dimensions are also a critical parameter for device performance, while we find the different dimensions of the device under study is included in Table 1.

Table 1. Parameter HEMT device

Name	Symbole	Valeur [nm]
Thickness Cap Layer	E_{OH}	3
Thickness Layer Schottky	E_S	7
Thickness Layer Donor	E_D	3
Thickness Layer Spacer	E_E	1
Thickness Canal Layer	E_C	37
Thickness Tampon Layer	E_T	150
Thickness of Bulk	E_B	100 10^3
Length Drain Gate	L_{DG}	1.47 10^3
Length Gate Source	L_{GS}	0.50 10^3
Length Gate	L_G	30
Length Drain & Source	L_D	0.5 10^3

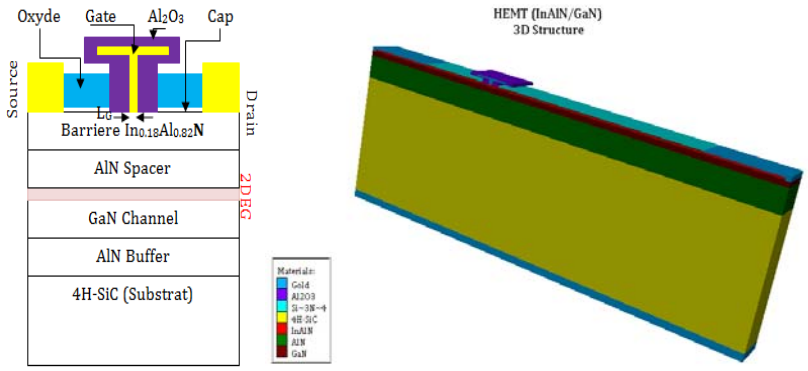

Figure 1. Device and schematic diagram of a HEMT device simulated.

3. Simulation Results

Simulate the structure with the same dimensions and parameters has been selected, or when a device (geometries, meshes, regions, electrodes and doping) consistent distribution are described with the same sequence of states, also in the material parameters and models physical are applied in overall at cases. But in the case of specifying the effect of the avalanche or KINK with the impact ionization model generation, will be demonstrated these effects located in the next of this work.

3.1. DC Results

After the definition of the HEMT structure and materials used for model, the initial solution is obtained from the gate voltage set to zero, the structure under zero bias (the initial case reported for supply voltages), and the solutions are obtained from the choices specified in the algorithm, to obtaining a depth characterization from the simulation. Accurate simulation results can be obtained by solving Hydrodynamics model physics for simulation the analyze device performance [18], The device temperature is not at all constant especially at the gate exit in the reality for that the simulation has been begin 300K and this value is higher with time the simulation for that Giga should be used to simulate the heat-flow in the device [19].

In this device simulation, the electrical transfer characteristics are illustrated in Figure 2(a). For the HEMTs with a gate length of 30 nm, short-channel effects are apparent not only from the large threshold voltage shifts but also from the high output conductance in both highly scaled Ga-polar HEMTs [20].

The increasingly positive drain voltage led to the electric field across the channel increasing the speed of the electron. The voltage distribution across the canal led to a voltage difference between the gate and the channel along it, with the transistor demonstrating a variable resistance behavior controlled by the gate voltage. This indicates excellent gate control of the 2DEG channel [21], and the maximum drain current available reached 644 mA/mm when V_{GS} was biased at 0.5 V & V_{DS}=2.0 V. The pinch-off voltage was found to be −1.0 V, as shown in Figure 2(a).

Figure 2(b) presents the extrinsic transconductance (g_m) characteristics of the device, where the simulation is extracted displays a maximum peak g_m as 710 mS/mm at V_{DS}=2.0 V. This peak appears in the curve of the transconductance as a dependence on the gate bias V_{GS}. This obviously reflects the DC behavior of the simulated HEMT, which correspond to the 2DEG channels modulated by different gate voltages. These properties are superior to the values previously reported for similar structures based on AlGaN/GaN heterostructures [22].

Here, a better DC characteristic is realized on a sample with slightly inferior electrical properties in comparison with those reported earlier [23]. The total parasitic resistance is generally dominated by a low Ohmic contact resistance, which is highly desirable, and could be attributed to the increased carrier concentration or/and an increased carrier mobility [24].

The device is delivered to extract an ON/OFF current density ratio higher than 8×10^8 (with range V_{GS} between -10V to 1.0V), leakage current density off-state $I_F=9 \times 10^{-26}$ A/m, and we have investigated the conduction band profiles to calculate that the drain-induced barrier lowering (DIBL) is more explicit in a highly scaled device at the gate length 30 nm when DIBL=168.38 mV/V with V_{DS} fixed between 0.1 V and V_{DD}. The effects that were observed due to this gate length are called short-channel effects (SCE). Effects occurring at a larger V_{DS} are termed drain induced barrier lowering (DIBL) effects [25], as shown in Figure 2(d), we are not the first to observe this in simulations for HEMTs, as they were investigated as early as 1989 by Awano, et al. [26]. We have the possibility to achieve the reduction of these phenomena with the engineering of dynamically active interface states [27].

We changed the acceleration of the drain voltage between 0 V to 3 V, when the simulation was first conducted to obtain the I-V characteristic in the DC mode to change the state of the gate voltage by 5 different bias values, V_{GS} = 0.2 V to – 0.8 V with a step of -0.2 V. The device R_{ON} extracted at V_{GS} = 0 V and V_{DS} in the range between 0 and 1.0 V is 0.354 Ω ·mm, the I-V characteristics show good pinch-off characteristic and the current collapse phenomenon was might ultimately limit the scalability of the device and it is too low compared to usual values obtained if we compared with others work simulation because the barrier layer is very thin for minimizing pinch-off these very important in logical electronics application, and because model used in this work is hydrodynamics.

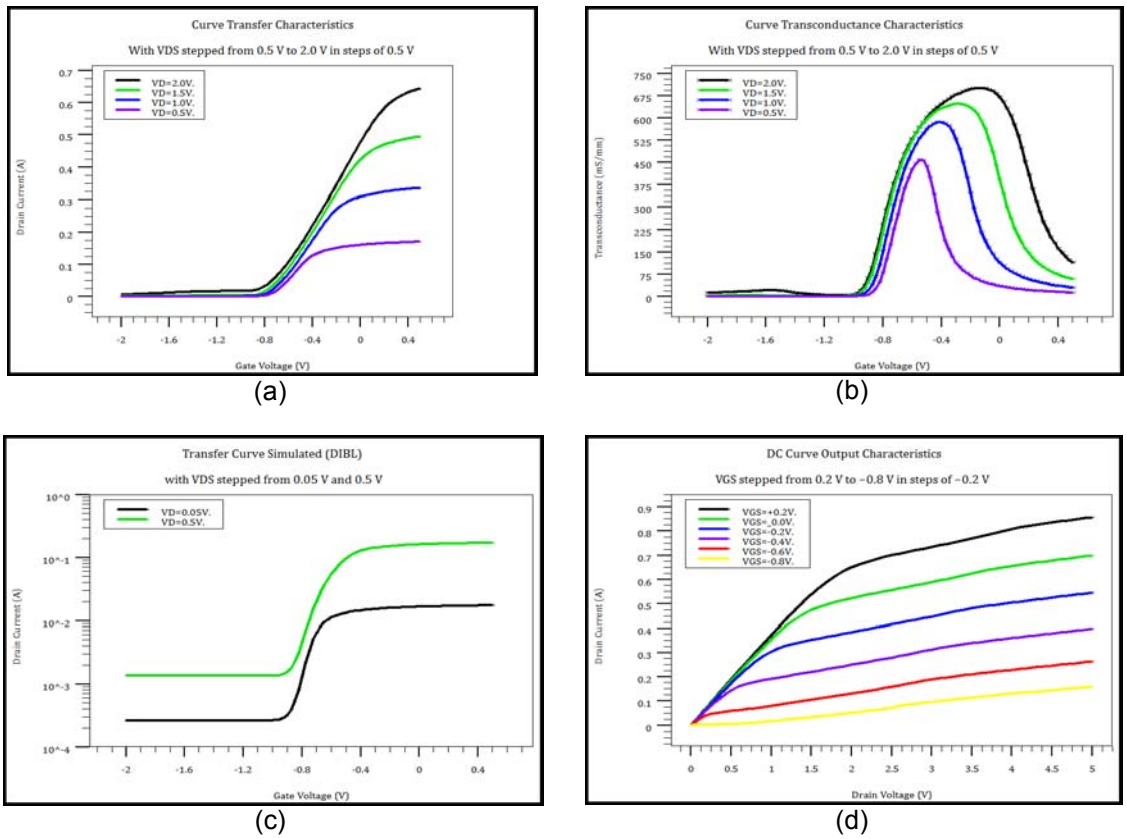

Figure 2. (a) Transfer curve simulated with V_{DS} stepped from 0.5 V to 2.0 V in steps of 0.5 V and V_{GS} sweeping from 1 V to −10 V, (b) Transconductance characteristics of HEMT InAlN/GaN with a gate length of 30 nm with V_{DS} stepped from 1.0 V to 2.0 V in steps of 0.5 V. (c) Transfer curve simulated with V_{DS} stepped from 0.05 V and 0.5 V and (d) DC Output characteristics of HEMT InAlN/GaN with a gate length of 30 nm with V_{GS} stepped from 0.2 V to −0.8 V in steps of −0.2 V

3.2. Side Effect

The operation of the power field effect transistors is substantially limited on one hand by the conduction current of the diode and the other gate voltage by the avalanche phenomenon. In field effect devices, two types of breakdown voltage can be highlighted: breakdown by Kink effect and impact ionization [28-30], this type of simulation is very difficult for the effect of KINK therefore defining of the impact such Selberherr impact ionization models [19] has been measured and modeled extensively at room temperature. Recently, Valdinoci and al. has extended the simulated temperature range to 400K and has developed a compact model for both electron and holes mobility impact ionization.

In order to simulate avalanche breakdown, the impact ionization-generation model should be turned on. This is done using the impact Selb statement in which the Selberherr impact ionization model is activated, Here the beam statement is used to specify an optical source of carrier pair generation in addition to the thermal generation provided by recombination SRH.

Most device simulators of the lattice temperature variations within a structure must be taken into account. It is based on this work on the model of Wachutka [31] and includes all thermal sources and sinks (Joule heat, Thomson term, etc.). Successful thermal modeling requires appropriate boundary conditions to be specified.

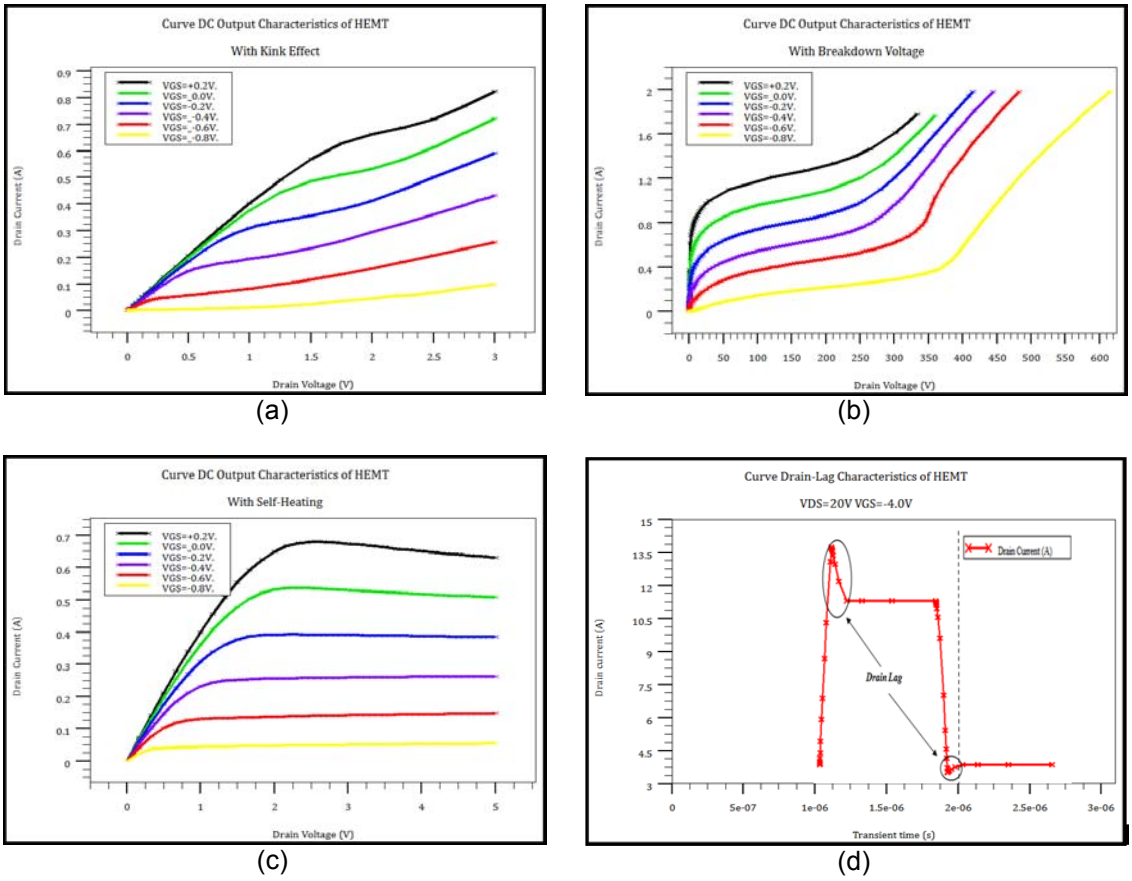

Figure 3. Output characteristics of the 30 nm length gate InAlN/GaN HEMT with (a) Kink effect, (b) Breakdown effect & (c) Self-heating & (d) Voltage V_{GS} = constant = -4V with a pulse width of 0.1μs and a pulse period of 0.2 μs

Figure 3(a) shows the output characteristics of an HEMT with LG of 30 nm with Kink effect for temperature ambient. The device exhibits the variation of drain current with drain voltage shows a rise after stress with abrupt growth in current at different of a V_{GS} voltage, indicating existence of the traps in device. Therefore, the enhancement of the kink effect is probably due to the traps activated in the InAlN barrier layer, which is a sharp increase in the drain current at a certain voltage, thus causing an increase of the output conductance and the dispersion between DC and other characteristics. The kink effect also increases noise in excess of the low frequency component [32]. Indeed, as the output conductance is fluctuating over a range of V_{DS}, the conductivity will fluctuate under the influence of de-trapping, and therefore the noise at low frequencies 1 / f will tend to increase. This effect has often been attributed to impact ionization [33-34], resulting in an accumulation of holes amending surface potentials or channel / substrate interface.

The open squares indicate the critical drain voltage (V_{kink}) at which the output conductance is the maximum in the kink region. Vkink increases regular especially with the gate bias, suggesting that the de-trapping process is directly related to V_{GD} (i. e. the electric field) and is field-assisted in nature and it is suggested that this kink could be induced by hot electron trapping and field-assisted de-trapping via donor-like traps in the GaN buffer layer [35].

The off-state I_{DS}–V_{DS} characteristics or breakdown voltage of conventional InAlN/GaN HEMTs with a wide drain bias region of the gate voltage between –0.8 V and 0.2V are shown in Figure 3(b).

The conventional HEMTs demonstrate the off-state breakdown voltages of 250 and 375 V, respectively, which indicate that the breakdown characteristic of the HEMT device with an AlN buffer layer has been significantly improved in this device. It is believed that enhancement of the off-state breakdown voltage of the HEMT device is attributed to a better carrier

confinement and the increased back-barrier height of the AlN buffer layer used suppresses the spillover of the 2DEG into the buffer layer and postpones the punch through of the buffer layer, thus reducing the subthreshold drain leakage current and increasing the breakdown voltage remarkably.

The punch through of the electrons into the buffer layer causes a rapid increase of the drain leakage current and the device breakdown occurs when the drain leakage current exceeds a certain value [36], such as 400 mA/mm in V_{GS}=-0.8 for example.

As mentioned above, the electrons spilling over from the channel to the buffer layer at a higher drain supply voltage can from the buffer leakage current. In many cases, breakdown in GaN-based HEMTs is initiated by the electron current underneath the depletion region of the gate through the insulating buffer layer and is known as the buffer-layer punch through effect [37], the drain current change in I_{DS} for the remarkable kink is maximum near the pinchoff of the device and reduces with the decline in the gate voltage.

This phenomenon leads to substantially reduced carrier mobility, increased threshold voltage and a drop in conductance for the gate voltages and drain important. The gain was one of the top priorities, because gain affects the efficiency and the consumption power of the device.

The Self-heating effect is related to many different phenomena like to the presence of surface traps in the semiconductor, the increasing passivation layer thickness and type of passivation material strongly influence on hot spot temperature [38] and The tunneling and leakage current mechanisms can significantly contribute to surface trapped charge modulation [39], especially at high drain-gate bias [40-42], see Figure 3©. The electrons flowing in the channel are accelerated by the electric field. If the latter is sufficiently high, the electrons in the atoms of the crystal percussive free pair of electron holes. The holes are collected by the gate electrode and electrons by the drain electrode. This kind of avalanche can cause light emission.

At low temperatures, the electron mobility increases due to a reduction in the dispersion of polar optical phonons [34]. Pitfalls in question located under the grid, especially in the drain region side due to dissipation Joule electric power. The term "drain Lag" is used to describe the transient drain current when the drain voltage is pulsed from OFF (V_{DS} = 0V) to ON (V_{DS}> 0V) for a constant gate voltage [43]. There is then a decrease of the current I during this pulse if it is sufficiently long. The occupancy rates of the traps only depend of a V_{DS}.

We note in Figure 3(d) the transient behavior of the drain current thus indicating the presence of the phenomenon of drain Lag. As Zhang [44] suggests that the reduction of the output current in the GaN transistors during application of a pulse voltage at the drain is due to injection of electrons into the buffer layer where they are trapped.

When the drain voltage changes from the OFF state to the ON state, ie for a positive change in V_{DS}, electrons are accelerated by the electric field generated by V_{DS}. They are captured by traps deep localized energy levels within the buffer and / or the substrate, provided that the pulse duration is greater than the time constant of capture, and smaller than the time constant of emission. These electrons captured by the traps do not participate in the current channel. The direct result is the reduction of the drain current until it reaches its steady state, as and when the traps are filled.

$$D_{Lag} = \frac{I_{Dss} - I_{Dss0}}{I_{Dss}} * 100 \quad (1)$$

The device has excellent characteristics for calculating the drain obtained by simulation of 3.33%, we can say so device is more stable and better, however, after analyzing the current delay is more pronounced when the trailing edge of the pulse drain current establishment at high and low field drain.

3.3. AC Results

Shows in Figure 4, gain the current (H_{21}), maximum transducer gain power (GMT), stable maximum gain power (GMS), available maximum gain power (GMA) and unilateral gain power of the HEMT with L_G of 30 nm a**t** V_{DS} = 5 V and V_{GS} = 0.0 V versus frequency [1KHz-1THZ].

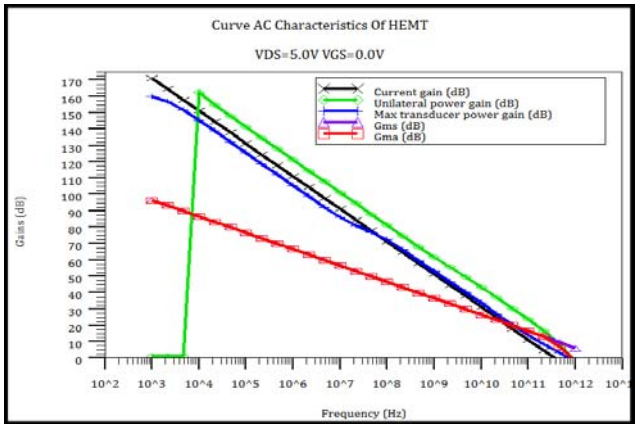

Figure 4. Simulated of the Gains current gain (H_{21}), Unilateral power gain (U) and max transducer power gain (MTG) versus frequency for the 30nm InAlN/GaN HEMTs. The bias condition were V_{DS}= 5.0 V and V_{GS}= 0.0 V from S-parameter simulations from a small-signal model

In this simulation, the maximum gain shown for the current H_{21} is 55 dB, the maximum transducer gain of power is 60 dB and the maximum stable gain of power is 40 dB at 1 GHz.

These result values were extracted from the extrinsic S-parameters and were then used to verify the intrinsic values of this device by simulation. The electronic transfer in the channel is optimized due to the effect of the capacitances of the high values of the gate to source capacitance (C_{GS}), which result from the extended effective gate length [45], the electronic transfer in the channel is optimized. We have extracted the cutoff frequency is 385 GHz and the value of the maximum frequency is 810 GHz extract in slope 0 dB/Dec. For comparison, the highest ft reported so far in nitride transistors was 370 GHz in 4-nm barrier InAlN/GaN HEMTs with 30-nm gate length [46].

3.4. RF Results

In small signal RF measurements the HEMT with gate width of 0.03 × 125 μm (30 nm × 100 μm) are used. This simulate typical 10 GHz large signal simulated performance quantities related to power output, we have generated plots the output signal shape versus time for each of the ten input signal levels simulated. Ten large signal input amplitudes are defined using WAVEFORM statements. Each of these waveforms is applied to the gate in order of increasing amplitude [47].

Show the output power (Pout), power-added efficiency (PAE) and gain power (GP) versus the broadband RF performance over the 9-11 GHz frequency range at a drain voltage of 30 V, gate voltage -2 V and input power of 16 dBm. The device was optimized for the PAE-matched condition X-Band; the simulated output power reached 32 dBm with 15.1 dB linear gain and 22% of maximum PAE of associated gain at 9 GHz.

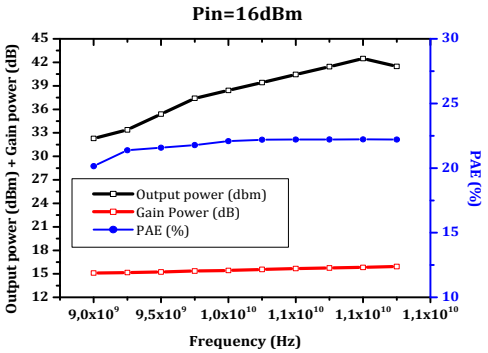

Figure 5. Power Output, Gains power and PAE for HEMT InAlN/GaN

Compared with reported results of X-band HEMT power delivers a maximum output power of 45.5 dBm (35.8W) with 39.5% of PAE and 13.5 dB of associated gain at 9.5 GHz [48]. Continuous-wave power measurements in class "A" operation at 10 GHz with V_{DS} = 15 V revealed a 19-dB linear gain, a maximum output power density of 2.5 W/mm with an ~23% power-added efficiency (PAE), and a 9 dB large-signal gain [49].

4. Conclusion

An InAlN/GaN HEMT device with 30 nm length gate design on SiC substrate is developed. Show that the performances of the device are strongly dependent on minimizing side effect, indicating that improving operating different adverse phenomena is key to achieve higher results, we have used the periphery oxide of the gate and optimal structures for minimized that.

These devices exhibited current density as high as 644 mA/mm, a peak extrinsic transconductance of 710 mS/mm at V_{DS}=2 V, and a cutoff of 385 GHz. The maximum frequency was 810 GHz, with a maximum efficiency of 23%, maximum breakdown voltage 365 V, DIBL=168.38 mV/V and ON/OFF current ratio higher than 8x 10^8. This paper demonstrates the great interest of GaN technology for different applications with adverse effect that accompanies run of the device.

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