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Assessment of Equal and Unequal Amplitude Carriers for a 1Φ Five Level Flying Capacitor Multilevel Inverter

P.Sureshpandiarajan, S.P.Natarajan*, C.R.Balamurugan, K.Ramasamy
P.S.R Rengasamy College of Engineering for Women, Sivakasi, India
*Corresponding author, e-mail: spn_annamalai@rediffmail.com

Abstract

This work presents the comparison of various Pulse Width Modulation (PWM) techniques for the chosen single phase half bridge FCMLI (Flying Capacitor Multi Level Inverter). In this paper, a single phase half bridge flying capacitor multilevel inverter is controlled with sinusoidal, THI (Third Harmonic Injection), Trapezoidal and TAR (Trapezoidal Amalgamated Reference) reference with Equal Amplitude Carriers (EAC) and UEAC (Un Equal Amplitude Carriers). The proposed EAC and UEAC is applied for various PWM strategies. The PWM methods used for the analysis are PD (Phase Disposition) PWM, POD (Phase Opposition and Disposition) PWM, APOD (Alternative Phase Opposition and Disposition) PWM and CO (Carrier Overlapping) PWM with EAC and UEAC. For all the PWM methods and references the UEAC produces less THD and higher fundamental RMS (Root Mean Square) values except for m_a =1. For m_a =1 the EAC provides less THD (Total Harmonic Distortion) and higher fundamental RMS (Root Mean Square) values for all the PWM methods and references. To validate the developed technique, simulations are carried out through Power System Block Set.

Keywords*: VAPWM, 60 degree PWM, TAR, THD, FCMLI.*

1. Introduction

FCMLI is a multiple voltage level inverter topology which uses capacitors (called flying capacitors) for clamping the voltage across the power semiconductor devices. DCMLI has much difficulty beyond four levels in output voltage in controlling or balancing voltage of each capacitor constituting DC-link. DCMLI is hard to be expanded to high level systems structurally due to large number of clamping diodes. FCMLI does not require isolated DC sources and additional clamping diodes. FCMLI topology can be easily expanded to high level systems. FCMLI offers also a great advantage with respect to the availability of voltage redundancies. On the other hand FCMLI has a drawback due to the need for providing additional flying capacitors and balancing control of flying capacitor voltages. Various multi-carrier PWM strategies are developed and simulated using MATLAB-SIMULINK for chosen three phase FCMLI. Chiasson [1] proposed the method to eliminate harmonics in a switching converter is considered. That is, given a desired fundamental output voltage, the problem is to find the switching times (angles) that produce the fundamental while not generating specifically chosen harmonics. In contrast to the well known work of Patel and Hoft and others, here all possible solutions to the problem are found. This is done by first converting the transcendental equations that specify the harmonic elimination problem into an equivalent set of polynomial equations. Juan and Moran [2] focussed on minimizing the number of power supplies and semiconductors for a given number of levels. Multilevel inverters with a large number of steps (more than 50 levels) can generate high quality voltage waveforms, good enough to be considered as suitable voltage template generators. Many levels or steps can follow a voltage reference with accuracy, and with the advantage that the generated voltage can be modulated in amplitude instead of pulse-width modulation. The main disadvantage of this type of topology is the large number of power supplies and semiconductors required to obtain these multistep voltage waveforms. Wells et al [3] suggested calculating easily and quickly the desired waveform without solution of coupled transcendental equations. A modulation-based method for generating pulse waveforms with selective harmonic elimination is proposed. Harmonic elimination, traditionally digital, is shown to be achievable by comparison of a sine wave with modified triangle carrier. Urmila and Subbarayudu [4] presents a comparative study of nine level diode clamped inverter for constant

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Switching frequency of sinusoidal Pulse width Modulation and sinusoidal Natural Pulse width Modulation with switching frequency Optimal Modulation. Khoucha et al [5] presents the comparison study for a cascaded H-bridge multilevel direct torque control (DTC) induction motor drive. Earlier studies have pointed out the limitations of conventional inverters, especially in high-voltage and high-power applications. In recent years, multilevel inverters are becoming increasingly popular for high-power applications due to their improved harmonic profile and increased power ratings. Several studies have been reported in the literature on multilevel inverters topologies, control techniques, and applications. However, there are few studies that actually discuss or evaluate the performance of induction motor drives associated with three-phase multilevel inverter. Nami et al [6] proposed a comparative study has been carried out to present high performance of the proposed configuration to approach a very low total harmonic distortion of voltage and current, which leads to the possible elimination of the output filter. A novel H-bridge multilevel pulse width modulation converter topology based on a series connection of a high-voltage diode-clamped inverter and a low-voltage conventional inverter is proposed in this paper. A dc link voltage arrangement for the new hybrid and asymmetric solution is presented to have a maximum number of output voltage levels by preserving the adjacent switching vectors between voltage levels. Hence, a 15-level hybrid converter can be attained with a minimum number of power components. Kangarlu et al [7, 8] proposes a new topology based on the non-insulated dc voltage sources for multilevel inverter with reduced number of switching devices. Multilevel inverters have an important portion in power processing in power systems. Babaei et al [9, 10] developed a new general cascaded multilevel inverter using H-bridges is proposed. The proposed topology requires a lesser number of dc voltage sources and power switches and consists of lower blocking voltage on switches, which results in decreased complexity and total cost of the inverter. These abilities obtained within comparing the proposed topology with the conventional topologies from aforementioned points of view. Moreover, a new algorithm to determine the magnitude of dc voltage sources is proposed.

2. Flying Capacitor Multilevel Inverter

Figure 1 shows the general structure of half bridge five level flying capacitor inverter for R-phase. FCMLI requires 8 semiconductor switches (S1-S4, S1'-S4') 3 flying capacitors (C3', C4', C5') and 2 DC link capacitors (C1', C2'). This FCMLI consists of four switch pairs (S1, S1'), (S2,S2'), (S3,S3') and (S4,S4'). The switches are clamped by DC-link together with flying capacitors. The four switches (S1-S4) must be connected in series between DC input and load and likewise for switches (S4'-S1'). The three flying capacitors C3', C4' and C5' are charged to different voltage levels. By changing the transistor switching states, the capacitors and the DC source are connected in different ways to produce different load voltage levels. A typical switch combination used to synthesize the various load voltages are shown in Table 1.

Table 1 also indicates the state of the flying capacitor corresponding to the switch combination chosen. Charging of a capacitor is indicated by '+', discharging by '-' while NC indicates neither charging nor discharging. By proper selection of capacitor combinations, it is possible to balance the capacitor charge. The capacitor states (+ and -) will reverse for the negative current. The flying capacitor five level inverter is modeled in SIMULINK using power system block set. Switching signals for chosen FCMLI are developed using PWM techniques discussed previously. Simulations are performed with different values of m_a ranging from 0.6 to 1 and resistive load of 100Ω. Simulated output voltages of chosen MLI with various strategies are displayed only for a sample value of m_a=0.8. In this chapter m_f is chosen as 20 as a trade off in view of the following reasons: (i) to reduce switching losses (which may be high at large m_f) (ii) to reduce the size of the filter needed for the closed loop control, the filter size being moderate at moderate frequencies (iii) to effectively utilize the available dSPACE system for hardware implementation. FCMLIs are especially well designed for applications where the number of output voltage levels is high. The applications of FCMLI are fans and pumps, compressors, conveyors, mills, mine winding machines, propulsion drives in marine applications and metal industries. Appropriate PWM strategies may be employed depending on the performance measure required in a particular application.

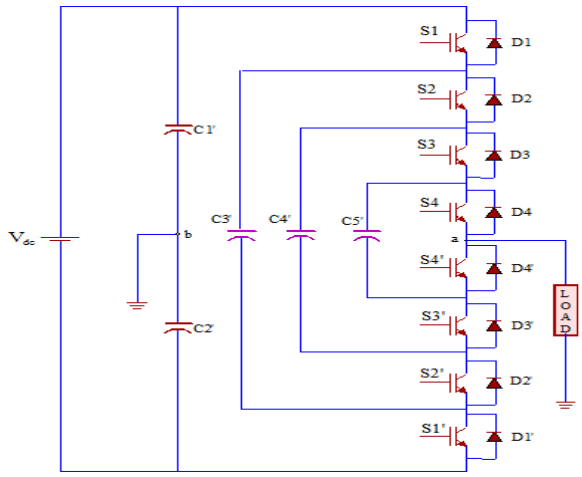

Figure 1. Half bridge five level flying capacitor inverter

Table 1. Switch states and output voltage levels for one phase of flying capacitor inverter

S1	S2	S3	S4	C3'	C4'	C5'	V_{an}
1	1	1	1	NC	NC	NC	$+V_{dc}/2$
1	1	1	0	NC	NC	+	
1	1	0	1	NC	+	-	
1	0	1	1	+	-	NC	$+V_{dc}/4$
0	1	1	1	-	NC	NC	
0	0	1	1	NC	-	NC	
0	1	0	1	-	+	-	
0	1	1	0	-	NC	+	
1	0	0	1	+	NC	-	0
1	0	1	0	+	-	+	
1	1	0	0	NC	+	NC	
1	0	0	0	+	NC	NC	
0	1	0	0	-	+	NC	
0	0	1	0	NC	-	+	$-V_{dc}/4$
0	0	0	1	NC	NC	-	
0	0	0	0	NC	NC	NC	$-V_{dc}/2$

3. Modulation Strategies

Several CFDs exist in multi-carrier PWM strategies for MLIs. These strategies have more than one carrier option that can be triangular, saw tooth, a new function etc. As far as the particular carrier signals are concerned, there are multiple CFDs including function, frequency, amplitude, phase of each carrier and offset between carriers. Although multilevel inverter offers several advantages, the control strategies of MLI are quite challenging due to the complexity to cater the transitions between the voltage levels (or steps). A number of modulation strategies are used in multilevel power conversion applications. In this proposed topology two methods are used.

1. Equal Amplitude Carriers
2. Un Equal Amplitude Carriers (or) Variable Amplitude Carriers (VAC)

3.1. Equal Amplitude Carriers

In this method, all the triangular carriers used will have the same amplitude. The PWM methods used are PDPWM, PODPWM, APODPWM and COPWM with sine, THI, trapezoidal, TAR and stepped wave references. Figure 2 to 4 shows the sample carrier arrangement, output voltage and FFT plot for PDPWM strategy with sine reference (m_a = 0.8 and m_f=20). Where m_a and m_f are the amplitude and frequency modulation index.

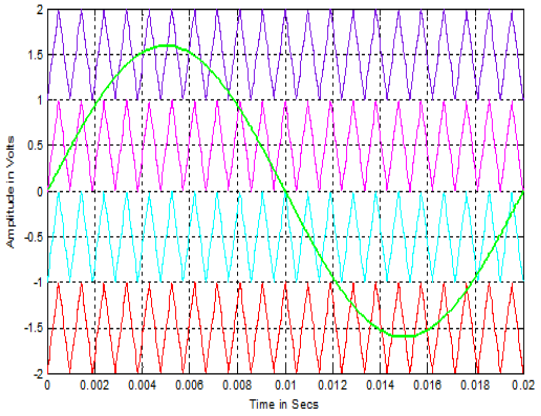

Figure 2. Sample carrier arrangement for equal amplitude carriers with PDPWM strategy (sine reference for m_a = 0.8 and m_f = 20)

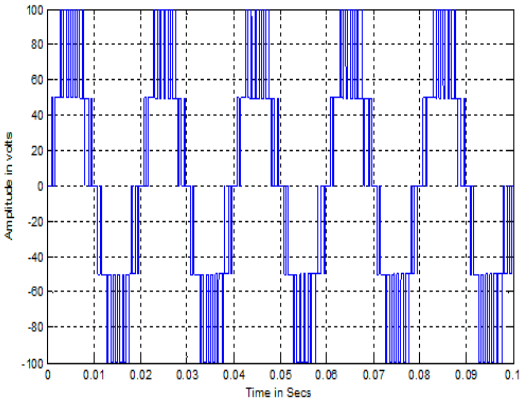

Figure 3. Sample Output voltage of five level inverter based on equal amplitude carriers with PDPWM strategy (sine reference for m_a = 0.8 and m_f =20)

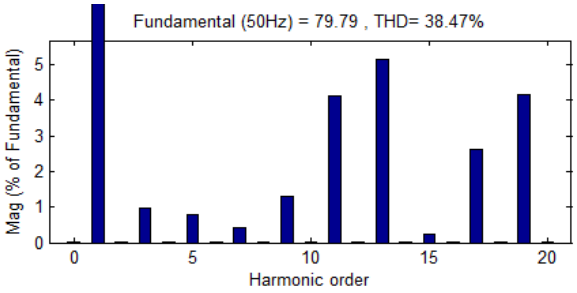

Figure 4. Sample THD plot for five level output voltage based on equal amplitude carriers with PDPWM strategy (sine reference for m_a = 0.8 and m_f =20)

3.2. Un Equal Amplitude Carriers (or) Variable Amplitude Carriers (VAC)

In this method, all the triangular carriers used will not have the same amplitude. The PWM methods used are UEAPD (Un Equal Amplitude Phase Disposition) PWM, UEAPODPWM, UEAAPODPWM and UEACOPWM with sine, THI, trapezoidal and TAR references. Figure 5 to 7 shows the sample carrier arrangement, output voltage and FFT plot for PDPWM strategy with sine reference (m_a = 0.8 and m_f=20). Figure 8 to 10 show the sample reference waveforms. m_a is varied from 1 to 0.6 for equal amplitude carrier methods. In EAC method if m_a is varied from 1 to 0.51 then the inverter will work as a five level inverter and if the m_a is varied from 0.5 to zero then the inverter will work as a three level inverter. But in case of UEAC method if m_a is varied from 1 to 0.26 then the inverter will work as a five level inverter and if the m_a is varied from 0.25 to zero then the inverter will work as a three level inverter.

Where,

$$m_a = \frac{A_m}{A_c} \quad (1)$$

$$m_f = \frac{f_c}{f_m} \quad (2)$$

m_{f1} - Frequency modulation index for upper and lower carriers.
m_{f2} - Frequency modulation index for intermediate carriers.

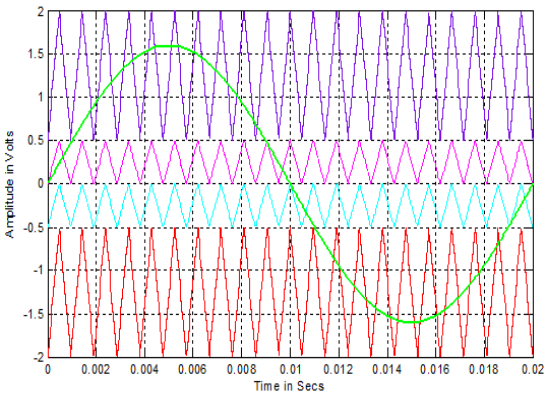

Figure 5. Sample carrier arrangement for unequal amplitude carriers with PDPWM strategy (sine reference for m_a = 0.8 and m_f =20)

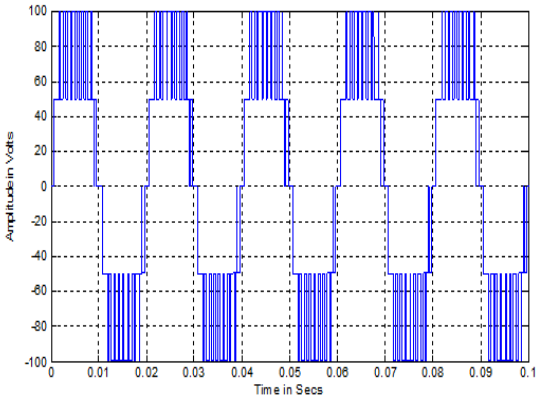

Figure 6. Sample output voltage of five level inverter based on unequal amplitude carriers with PDPWM strategy (sine reference for m_a = 0.8 and m_f =20)

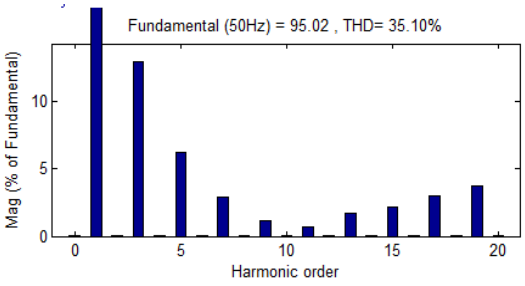

Figure 7. Sample THD plot for five level output voltage based on unequal amplitude carriers with PDPWM strategy (sine reference for m_a = 0.8 and m_f =20)

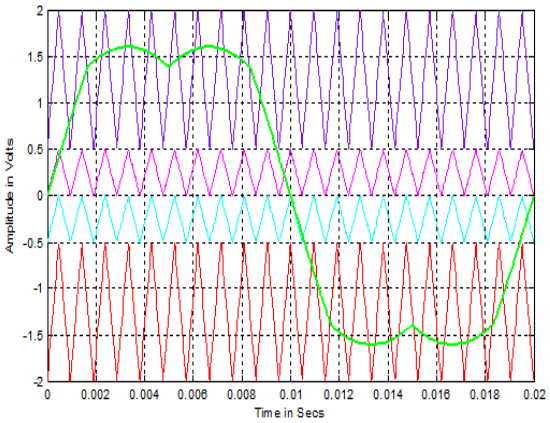

Figure 8. Sample carrier arrangement for unequal amplitude carriers with PDPWM strategy (THI reference for m_a = 0.8 and m_f =20)

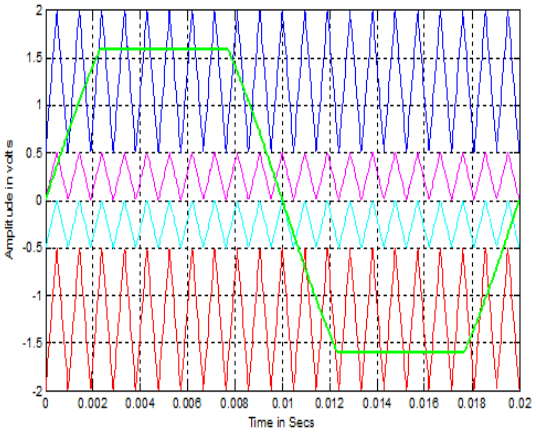

Figure 9. Sample carrier arrangement for unequal amplitude carriers with PDPWM strategy (trapezoidal reference for m_a = 0.8 and m_f =20)

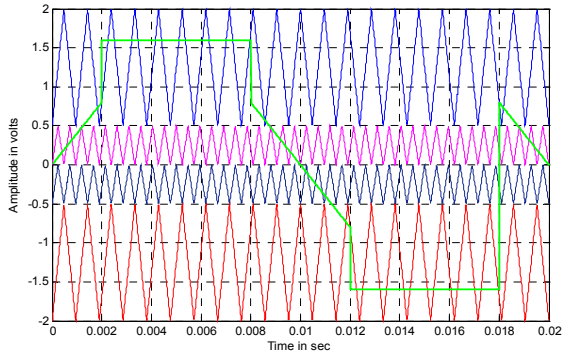

Figure 10. Sample carrier arrangement for unequal amplitude carriers with PDPWM strategy (TAR reference for m_a = 0.8 and m_f =20)

4. Simulation Results

The following parameters are used for the simulation V_{dc} = 200V, R (Resistance) = 100 ohms, C1'=C2'= 4700μF, C3'=1000μF, C4'=1500μF, C5'=3000μF, A_c (Amplitude of the carrier signal) = 0.5, 1 and 1.5, A_m (Amplitude of the modulating signal = 2, f_c (frequency of the carrier signal) = 1000 Hz and 2000Hz and f_m (frequency of the modulating signal) = 50 Hz. Table 1 and 2 shows the THD and V_{RMS} values for the proposed five level inverter. In tables it is represented as 3-level for m_a = 0.5 to 0.3. The equal amplitude carrier methods will give five levels only up to m_a = 0.59 but the UEAC method will give five levels up to m_a = 0.26. The tables compare the total harmonic distortion and voltage in terms of RMS for various references and carriers.

Table 2. %THD for five level output voltage based on equal amplitude and unequal amplitude carriers with various modulation indices

Ref.	m_a	% THD for 5-level inverter							
		PDPWM		PODPWM		APODPWM		COPWM	
		PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	CO	UEACO
Sine reference	1	26.85	27.55	26.57	27.35	26.85	27.21	26.85	30.22
	0.9	33.11	31.52	32.66	31.74	33.11	31.81	33.11	34.43
	0.8	38.47	35.10	37.66	35.38	38.47	35.36	38.47	37.90
	0.7	42.02	38.21	41.85	38.19	42.02	38.25	42.02	40.68
	0.6	44.51	39.61	43.45	39.70	44.51	39.60	44.51	43.58
	0.5		40.62		40.51		40.59		46.2
	0.4	3-level	40.53	3-level	42.70	3-level	40.38	3-level	49.31
	0.3		42.57		43.52		41.5		60.03
THI reference	1	27.58	32.18	28	32.30	28.09	32.49	33.28	33.55
	0.9	35.53	35.72	35.80	35.62	35.8	35.82	37.94	37.64
	0.8	41.34	39.84	41.40	39.99	41.43	39.91	41.52	41.49
	0.7	43.92	43.26	43.77	43.27	43.92	43.18	45.87	44.73
	0.6	43.08	45.41	42.92	45.56	43.05	45.54	52.52	47.46
	0.5		45.54		46.06		45.84		48.80
	0.4	3-level	44.80	3-level	44.87	3-level	44.89	3-level	48.61
	0.3		39.20		39.2		39.27		51.38
Trapezoidal reference	1	22.36	26.48	22.40	26.49	22.45	26.58	29.41	29.25
	0.9	31.50	32.08	31.42	32.25	31.67	32.13	34.33	34.02
	0.8	37.50	36.68	37.62	36.84	37.37	36.80	39.58	38.49
	0.7	41.85	40.22	41.77	40.28	41.96	40.39	44.12	42.04
	0.6	42.18	42.52	42.37	42.68	42.28	42.71	48.75	45.11
	0.5		44.13		44.14		44.24		46.78
	0.4	3-level	43.23	3-level	43.04	3-level	43.10	3-level	48.07
	0.3		39.12		39.22		39.17		48.71
TAR reference	1	34.76	37.50	34.67	37.70	34.67	36.29	42.29	38.98
	0.9	42.96	42.62	42.35	42.78	42.53	39.42	47.09	43.34
	0.8	49.75	47.13	48.26	47.34	49.35	42.49	51.63	48.14
	0.7	53.88	50.27	51.64	50.41	53.84	46.32	55.76	52.36
	0.6	55.06	52.99	52.38	52.59	54.70	49.32	58.90	55.89
	0.5		54.34		54.12		51.99		58.66
	0.4	3-level	54.70	3-level	55.28	3-level	54.5	3-level	60.36
	0.3		50.80		51.86		59.15		61.60

Table 3. V_{RMS} (fundamental) for five level output voltage based on equal amplitude and unequal amplitude carriers with various modulation indices

Ref.	m_a	V_{RMS} (Fundamental) for 5-level inverter							
		PDPWM		PODPWM		APODPWM		COPWM	
		PD	UEAPD	POD	UEAPOD	APOD	UEAAPOD	CO	UEACO
Sine reference	1	70.63	76.7	70.51	76.85	70.32	76.79	70.63	77.5
	0.9	63.52	71.97	63.29	71.96	63.52	71.91	63.52	72.89
	0.8	56.42	67.19	56.52	67.27	56.42	67.13	56.42	68.25
	0.7	49.2	62.04	49.21	62.13	49.2	65.05	49.2	63.63
	0.6	42.17	57.21	42.36	57.24`	42.17	57.2	42.17	58.74
	0.5	3-level	52.07	3-level	52.04	3-level	52.03	3-level	53.7
	0.4		46.45		46.38		46.46		48.01
	0.3		39.83		41.20		41.30		40.04
THI reference	1	81.85	84.53	81.81	84.46	81.73	84.43	84.17	84.73
	0.9	73.66	78.74	73.63	78.83	73.6	78.75	78.75	79.54
	0.8	65.37	73.41	65.44	73.22	65.39	73.39	73.59	74.29
	0.7	57.08	67.78	57.09	67.78	56.98	67.82	67.97	69.17
	0.6	48.78	62.34	48.8	62.2	48.87	62.23	61.31	63.92
	0.5	3-level	56.75	3-level	56.63	3-level	56.79	3-level	58.47
	0.4		50.81		50.78		50.79		53.01
	0.3		44.69		44.79		44.78		46.05
Trapezoidal reference	1	82.84	84.94	82.82	84.92	82.86	84.96	84.63	85.24
	0.9	74.46	79.41	74.56	79.38	74.41	79.36	79.26	79.98
	0.8	66.11	73.77	65.89	73.77	66.12	73.75	73.66	74.72
	0.7	57.75	68.17	57.92	68.19	57.59	68.14	68	69.5
	0.6	49.35	62.63	49.36	62.59	49.4	62.61	61.95	64.02
	0.5	3-level	56.79	3-level	56.71	3-level	56.83	3-level	58.59
	0.4		50.89		51.15		50.87		52.87
	0.3		44.76		44.67		44.62		46.62
TAR reference	1	75.94	77.97	75.86	77.94	75.86	77.39	76.79	78.43
	0.9	68.31	73.02	68.03	72.88	68.84	73.48	71.89	73.72
	0.8	60.74	67.96	60.14	67.68	61.68	69.45	67.02	68.75
	0.7	52.81	62.64	52.34	62.33	53.76	65.46	62.06	63.71
	0.6	45.18	56.93	45.22	56.96	45.93	61.51	56.91	58.33
	0.5	3-level	51.33	3-level	51.48	3-level	57.34	3-level	53.02
	0.4		45.61		45.46		45.68		47.69
	0.3		40.29		40.13		34.2		42.73

4. Conclusion

The proposed work compares the various pulse width modulation techniques for the chosen single phase half bridge DCMLI. For all the PWM strategies and references the UEAC produces less THD and higher fundamental RMS (Root Mean Square) values except for m_a =1. For m_a =1 the EAC provides less THD (Total Harmonic Distortion) and higher fundamental RMS (Root Mean Square) values for all the PWM methods and references. Table 2 and 3 displays the total harmonic distortion and output fundamental voltages for various PWM techniques and references.

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