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Recent advances in phase-locked loop based synchronization methods for inverter-based renewable energy sources

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ABSTRACT

Recently, researchers have shown an increased interest in renewable energy sources (RESs) to improve power quality, reliability and stability of the power system. However, RESs require proper control strategies to ride through grid disturbances and stay connected to the main grid for the stability contribution. Moreover, the control of them relies mainly on the synchronization algorithms to precisely detect the voltage phase angle, magnitude and frequency. Throughout the years, various synchronization schemes have been introduced and developed. In the renewable-based generation sources, the phase-locked loop (PLL) is a well-known technique for operating grid-tied power converters for the estimation of the synchronization information and grid voltage monitoring. This paper aims to provide a comprehensive review of the recently developed PLL algorithms for grid synchronization applications. At first, various estimation techniques are discussed. Then, a comparison between various PLLs and possible future works are recommended.

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1. INTRODUCTION

In recent years, the use of renewable energy sources (RESs) has remarkably increased and they are currently becoming a popular option to replace the dependency on fossil fuels for the effort to achieve the sustainable development [1, 2]. Therefore, it is needed to integrate more RESs in the power system to provide economic and environmental advantages [3]. However, the increasing penetration of RESs is required power electronic-based grid side converters to ease the smooth, reliable and efficient integration with he power system.

Increasing penetration of RESs may deteriorate the reliability, stability and power quality of the power grid. So that, these renewable sources must ride-through all disturbances efficiently and become in synchronism with the power system. The interaction of these RESs over the power converter with the grid or among various converters are followed with the process called synchronization. Moreover, to attain the grid synchronization between the power converters output voltages and the main grid voltages at the point of common coupling (PCC), it is substantial to have precise information regarding the grid voltage fundamental components such as phase angle, magnitude and frequency.

The most well-known synchronization method is based on phase-locked loop (PLL) for advantages such as robustness, simplicity and effectiveness. However, voltage sags, swell, harmonics, voltage unbalance

and DC offset in the voltage have negative impacts and affect the tracking ability of the PLL for accurate fundamental grid voltage phase angle. For this reason, a continuous attempt of improvement and development of the existing PLL schemes is taking place to fulfill reliable operation with better stability and faster synchronization without the large computational overhead. In recent years, many papers have introduced various PLL schemes such as synchronous reference frame PLL (SRF-PLL), dual second-order generalized integrator PLL (DSOGI-PLL), double synchronous reference frame PLL (DSRF-PLL), and enhanced PLL (EPLL) [4, 5]. Table 1 illustrates the comparison of the selected PLL algorithms with their strong and weak sides.

Table 1. Performance comparisons of some PLL synchronization schemes

Synchronization algorithm	Advantage-side	Limitation-side
SRF-PLL	-Simple implementation -Stability -DC offset -Low computational burden -Fast dynamic response -Voltage unbalance -Load rising -Harmonics	-Harmonics -Phase Jump -Voltage unbalances -Load rising -Frequency rising and overshoot
DDSRF-PLL	-DC offset -Stability -Phase jumping -Low computational burden -Voltage unbalance -Frequency rising and variations	-Frequency rising and overshoot -Average implementation simplicity
DSOGI-PLL	-Phase jumping -DC offset -Stability -Fast dynamic response -Harmonics	-Harmonic -Average implementation simplicity -Load rising -High computational burden -Load rising
EPLL	-DC offset -Phase jumping -Stability	-Average implementation simplicity -Frequency rising and variations -Voltage unbalances -Slow dynamic response

This paper introduces a thorough survey on the most relevant and applicable PLL synchronization strategies to facilitate the appropriate selection for most desirable applications and letting know the research community and engineers their advantages and limitations. The rest of the paper is organized as follows. In section 2, grid synchronization methods during faulty conditions are introduced. Section 3 summarizes PLL in detail as well as several PLL algorithms along with their specific block diagrams and equations. Sections 4 concludes the paper with the recommendation for future works.

2. GRID SYNCHRONIZATION METHODS DURING FAULTY CONDITIONS

In recent years, the rapid proliferation of distributed generation (DG) in the power system has given rise to the proposal of various synchronization schemes for grid-connected converter (GCC) applications. They can be classified into two categories, the open-loop and closed-loop approaches as depicted in Figure 1. The zero-crossing detection method [6-8], adaptive notch filtering [9, 10], artificial intelligence [11, 12], nonlinear least square [13], discrete Fourier transform [14], delayed signal cancellation [15, 16], and Kalman filter [17] are the common examples of the open-loop category. On the other hand, the PLL method, SRF-PLL [18, 19], EPLL [20], and SOGI-PLL [21] are the main examples of the closed-loop category. Most of the proposed methods have very good behavior, when the grid voltage is symmetrical; although, find it crucial to accurately estimate the grid voltage angle under distorted voltages or particularly under asymmetrical grid faults. In this paper, despite the importance of the open-loop methods, however, the concentration on phase-locked loop synchronization technology taking into account as PLL techniques are most popular due their accuracy and robustness.

Figure 1. Different grid synchronization methods

3. OVERVIEW OF PHASE-LOCKED LOOP SYNCHRONIZATION TECHNOLOGY

PLL is an old technology since its concept first came into publishing by Bellescise in 1932 [22]. Moreover, it has been applied in an expansive range of applications such as communications, instrumentation, control schemes and many other methods. The basic schematic block diagram of PLL can be described by the three basic elements as shown in Figure 2, where the difference between the phase angle of the input and the output signal is measured by the phase detection (PD) and passed through the loop filter (LF) for phase error elimination. The LF output signal drives the voltage-controlled oscillator (VCO) to generate the output phase, which could follow the input signal. Furthermore, to enhance the PLL performance in different grid conditions, various modifications and improvements have been made such as SRF-PLL, decoupled double synchronous reference frame PLL (DDSRF-PLL), EPLL and SOGI-PLL are among these development schemes. The difference among these strategies usually lies in how the PD block is implemented. In the following subsections, some of them has discussed in detail.

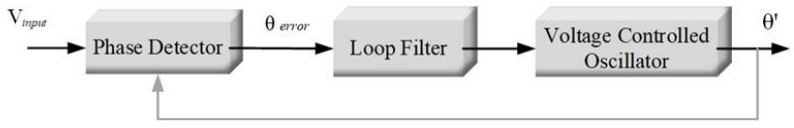

Figure 2. Schematic diagram of a PLL

3.1. SRF-PLL Algorithm

The synchronous reference frame PLL is considered a fundamental PLL, and different advanced PLLs are built upon the Clarke and Park transformations, which converts the natural abc reference frame into the synchronous reference frame. Additionally, the proportional integrator (PI) is then applied to control the *q* variables and the output of the PI controller is the grid frequency. Moreover, the utility phase angle is attained by integrating this grid frequency, which is then fed back into the PD (αβ-dq transformation). Many works have been presented the SRF-PLL algorithm that is used in three-phase grid-connected power converters due to implementation simplicity and fast and accurate estimation of the phase/frequency in typical grid conditions. Figure 3 illustrates the SRF-PLL structure. As mentioned earlier, since the SRF is rotating with the positive angular speed; hence, the conventional SRF-PLL allows fast and accurate estimation of the phase angle and grid-voltage frequency in ideal situations and works properly under balanced grid faults conditions. On the other hand, it fails to track the phase angle, when an unbalanced fault takes place. This is due to the consequence of the presence of twice-grid frequency (2ω) fluctuations which induced by the negative sequence components that disturb the *dq*-components appearing in the mismatch of V_d from the positive sequence magnitude [23]. In addition, the SRF-PLL cannot properly work under harmonically distorted voltages.

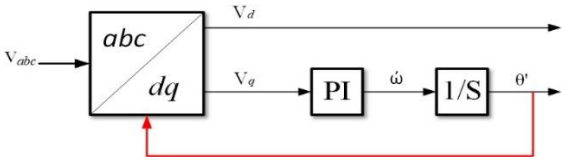

Figure 3. The structure of the synchronous reference frame PLL

3.2. DDSRF-PLL Algorithm

Under unbalanced grid conditions, the performance of SRF-PLL is inaccurate, which leads the loop filter being incapable to abolish harmonic contents occurrence. Using two different reference systems are essential, as the algorithm that expresses grid voltage vector through its direct and inverse sequence components using double synchronous reference frame is called DDSRF-PLL, which the coupling effect between the positive and negative sequences of the voltage is decoupled subsequently [24]. As can be seen in (1) and (2), the transformed voltage vectors consist of DC values and oscillation (2ω) values. The DDSRF-PLL is implemented by converting the grid voltage into positive and negative synchronous reference frames, as shown in Figure 4.

Even though this method can completely remove estimation errors in conventional SRF-PLL, the estimation process is quite complex and sensitive to the phase-angle jump of the grid voltage. The theoretical basis of the DDSRF-PLL with its decoupling network model (Figure 4) is explained below. As a consequence of the decoupling process, the DDSRF-PLL assures a satisfactory operation under unbalanced grid faults.

$$v_{dq}^{-1} = \begin{bmatrix} v_d^{-1} \\ v_q^{-1} \end{bmatrix} = \left[T_{dq}^{-1} \right] \cdot v_{\alpha\beta} = v^{+1} \begin{bmatrix} \cos(2\omega t) \\ \sin(2\omega t) \end{bmatrix} + v^{-1} \begin{bmatrix} 1 \\ 0 \end{bmatrix} \quad (1)$$

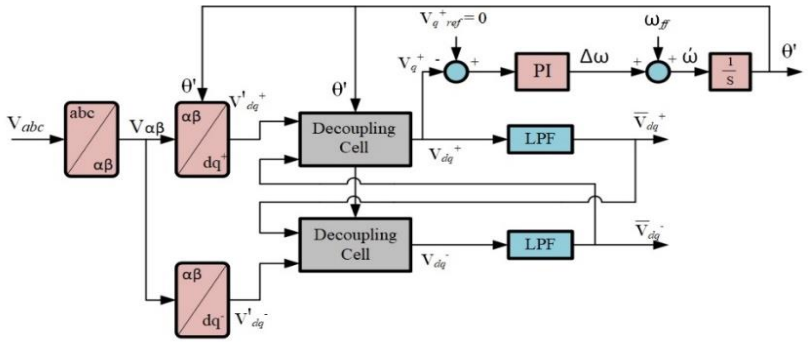

Figure 4. Block diagram of the DDSRF-PLL

$$v_{dq}^{+1} = \begin{bmatrix} v_d^{+1} \\ v_q^{+1} \end{bmatrix} = \left[T_{dq}^{+1}\right] \cdot v_{\alpha\beta} = v^{+1} \begin{bmatrix} 1 \\ 0 \end{bmatrix} + v^{-1} \begin{bmatrix} \cos(-2\omega t) \\ \sin(-2\omega t) \end{bmatrix} \quad (2)$$

where

$$\left[T_{dq}^{+1}\right] = \left[T_{dq}^{-1}\right] = \begin{pmatrix} \cos(\theta') & \sin(\theta') \\ -\sin(\theta') & \cos(\theta') \end{pmatrix} \quad (3)$$

However, for extracting direct sequence grid voltage vector, cross-feedback decoupling network is needed along with the low pass filter (LPF). LPF block is usually selected with first-order transfer function presented in (4):

$$LPF(s) = \frac{\omega_f}{s + \omega_f} \quad (4)$$

where ω_f presents LPF's cut-off frequency. With refer to [23], to secure a stable response of the PLL, the ratio of cut-off frequency and fundamental grid frequency has to be below $(1/\sqrt{2})$. The demonstration of decoupling network for direct sequence is presented in Figure 5.

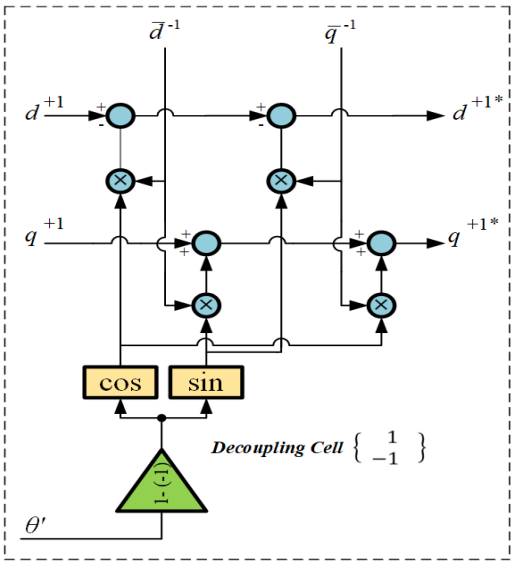

Figure 5. Block diagram of the decoupling cell [23]

3.3. DSOGI-PLL Algorithm

A solution to surpassing issues caused by the voltage unbalances to the phase angle detection can be achieved by proposing a DSOGI-PLL [23]. Basically, DSOGI-PLL has designed in the stationary reference frame basis on instantaneous synchronous technique [25, 26]. In addition, the SOGI converts the input voltages as seen in (5), into an in-phase and a quadrature signal in the αβ reference frame. The strategy uses a LPF together with a bandpass filter (BPF), to take care of the harmonic filtering as well as handle the in-quadrature signals (90° shifted) for $V_{\alpha\beta}$ which computed by two SOGI with a quadrature signal generation (SOGI-QSG) [27]. The block diagram of SOGI, which behaves as an integrator with infinite gain and its transfer functions is described in Figure 6. As seen in (6) and (7), the transfer function of the SOGI's LPF and BPF can be derived from the block diagram as:

$$SOGI(s) = \frac{v'}{k\varepsilon_v}(s) = \frac{s}{s^2 + \omega'^2} \quad (5)$$

$$BPF(s) = \frac{v'}{v}(s) = \frac{ks}{s^2 + ks + \omega'^2} \quad (6)$$

$$LPF(s) = \frac{qv'}{v}(s) = \frac{k\omega'^2}{s^2 + ks + \omega'^2} \quad (7)$$

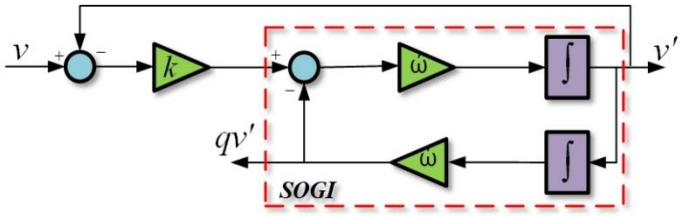

Figure 6. Block diagram of second order generalized integrator (SOGI)

Direct voltage sequence in αβ-frame is extracted by applying two SOGIs based on a quadrature generation (QG), which acts as an adaptive band-pass filter along with Positive-Sequence Calculator (PSC). The Block diagram of complete DSOGI-PLL is shown in Figure 7. When the positive sequence voltage vector is obtained, the *q*-component is forced to zero. Consequently, in order to adapt the center frequency of the DSOGI, the estimated frequency is fed back to the SOGI-QG block. Moreover, the DSOGI-PLL performs an accurate phase angle estimation under unbalanced grid fault conditions, unless it results in large frequency-overshoots and slow dynamics as well.

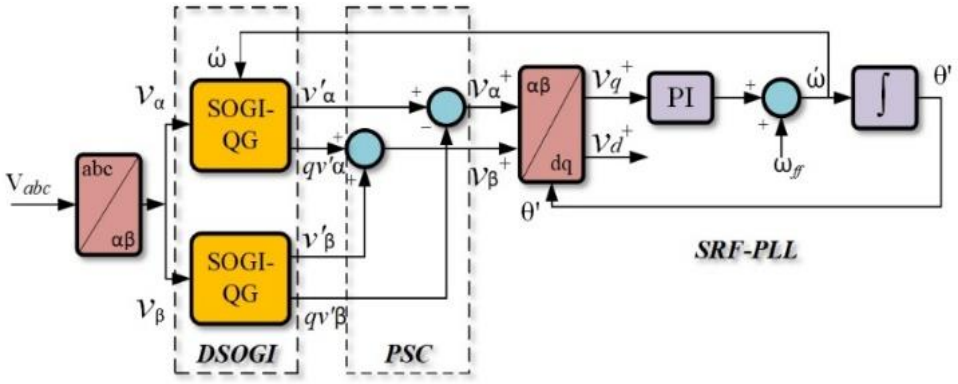

Figure 7. Schematic block diagram of quadrature generation based DSOGI-PLL

3.4. EPLL Algorithm

Fundamentally, the enhanced PLL algorithm is a frequency-adaptive nonlinear synchronization method, its major difference with the existing PLL schemes is to grant more resilience and offer more information to track the frequency, phase angle and magnitude of three-phase input systems [20]. The concept that EPLL basis on the extraction of the positive sequence component of an input signal through a BPF. Furthermore, it is well-known that the impact of the nonideal grid situations, such as noise, unbalance, harmonics, and also the DC offset on the EPLL must be eliminated to assure that it is capable to implement in the utility supply voltage. EPLL is also applied with unified power-quality conditioner (UPQC) to control its voltage source converters (VSCs). When tested in the presence of voltage sags and harmonics on an Electromagnetic Transients DC analysis program, the UPQC was capable to extract the reference signals quickly and directly for the supply voltage and the load current. Introduction of the LPF after the integrator block in the VCO can result in a smoother estimate of phase angle under distorted utility grid conditions [6]. The schematic block diagram of EPLL is depicted in Figure 8. As can be seen that the K parameter is controlling the dynamic response of the phase-locked loop by affecting the speed of convergence of the peak value

estimation loop. Moreover, EPLL can provide the 90° shift of the input signal. Thus, it is an attractive solution in some single-phase system implementations.

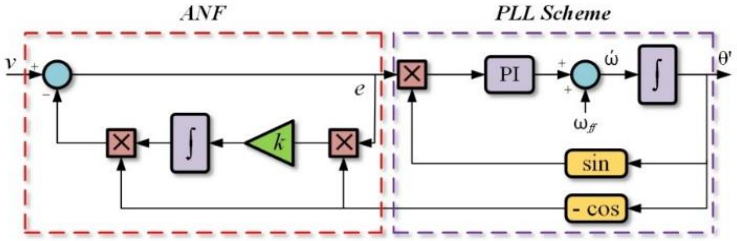

Figure 8. Block diagram of EPLL

4. CONCLUTION AND FUTURE RECOMMENDATIONS

This paper provides a comprehensive review of several state-of-the-art PLL synchronization algorithms than can be applied as a benchmark for the appropriate control of the grid-tied RESs. From the existing literature, it can be clarified that many modifications have been made in the past couple of years for enhancing PLL performance to dismiss any adverse grid conditions. A detailed implementation analysis regarding operating principals, schematic diagram and performance ability has been carried out. Furthermore, as the grid voltage disturbances affecting the capability of synchronization algorithms to accurately estimate the phase angle, hence, this work highlighted the significant characteristics and detailed comparisons of popular PLL synchronization methods performance under different causes of unbalanced conditions. In addition, for the future recommendation, developing effective techniques for frequency deviation and phase angle detection for efficient dynamic performance under severe voltage conditions and harmonics is highly required. Correspondingly, initiating artificial intelligence methods in hybrid with the conventional schemes for grid-tied power converters can be paid more attention in the future researches.

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