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A novel approach of multiplier design based on BCD decoder

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Article Info	ABSTRACT
	A novel approach of multiplier design is presented in this paper. The design idea is implemented based on binary coded decimal (BCD) decoder to seven segment display, by computing all the probability of multiplying 3×3 binary digits bits and grouping in table rows. The obtaining of the combinational logic functions is achieved by simplified the generated columns of [A5: A0], using a Karnaugh map. Then, the 3×3-bits multiplier circuit is used to implement the 6×6- and 12×12-bit multipliers. Comparing with a conventional multiplier, the proposed design outperformed in terms of the time delay by a 32% and 41.8% respectively. It is also reduced the combinational adaptive look-up-tables (ALUTs) by 24.6%, and 46% for both multipliers. Both overmentioned advantages make the proposed multipliers more attractive and suitable for high-speed digital systems.

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1.   INTRODUCTION

The rapid growth of portable computing and wireless communication systems in recent years leads to a need for high-speed arithmetic operation circuits. In addition to that; power consumption and size area dimension are important design factors for any chip designers. Since the multiplier is the key element for most computing processes and other applications such as medical image compression[1], therefore; the improvement of multipliers became a researcher's target.

The concept of array multiplier as early described by [2], is calculating partial products, shifting them to the left and then adding them together. The conventional array multiplier circuit consists of multistages of adders [3, 4] to generate the partial products. A various method and multi techniques have been used to improve the performance of multiplier. Reduction of partial product array is a technique used to improve the booth multiplier [5] and reducing the power [6], [7].

Wallace reduction tree method has been used to provide an area-efficient [8, 9] and improving the multiplication speed. Reducing the power and improving the speed is applied in [10] to optimize the array multiplier. A Vedic algorithm is a useful method for performing the mathematical operations [11,12] with a fast rating.

This paper presents the novel approach of a 3x3 bit multiplier based on BCD decoder to seven segment display. The proposed 3×3 circuit is used to construct a 6×6 multiplier and in the same way, the 6×6 multiplier is used for 12×12 multiplier designing.

2.   DESIGN ARCHITECTURE

The main idea of the suggested circuit design is the following: An 3×3 -bit binary numbers have been used to prepare the results of multiplying each 3-bit of X-group with the others of Y-group. The probability of achieving multiple 3-bit digit numbers is eight (000,001,010,...,111), therefore; each of these

eight multiples 3-bit digit numbers (000 – 111) of X-group multiplying with the listed (000 – 111) Y-group numbers to achieve the correct 6-bit result. Figure 1 shows the multiplication of the X and Y groups in the table.

X Digit Bit	Y Digit Bit	Result	A_5	A_4	A_3	A_2	A_1	A_0
000	000 ⋮ 111	000000 ⋮ 000000	0 ⋮ 0	0 ⋮ 0	0 ⋮ 0	0 ⋮ 0	0 ⋮ 0	0 ⋮ 0
001	000	000000	0	0	0	0	0	0
	001	000001	0	0	0	0	0	1
	010	000010	0	0	0	0	1	0
	011	000011	0	0	0	0	1	1
	100	000100	0	0	0	1	0	0
	101	000101	0	0	0	1	0	1
	110	000110	0	0	0	1	1	0
	111	000111	0	0	0	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
111	000	000000	0	0	0	0	0	0
	001	000111	0	0	0	1	1	1
	010	001110	0	0	1	1	1	0
	011	010101	0	1	0	1	0	1
	100	011100	0	1	1	1	0	0
	101	100011	1	0	0	0	1	1
	110	101010	1	0	1	0	1	0
	111	110001	1	1	0	0	0	1

Figure 1. Multiplication of the X and Y groups

The achieved ($X \times Y$) multiplicand results (shown in Fig. 1) are arranged in $A_5 : A_0$ columns based on the seven segment display concept and the technique used in [13, 14]. Mapping each of these columns in 3×3 in Karnaugh map to minimize the created function. The created functions are given as in follows:

$$A_0 = X_0 Y_0 \tag{1}$$

$$A_1 = X_1 \overline{X_0} Y_0 + X_1 \overline{Y_1} Y_0 + X_0 Y_1 \overline{Y_0} + \overline{X_1} X_0 Y_1 \tag{2}$$

$$A_2 = X_2 X_0 \overline{Y_2} Y_0 + X_2 \overline{X_0} \overline{Y_1} Y_0 + X_2 \overline{X_1} \ \overline{X_0} Y_0 + X_1 \overline{X_0} \overline{Y_1} \overline{Y_0} + X_2 X_1 \overline{X_0} Y_1 + X_1 \overline{Y_2} Y_1 \overline{Y_0} + \overline{X_2} X_0 Y_2 Y_0 + X_0 Y_2 \overline{Y_1} \overline{Y_0} + \overline{X_1} X_0 Y_2 \overline{Y_0} \tag{3}$$

And so on to the rest A_3, A_4 and A_5 equations.

These functions used to design the architecture of the 3×3 -bit multiplier. The achieved functions are coded Verilog hardware description language (HDL) using Quartus II software. The proposed multiplier design codes were synthesized and elaborated in the ALTERA Quartus II software system. The register transfer level (RTL) of the proposed circuit is shown in Figure 2.

The proposed multiplier circuit can be used instead of the conventional 3×3 -bit multiplier circuit (designed by a group of adders in three layers).

2.1. 6×6 -bit Binary multiplier

The proposed 3×3-bit multiplier circuit is used as a key element to contract a 6x6-bit multiplier. Figure 2 explains the design idea. The 6-digit bits of X- and Y-groups are partitioned in two 3-bit blocks namely; first and second blocks. The first block of X-group is multiplied with the first block of Y-group and is also multiplied with the second block of Y-group to create two results of 6-digit bits. The generated 6-bit result of the first and second multiplication results are summed together with a 3-digit bit shifting to the left. Then the generated 9-bit result of the first summation is added to the second summation result with a 3-digit bit shifting to the left also. Figure 3 explains the 12-bit result.
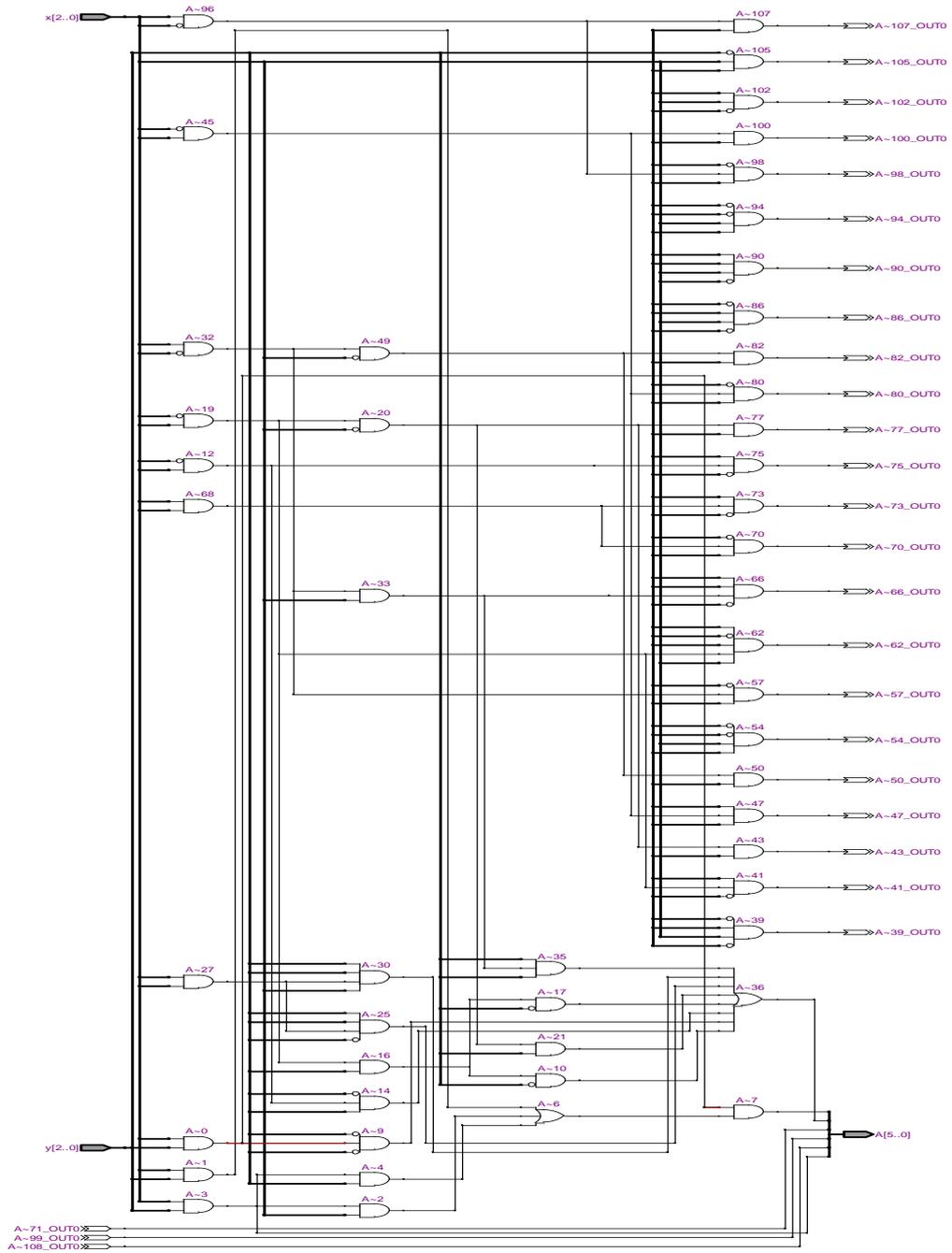
Figure 2. RTL schematic for 3×3 multiplier
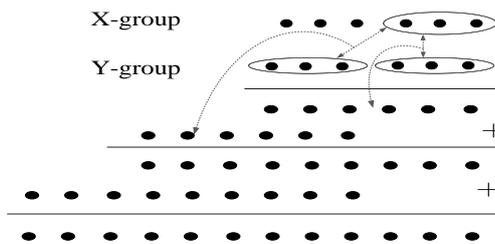
Figure 3. Multiplicand concept of the 6×6 multiplier.

Figure 4 explains the implementation of two pairs of a 3x3-bit multiplier to construct the 6x6 circuit. Arithmetic summation includes a group of half and full adders have been used to achieve the S1 and S2 results and then added together to get the desired 12-bit result. Figure 3 shows the block circuit diagram of the proposed 6x6 multiplier.
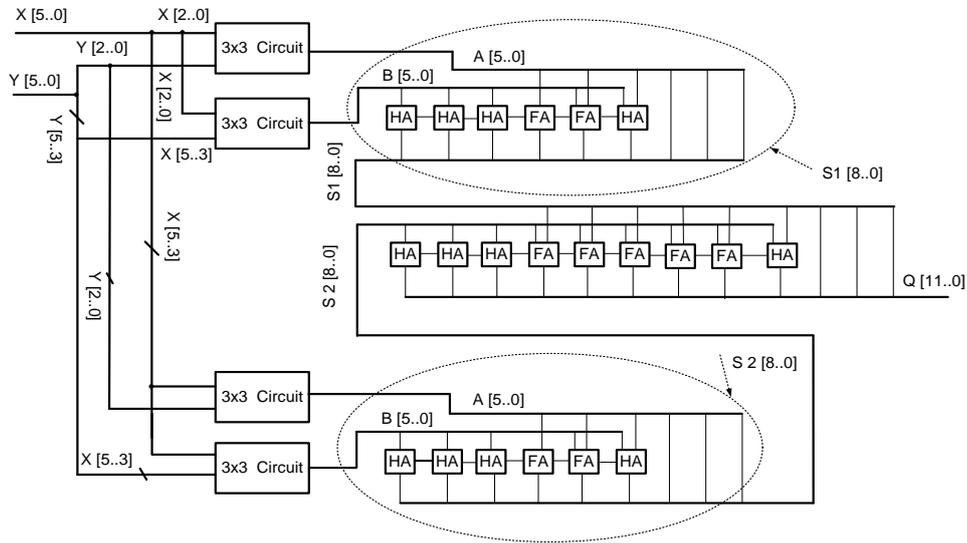
Figure 4. Block circuit diagram of the 6×6 multiplier

2.2. 12 × 12-bit Binary multiplier

The suggested 12×12-bit multiplier is designed based on a 6×6-bit multiplier (as explained in the previous section). The 12-digit bits of X and Y groups is partitioned into two 6-bit block circuits for each of X- and Y-inputs, as shown in Figure 5. Two steps of arithmetic summation have been done including two 18-bit adders for the first step and single 24-bit adder to accomplish the circuit. A 6-bit shifting to left in each of the summation step with multi half and full adders are required to achieve the proposed circuit.
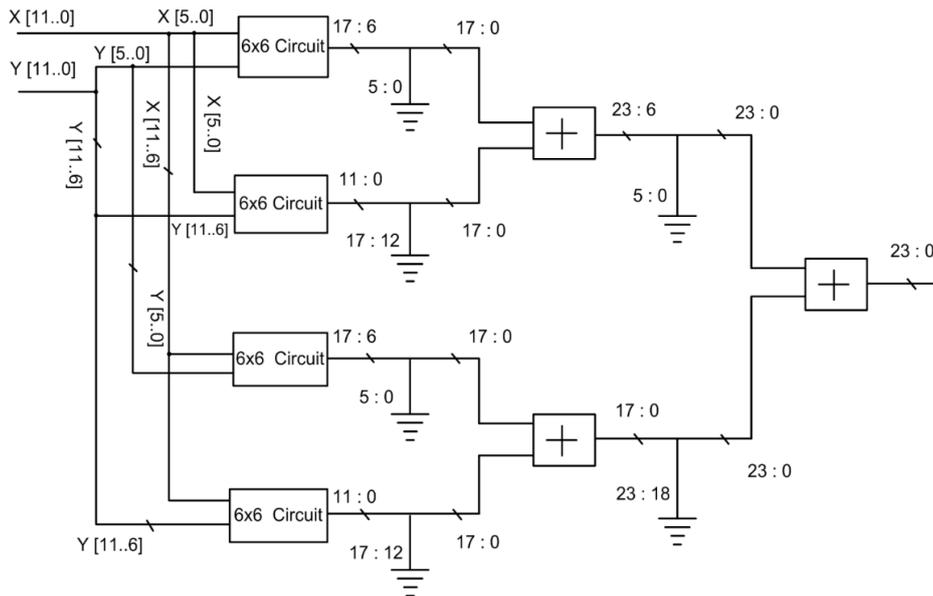
Figure 5. Block circuit diagram of the 12×12-bit multiplier

3.   RESULTS AND ANALYSIS

The proposed multiplier circuit consists of the suggested circuit for 3×3-bit multiplier with half and full-adders that needs to architect the other 6×6- and 12×12-bit study case design circuits. Since all these circuits digitally operate the system, therefore; these design circuits have been coded in Verilog HDL code using Quartus II software. The proposed multiplier design codes were synthesized, elaborated and compiled in the ALTERA Quartus II software system with Stratix III FPGA kit board, to functionally verify the system design. ModelSim 6.5 software is used to simulate the proposed design. First of all, the 3×3-bit multiplier code is need to be simulated, because it uses a key element for the next two designed projects. Since the simulated result was proved, then the 3×3 multiplier circuit was employed in 6×6-, and 12×12-bit circuits.

The compilation report of Quartus II software shows that the design circuits constructs with 4, 43 and 219 adaptive look-up-tables (ALUTs) for 3×3-,6×6-, and 12×12-bit multipliers respectively. The simulation result of the 3×3-bit multiplier is shown in Figure 5-a. As shown in Figure 6-a, the proposed 3×3-bit multiplier introduced a valid correct multiplier output, thus the 3×3-bit multiplier circuit was employed in 6×6- and 12×12-bit circuits. The simulation result of 6×6- and 12×12-bit multipliers are shown in Figure 6-(b and c). The achieved output results of 3-, 6-, and 12-bit multipliers regarding their given input numbers show that they are exactly matched with mathematically multiplication results.
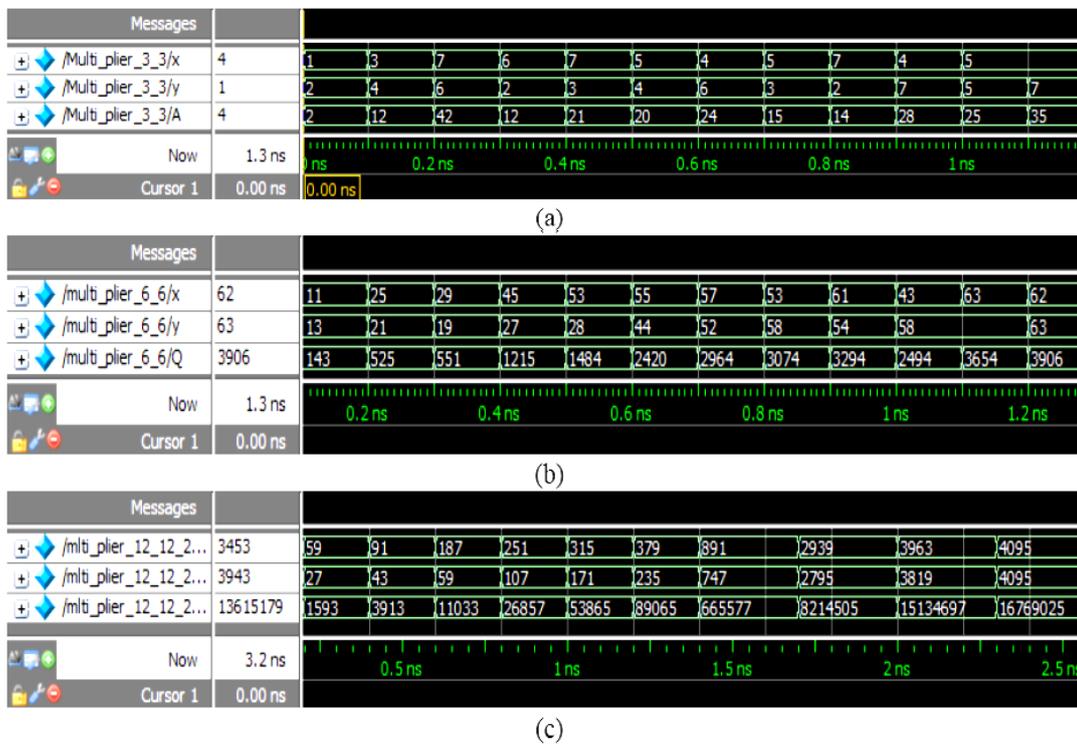
Figure 6. Simulation result of: (a) 3×3-bit, (b) 6x6-bit, and (c) 12x12-bit multipliers

The coded design circuits were elaborated, synthesized and compiled using Quartus II software system and Stratix III field programmable gate array (FPGA) kit board. The proposed multiplier circuits have the delay of 1.714 and 5.268 ηSec for 6-, and 12-bit multipliers respectively.

To compare the proposed design multipliers with the conventional circuits, Verilog HDL has been used to construct the conventional multipliers using Quartus II software. The conventional multiplier of 3-, 6-, and 12-bit design codes were synthesized, elaborated and compiled in the Quartus II software system with Stratix III FPGA kit board. A comparison in maximum operating frequencies and combinational adaptive look-up-tables (ALUTs) cells between the conventional and the proposed design has been done in Table 1.

Table 1. Comparison between the Conventional and The Proposed Design Multipliers

Conventional	6×6		12×12	
	Conventional	Proposed	Conventional	Proposed
Delay (ηSec)	2.524	1.714	9.05	5.268
Combinational ALUTs cells	43	23	290	219

Table 1 shows that the proposed design outperforms other conventional multipliers in terms of delay time and lower combinational (ALUTs) cells. The Table 1 appears that the delay time of the proposed design multiplier is relatively increased and the combinational (ALUTs) relatively reduced proportionally with increasing the bit multiplier bit circuits (3-, 6-, and 12-bit multipliers).

4.   CONCLUSION

A novel approach of multiplier design based on BCD decoder to seven segment display is presented in this paper. Three multiplier circuits designs are introduced. A 3×3-bit multiplication operation is achieved by multiplying each the 3-bit X-group with the others from 3-bit Y-group and grouped the results in A5: A0 columns based on the seven-segment display concept.

Mapping the columns in 3x3 Karnough maps to create the desired functions for the 3×3 multiplier. The designed circuit of the 3×3-bit multiplier is used to architect the proposed 6x6-bit multiplier, and the same way is used to design the 12×12 multiplier. The proposed circuits are simulated using Verilog HDL, Modelsim, and Quartus II software.

The proposed multiplier outperforms the conventional multipliers in the delay time and ALUTs cells by a 32% and 41.8% time improvement are achieved for both 6×6- and 12×12-bits multipliers. Also, both multipliers achieved 24.6% and 46% reduction in comparison with other multipliers.

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