Indonesian Journal of Electrical Engineering and Computer Science
Vol. 12, No. 3, December 2018, pp. 1358~1365
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v12.i3.pp1358-1365

30nm DG-FinFET 3D Construction Impact Towards Short Channel Effects

Ameer F. Roslan, F. Salehuddin, A.S.M. Zain, K.E. Kaharudin, H. Hazura, A.R. Hanim, S.K. Idris, B.Z. Zarina, Afifah Maheran A.H
MiNE, CeTRI, Fakulti Kejuruteraan Elektronik dan Kejuruteraan Komputer, Universiti Teknikal Malaysia Melaka, Jalan Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia

Article Info

Article history:

Received Aug 28, 2018
Revised Oct 15, 2018
Accepted Oct 29, 2018

Keywords:

Double-gate finfet
Mosfet
Multi gate
Short channel effects

ABSTRACT

This paper presents an investigation on properties of Double Gate FinFET (DG-FinFET) and impact of physical properties of FinFET towards short channel effects (SCEs) for 30 nm device, for which the depletion-layer widths of the source-drain relates to the channel length aside from constant fin height (H_{FIN}) and the fin thickness (T_{FIN}). Virtual fabrication process of 3-dimensional (3D) design is applied throughout the analysis. Further to that, its electrical characterization is employed and the ratio of drive current against the leakage current (I_{ON}/I_{OFF} ratio) of the FinFET design on the other hand has showcased substantial difference at 563138.35 compared to the prediction made by the International Technology Roadmap Semiconductor (ITRS) 2013. Conclusively, the incremental in ratio has fulfilled the anticipated increment on the drive current (I_{ON}) as well as reductions of the leakage current (I_{OFF}). Threshold voltage (V_{TH}) meanwhile has also achieved the nominal prediction that is obliged by the International Technology Roadmap Semiconductor (ITRS) 2013 for which is at 0.676±12.7% V. The I_{ON}, I_{OFF} and V_{TH} obtained from the device has evidently met the minimum condition by ITRS 2013 for low power Multi-Gate technology.

Corresponding Author:

Ameer F. Roslan,
MiNE, CeTRI, Fakulti Kejuruteraan Elektronik dan Kejuruteraan Komputer,
Universiti Teknikal Malaysia Melaka,
Jalan Hang Tuah Jaya, 76100 Durian Tunggal, Melaka, Malaysia.
Email: m021710023@student.utem.edu.my

1. INTRODUCTION

Moore's law has served as guideline for MOSFET miniaturization for over a decade. Yet, the circumstances in the rescaling of the MOSFET is due to the gate controllability decreased over the channel caused by high electric field [1, 2]. Besides, shrinking the conventional MOSFET needs improvements to bypass the barriers that are due to the fundamental physics [3]. Continuous scaling of bulk-Si MOSFET technology have also been massively challenged by the increment in leakage current and also the performance variability of transistor [4, 5]. This indicates that the short channel effects (SCEs) have continually been the key issues when the rescaling is implemented. That being said, an alternative way to analyse and process multi-gate transistor like double-gate FinFET (DG-FinFET) have been done in order to achieve the perfect switch for transistor, along with to minimize the SCEs. SCEs occurred due to the charge sharing effect in the shorten devices channel, aside from the reason that the channel depletion region and inversion layer channel charge control has been contested by both gate and source/drain regions. In addition to that, the extreme increment in the subthreshold leakage current has become concerning once it approaches the nanometer regime [6].

The electrostatics of the channel has been effectively impacted by the drain potential and, consequently, channel has been unable to be controlled by the gate as these are mainly due to the channel lengths that are thinned in deeply scaled MOSFET. Consequently, the gate is incapable to fully close the

channel in the off-mode operation, which directs to the rise of I_{OFF} between the drain and the source. Meanwhile, the alternative to the existing planar MOSFET, that is the multiple-gate field-effect transistors (MGFETs), has showcased a better screening of the drain potential from the channel and this is due to the proximity of the supplementary gate(s) to the channel (i.e., higher gate-channel capacitance) [7, 8]. This makes the short channel performance metrics, such as subthreshold slope (*SS*), drain-induced barrier lowering (DIBL), and threshold voltage (V_{TH}) roll-off better in MGFETs compared to the orthodox planar MOSFET. These metrices improvements would means reduced in degradation in the transistor's V_{TH} with continuous scaling and thus bringing less degradation as well to the leakage current (I_{OFF}) [9]. DIBL effect is evident as the shrinkage of the device occurred due to substantial field penetration from drain to source for which the aforementioned source and drain depletion regions can infringe the channel without bias due to smaller gaps between these junctions in short channel device. The V_{TH} roll off in the meantime is caused by reduction in V_{TH} due to decrement in gate length as the channel length is unacceptable when the off-state I_{OFF} has become too great [10]. Several experiments of designing a 3D FinFET Double-Gate device is done after the initial fabrication simulation by revising several physical parameters. DG-FinFET has been contemplated in the present work because of its better gate control over the channel which allows an enhanced device performance [11]. Figure 1 shows the superior short-channel performance of DG-FinFETs over planar MOSFETs with the same channel length [12].

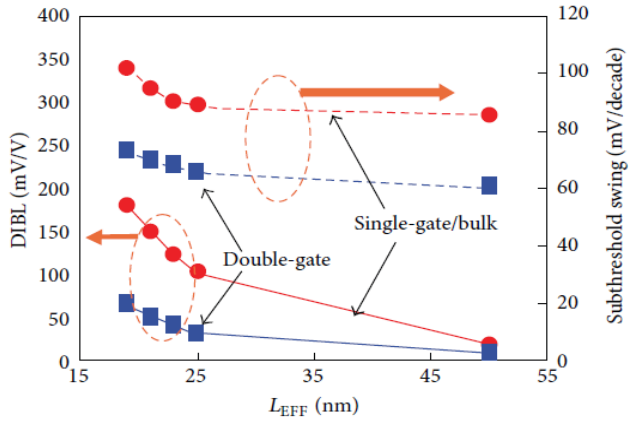

Figure 1. DIBL and subthreshold swing (*SS*) versus effective channel length for double-gate (DG) and bulk-silicon nFETs

DG-FinFETs emerge superior to planar MOSFETs by overcoming a major source of process variation [3]. The FinFET structure also utilizes a fin-shaped body that is perpendicular to the wafer surface to carry the current for which it is encased by two of the front and back gates that are developed thinly in order to reduce the SCEs. DG-FinFETs do suffer from other process variations. Due to their small dimensions and lithographic limitations, DG-FinFETs are subjected to several important physical fluctuations, such as variations in gate length, fin-thickness, gate-oxide thickness, and gate underlap [13].

Generally, a major amount of work on the projection of leakage current and leakage power prediction has been issued by various researchers [11], [14–23]. Bhattacharya and Jha reported that the three-dimensional (3D) process simulations and device simulations were carried out so that the fabrication processed and the device characteristics of 22nm DG-FinFETs is optimized [3]. Parameters studied has massively enhanced the respective V_{TH}, I_{ON}, I_{OFF} values for which is centred on the minimum requirement standardized by International Technology Roadmap Semiconductor (ITRS) 2013 prediction for low power (LP) multi-gate technology for the year 2020.

2. METHODS AND MATERIALS

2.1. Virtual Fabrication Process

In this study, the DG-FinFET fabrication procedure is done through DEVEDIT and ATLAS modules from Silvaco International. Both ATLAS and DEVEDIT contrasts in its functionality whereby the ATLAS as well as DEVEDIT provides device simulations MOSFET device. The general process flow of a DG-FinFET especially in obtaining its electrical properties is contained in the ATLAS module in Silvaco TCAD tool and the process simulation methods is summarized as in Figure 2.

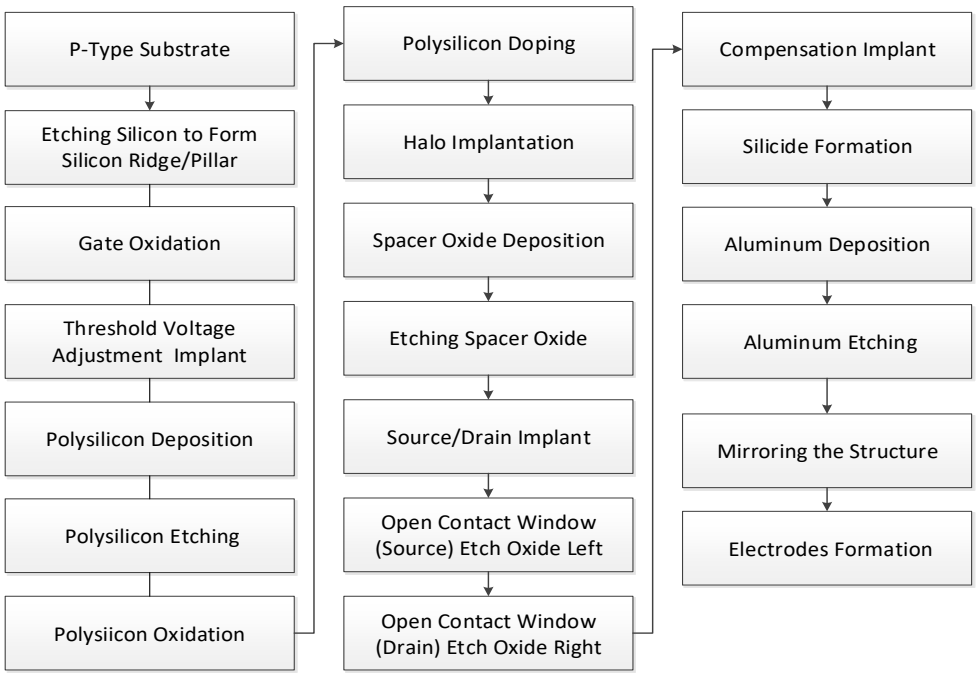

Figure 2. Basic DG-FinFETs Process Simulation

Since FinFET have a sizeable outcome towards the device's I_{OFF}, V_{TH} and I_{ON}, the dimensions of the fin has been defined beforehand in order to establish desired effective channel length and also gate width of the device [24]. The incremental towards the speed of the transistor switching can be done, should it have a high I_{ON} and a low V_{TH}. Based on the constant fin height (H_{FIN}) and the fin thickness (T_{FIN}), constrain of the width can be obtained as:

$$W = 2H_{FIN} + T_{FIN} \quad (1)$$

Leakage performance can also be influenced by the fin shape and its dimension whereby narrower fin encourages lower leakage current to be obtain. The values of geometrical parameters are identified as shown in Table 1.

Table 1. Value of the geometrical parameters set for Y-Z plane, X-Y plane and X-Z plane

Y-Z Plane		X-Y Plane		X-Z Plane	
Parameters	Value (nm)	Parameters	Value (nm)	Parameters	Value (nm)
Gate Length, L_G	30.00	SiO_2 Width, $W_{OX\ X-Y}$	30.0	SiO_2 Length, $L_{OX\ X-Z}$	100.0
SiO_2 Length, L_{OX}	100.0	SiO_2 Thickness, $T_{OX\ X-Y}$	30.0	SiO_2 Width, $W_{OX\ X-Z}$	30.0
SiO_2 Thickness, T_{OX}	30.00	Metal Gate SiO_2 Width, $W_{OX\ X-Y}$	16.0	Metal Gate SiO_2 Length, $L_{OX\ X-Z}$	80.0
Metal Gate SiO_2 Length, L_{OX}	80.00	Metal Gate SiO_2 Thickness, $T_{OX\ X-Y}$	18.1	Metal Gate SiO_2 Width, $W_{OX\ X-Z}$	2.98
Metal Gate SiO_2 Thickness, T_{OX}	2.98	Aluminium Width, $W_{AL\ X-Y}$	10.0	Aluminium Length, $W_{AL\ X-Z}$	10.0
Aluminium Length, L_{AL}	10.00	Aluminium Thickness, $T_{AL\ X-Y}$	15.0	Aluminium Width, $W_{AL\ X-Z}$	10.0
Aluminium Thickness, T_{AL}	15.00	Polysilicon Thickness, $T_{DM\ X-Y}$	25.0	Polysilicon Length, $L_{DM\ X-Z}$	30.0
Polysilicon Thickness, T_{DM}	7.10	Polysilicon Width, $W_{DM\ X-Y}$	30.0	Polysilicon Width, $W_{DM\ X-Z}$	7.0
Silicon Thickness, T_S	15.00	Silicon Thickness, $T_{S\ X-Y}$	15.0	Silicon Length, $L_{S\ X-Z}$	80.0
		Silicon Width, $W_{S\ X-Y}$	15.0	Silicon Width, $W_{S\ X-Z}$	10.0

Six constrained mesh regions were set comprises of silicon as the main substrate, two regions of silicon oxide (SiO_2), polysilicon, and two regions of Aluminium based bulk bottom electrodes. Meshing parameters were then set with its height and width set at 10 nm and 5 nm respectively whereby the maximum angle allowed within its triangle is controlled. The maximum slope is bounded at 28º with maximum ratio of 300. Impurities minimum spacing was applied at 20 nm when X-direction is equivalent to 0. The fabrication simulated using geometrical parameters that follows Table 1 is obtained and analysed from Y-Z plane as in Figure 3(A). Therefore, the calibration process was used with standard fluid (Glycerin) which was already brought with devices. To validate the data error of the reading from the measurement must less than 0.01. Meanwhile, the cross section of DG-FinFET from X-Y plane at elevation = -1 slices the device that showcases the Aluminium region and SiO_2 for which obeys the geometrical parameters in Table 1 as shown in Figure 3(B).

The structure at X-Y plane at elevation = 0 meanwhile exhibits two SiO_2 regions, Silicon and Polysilicon for which follows the parameters set as in Table 1 as shown in Figure 3(C). In the meantime, two cross sections of X-Z planed DG-FinFET simulated is presented ensuring all regions are viewed in each plane. Through geometrical parameters established in Table 1, the structure from elevation = 0.5 in Figure 3(D) shows the SiO_2 region that overlooks Silicon, metal gate SiO_2, and Aluminium-based electrode regions contrary to the cross section in for when the plane elevation = 0, for which veiled the SiO_2 region.

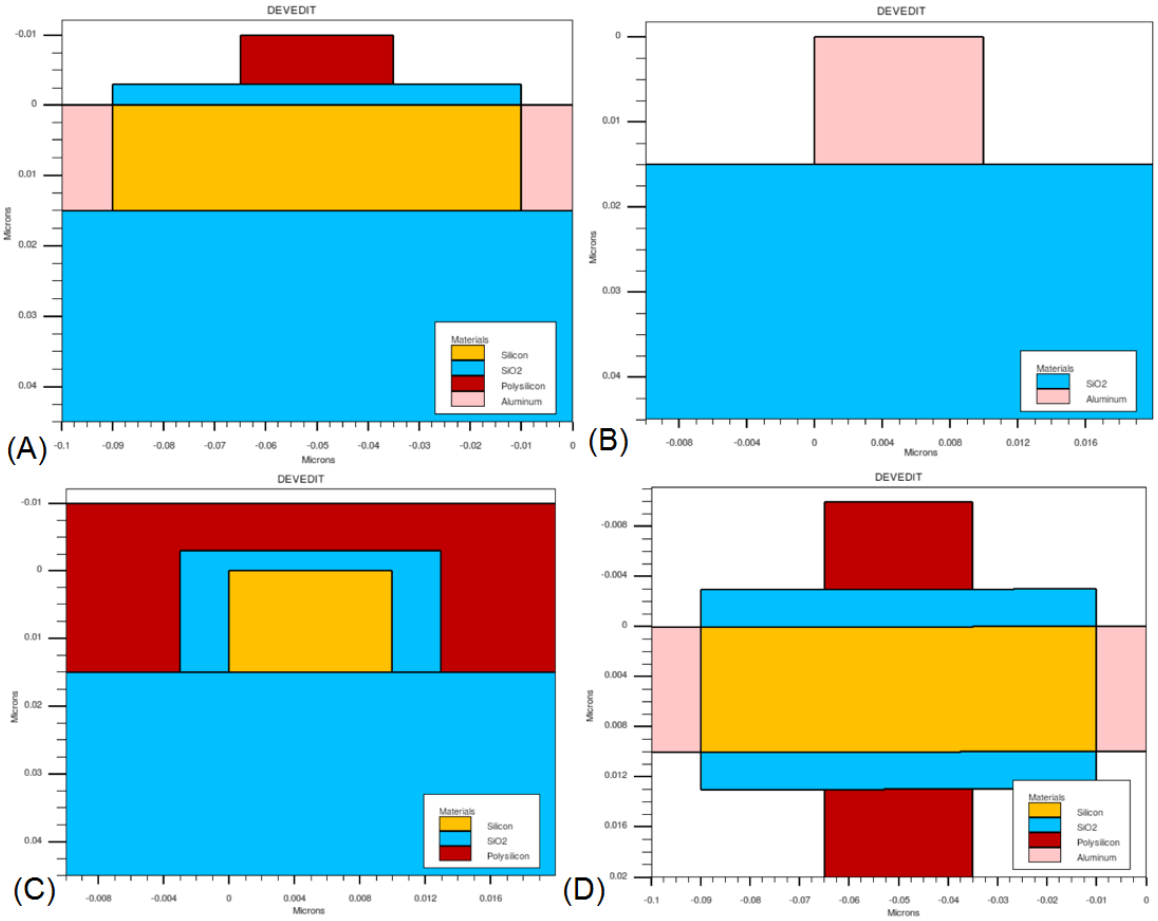

Figure 3. (A) Cross section of DG-FinFET on Y-Z Plane, (B) Cross section of DG-FinFET on X-Y Plane at elevation = -1, (C) Cross section of DG-FinFET on X-Y Plane at elevation = 0, and (D) Cross section of DG-FinFET on X-Z Plane at Elevation = 0.5

2.2. Process Design Fabrication

For the intent of I-V curves simulation of the devices, the Silvaco TCAD has employed the ensuing set of physical models: 1) drift diffusion (DD) model with simplified Boltzmann carrier statistics; 2) Fermi-Dirac model as a statistical approach implemented in order to reduce the concentrations of a heavily doped

carrier regions. Critical electrical characteristics like threshold voltage, ON-state current, OFF-state current and subthreshold swing could be extracted from the I_D vs. V_G characteristic.

The coefficient of V_{DS}, ALPHA is set at 1.4 1/V alongside the static feedback parameter, GAMMA at 0.3 through the application of the ATLAS tool with work function of 4.85 eV. The concentration of p-type silicon as the aforementioned main substrate is set at $1x10^{18}$ atom/cm^3 whilst is $1x10^{21}$ atom/cm^3 used for the n-type substrate for when Y_{MIN}=0, Y_{MAX}=0.015, and the characteristic length of laterial in Z-direction is set at 0.004 at Z_{MIN}=0.01, Z_{MAX}=0.0233 and Z_{MIN}=0.0767 and Z_{MAX}=0.091. Alternatively, the parameters for the band-edge alignment is definable as either electron affinity or edge alignment whereby in this design the electron affinity is involved. The silicon energy gap at 300K is set at 1.1245 eV followed with 4.05 eV for the material affinity at permittivity, ε=11.9. The temperature of the bandgap energy equation as well as default values applied for each energy bandgap parameters is as following in Table 2 [25]:

$$E_g(T_L) = E_g(0) - \frac{\mathbf{EGALPHA}(T_L^2)}{T_L + \mathbf{EGBETA}} = \mathbf{EG300} + \mathbf{EGALPHA}\left[\frac{300^2}{300 + \mathbf{EGBETA}} - \frac{T_L^2}{T_L + \mathbf{EGBETA}}\right] \quad (2)$$

Table 2. Default parameters for energy bandgap [26]

Parameters	Value
Energy gap at 300K, EG300	1.08 eV
Alpha Coefficient, EG_{ALPHA}	$4.73x10^{-4}$ eV/K
Beta Coefficient, EG_{BETA}	636 K
Conduction band density, NC300	$2.8x10^{19}$ cm^{-3}
Valence band density, NV300	$2.8x10^{19}$ cm^{-3}

Meanwhile, number of times the trap procedure is set to six so that it could be repeated in case of discrepancy with the number of initial block iteration set at 45. The block iteration would serve as an iteration method alongside Newton when convergence is unattainable through Gummel scheme as the Gummel iteration is capable to refine initial convergence guess from Newton method. The Fermi-Dirac model is then implemented that adheres the electrons with a semiconductor lattices in such thermal equilibrium at temperature T_L. The availability electron state is electron-occupied energy ε can be obtain through [26]:

$$f(\varepsilon) = \frac{1}{1 + \exp\left(\frac{\varepsilon - E_F}{kT_L}\right)} \quad (3)$$

The Fermi level energy in Equation (3) is represented by E_F followed with k which denotes the Boltzmann constant. Therefore, 8.05 eV is used for when the oxide energy gap is at 300K, with $2.8x10^{19}$ cm^{-3} of conduction band density implemented while the material affinity and its permittivity, ε is set at 1 eV and 3.9 respectively. The polysilicon at permittivity of 11.9 meanwhile requires 1.1245 eV of energy gap at 300K, 4.05 eV of affinity, and $2.8x10^{19}$ cm^{-3} of conduction band density, in addition to the valence band density of $1.04x10^{19}$ cm^{-3}. Since non-local effects is abandoned in conventional drift-diffusion model of the charge transport, the energy balance model is enabled in this model by considering the electron temperatures in the Fermi-Dirac statistical method. The parallel electric field dependence model for this design is used as it calls on the field-dependent mobility. The maximum magnitude of possible correction is set to 1.0 to damp the Gummel iterations.

In the meantime, the extraction of the drain current against gate voltage (I_D-V_G) and V_{TH} properties is acquired by applying Newton method when divergence occurred in a solution process whereby decremental of multiplication factor is carried out from the initial approximation of the electrode bias step. In this regard, drift-diffusion calculations are managed in the. ATLAS using the Newton iteration.

3. RESULTS AND DISCUSSION

Based on the 2D structure of the DG-FinFET produced which is the cross sections of the device, the 3D structure is also obtained as shown in Figure 4. Compared to the 2D cross sections obtained, it is observed that the 3D structure produced comprises the aforementioned X-Y plane, X-Z plane, and Y-Z plane. The silicon region is observed to be concealed away as in Figure 4 due to the fact that it is wrapped and surrounded by the

metal gate SiO2 and polysilicon as presented in Figure 3(C) in forming a notional DG-FinFET structure as this has ensured the fin shape minimizes the I_{OFF}, subsequently restricting SCEs from taking its place on the structure performance. The variation on gate length, channel doping and S/D doping concentration has been implemented to analyze the device performances of V_{TH}, I_{OFF}, I_{ON} and SS and ratio of I_{ON}/I_{OFF} for which a curve of Drain Current (A), I_D against Gate Voltage (V), V_{GS} is generated by ATLAS module as in Figure 5. Through comparisons made between read value obtained through simulations, against predicted value from ITRS 2013, V_{TH} obtained is slightly higher than predicted value made by the ITRS 2013 which is 0.699 V compared to 0.676±12.7% V albeit minimal in differences.

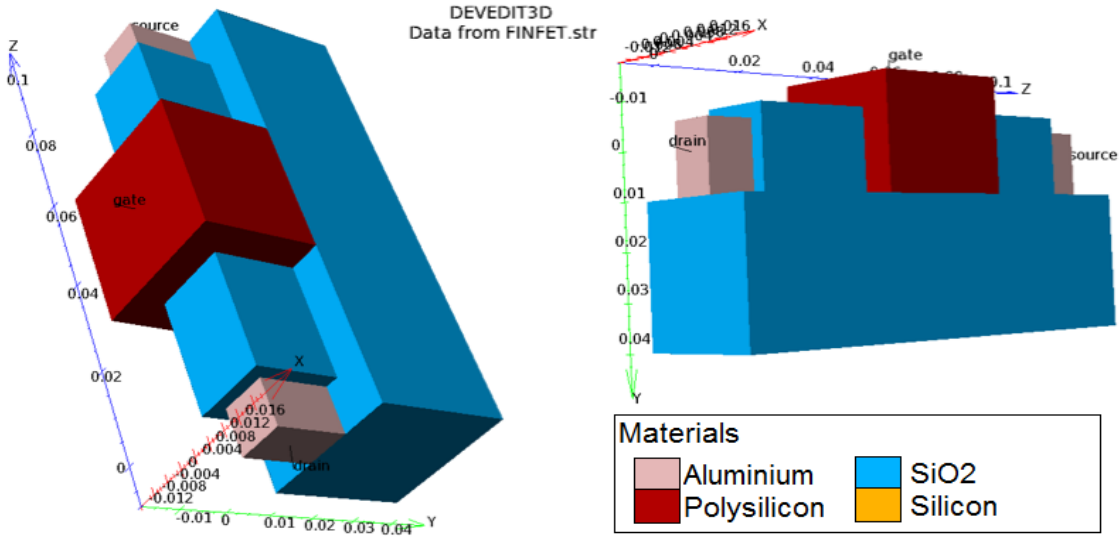

Figure 4. 3D structure of DG-FinFET

Nevertheless, the I_{ON} and I_{OFF} both have achieved desired values when assessed with the predicted ones whereby the I_{ON} obtained higher than 485 µA/µm at 1243.86 µA/µm as the I_{OFF} attained substantial difference in 0.0022 pA/µm as compared to 20 pA/µm predicted, bringing the I_{ON}/I_{OFF} ratio to be significantly higher. Preferably, the device with a greater I_{ON}/I_{OFF} ratio means that the device has met an exceptional value due to incremental of I_{ON} versus the decreasing I_{OFF}, that is consistent to the expectation made by the ITRS 2013 and hence, through Table 3 it is evaluated that the FinFET structure has bring the ratio much superior in contrast to the ideal ratio of 24.5 aimed.

Table 3. Comparisons in value of electrical characteristics based on read value and ITRS 2013 value

Parameters	ITRS Value	Read Value
V_{TH} (V)	0.676±12.7%	0.699
I_{ON} (µA/µm)	> 485	1243.86
I_{OFF} (pA/µm)	< 20	0.0022
I_{ON}/I_{OFF} Ratio	24.5	563138.35
SS (mV/ dec)	70 ~ 90	71.40
GIDL	-	0

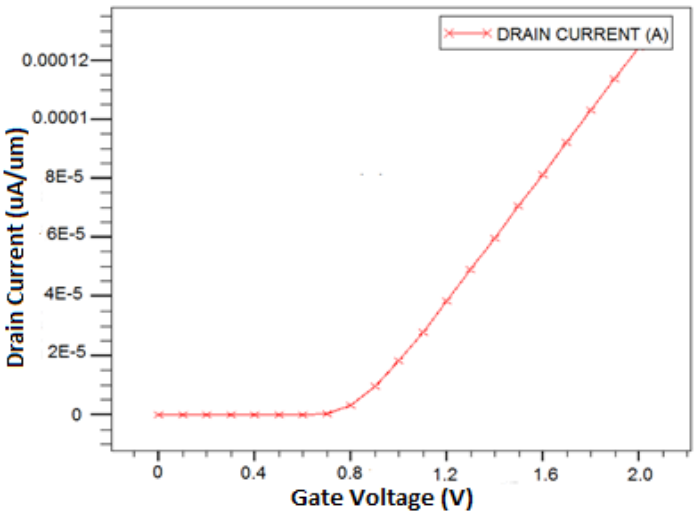

Figure 5. Drain Current (A), I_D against Gate Voltage (V), V_{GS} curve of DG-FinFET from ATLAS module

4. CONCLUSION

In this study, a 3D double gate FinFET is designed with focus of minimizing the impact of short channel effects (SCEs) that consequently contributes to the increment in leakage current (I_{OFF}) and reduction in the drive current (I_{ON}) due to the effects cause by the shrinkage of the structure into the nanometer regime that have reduces the channel length. At the end, it is observed that DG FinFET has fulfilled good electrical properties with high I_{ON}, and low I_{OFF} based on the electrical characteristics analysed. However, comparatively, the VTH does not met the nominal value desired which is differed by 3.3304% higher than, while still within the ranges of 0.676±12.7% V predicted by the ITRS 2013. Ideally, the device with substantial difference towards the increment of the I_{ON}/I_{OFF} ratio means that the device has met a superlative value that is due to increment in I_{ON} and lower I_{OFF} is obtained. In current analysis, the major difference between DG-FinFET with conventional planar MOSFET is in terms of leakage current value as it exceeded the minimum value predicted which is 20pA as specified by the ITRS 2013. Besides, the device characteristics have met the requirement of low power (LP) multigate (MG) technology predicted by the ITRS 2013.

ACKNOWLEDGEMENTS

The authors would like to thank the Ministry of Higher Education (MOHE) for sponsoring this work under project (FRGS/1/2017/TK04/FKEKK-CeTRI/F00335) and MiNE, CeTRI, Faculty of Electronics and Computer Engineering (FKEKK), Universiti Teknikal Malaysia Melaka (UTeM) for the moral support throughout the project.

REFERENCES

[1] Subrahmanyam B and Jagadesh Kumar M. Recessed source concept in nanoscale vertical surrounding gate (VSG) MOSFETs for controlling short-channel effects *Phys. E Low-Dimensional Syst. Nanostructures*. 2009; 41(4); 671–676.
[2] Wu M, Jin X, Kwon H I, Chuai R, Liu X, and Lee J H. The optimal design of junctionless transistors with double-gate structure for reducing the effect of band-to-band tunneling *J. Semicond. Technol. Sci.* 2013; 13(3): 245–251.
[3] Bhattacharya D and Jha N K. FinFETs: From devices to architectures. *Digit. Analog Analog. Digit. IC Des.* 2015; 2014: 21–55.
[4] Gupta K A, Anvekar D K, and Venkateswarlu V. Modeling of Short Channel MOSFET Devices and Analysis of Design Aspects for Power Optimisation *Int. J. Model. Optim.* 2013; 3(3) 266–271.
[5] Bakar A R A and Saad I. Investigation on effect of tilt angle ion implantations for vertical double gate MOSFET *2011 IEEE Reg. Symp. Micro Nanoelectron.* 2011; August 2016: 100–103.
[6] Kuhn K J. *CMOS scaling for the 22nm node and beyond: Device physics and technology*. *Int. Symp. VLSI Technol. Syst. Appl. Proc.* Hsinchu. 2011; 2011: 2-3.
[7] Skotnicki T, Hutchby J A, and King T. The End of CMOS Scaling *IEEE Circuits Devices Mag.* 2005; 21(1): 16–26.
[8] Miao J, Zhang S, Cai L, Scherr M, and Wang C. Ultrashort Channel Length Black Phosphorus Field-Effect Transistors. *ACS Nano*. 2015; 9(9): 9236–9243.

[9] Ferain I, Colinge C A, and Colinge J P. Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors. *Nature*; 2011:479(7373): 310–316.
[10] Kumar M J, Venkataraman V, and Nawal S. A simple analytical threshold voltage model of nanoscale single-layer fully depleted strained-silicon-on-insulator MOSFETs. *IEEE Trans. Electron Devices*. 2006; 53(10): 2500–2506.
[11] Kumar V, Gupta R, Preet R, Singh P, and Vaid R. Performance Analysis of Double Gate n-FinFET Using High-k Dielectric Materials. *Int. J. Innov. Res. Sci. Eng. Technol.* 2016; 5(7): 13242–13249.
[12] Nowak E J, Aller I, Ludwig T, Kim K, Joshi R V, Ching-Te Chuang, Bernstein K, and Puri R. Turning silicon on its edge. *IEEE Circuits Devices Mag.* 2004; 20(1): 20-31.
[13] Chaudhuri S M and Jha N K. 3D vs . 2D Device Simulation of FinFET Logic Gates under PVT Variations. *ACM J. Emerg. Technol. Comput. Syst.* 2014; 10(3).
[14] Feng P. Design, Modeling and Analysis of Non-classical Field Effect Transistors," *Electr. Eng. Comput. Sci. - Diss.*, 2012.
[15] Keerti K, Anil P, and Rao B. Parametric Variation with Doping Concentration in a FinFET using 3D TCAD. *Int. Conf. Microelectron. Circuits Syst.* 2014; 21–23.
[16] Leung G, Lai L, Gupta P, and Chui C O. Device- and circuit-level variability caused by line edge roughness for sub-32-nm FinFET technologies. *IEEE Trans. Electron Devices*. 2012; 59(8): 2057–2063.
[17] Srivastava A, Sylvester D, and Blaauw D. Statistical Optimization of Leakage Power Considering process variations using dual-Vth and sizing *Proceedings of the 41st annual Design Automation Conference.* San Diego. 2004; 773-778.
[18] Surwadkar T, Makdey S, and Bhoir D. Upgrading the Performance of VLSI Circuits using FinFETs *International Journal of Engineering Trends and Technology*. 2014; 14(4): 179–184.
[19] Wagadre A and Mane S. Design & Performance Analysis of DG-MOSFET for Reduction of Short Channel Effect over Bulk MOSFET at 20nm. *Engineering.* 2014; 4(7): 30–34.
[20] OushpaK KB and Sunkara S. Performance of 14nm SOI FinFET with ZrO 2 dielectric : A Comparative Study. *Int. Journal of Engineering Research and General Science* 3. 2015; 3(2): 299–305.
[21] Hajare R, Kumar A, and Jain S, and As S. Performance Analysis of FinFET Based Inverter circuit, NAND and NOR Gate at 22nm and 14nm Node technologies. *International Journal on Recent and Innovation Trends in Computing and Communication*. 2015; 3(5): 2527–2532.
[22] Sethupathy B and Aruna Priya P. Simulation and Performance of Double Gate FinFET Devices. International Journal of Advanced Research in Computer Science & Technology. 2014; 2(2): 43–45.
[23] Verma S, Srivastava P, and Srivastava N. Performance Evaluation and Comparative Study of Double Gate SOI MOSFET and FinFET using Silvaco TCAD Tool. *International Journal of Scientific & Engineering Research.* 2015; 6(2): 15-19.
[24] Kim D, Kang Y, and Kim Y. *Simple and accurate modeling of double-gate FinFET fin body variations*. 2012 Int. Conf. Synth. Model. Anal. Simul. Methods Appl. to Circuit Des. Seville. 2012; 2012: 265–268.
[25] Silvaco I. *Atlas User's Manual*. Silvaco, Inc., Report number: 408. 2016.