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A Nine Level Cascaded Multi Level Inveter Using Embedded and Flip Flops

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Abstract

This paper proposes a nine level cascaded multilevel inverter based on the flip flops and logic gates. Generally multilevel inverter is used to achieve the high power by using a series of power semiconductor switches with the several dc voltage sources which is used to perform the power conversion. In this paper the flip flop based CMLI is compared with the conventional CMLI. The flip flops and logic gates are used to create logic equation for the each switch of the CMLI by using the switching states. This proposed topology is mainly used to reduce the total harmonic distortion and also increase the performance of the system.

Keywords*: CMLI, PWM, embedded controller, flip flops, logic gates*

1. Introduction

In recent years multilevel inverters have gained much attention in the application areas of medium voltage and high power due to their various advantages such as lower common mode voltage, lower stress on power switches and lower harmonic contents in output voltage and current. Flip flop is the basic storage element in sequential logic. Flip flops can be divided into four flip flops: SR flip flops, JK flip flop, D flip flop and T flip flop. Pharne [1] proposed a review on various types multilevel inverter. Krishna Kumar et al [2] developed a new topology which contains the symmetric input DC sources. Nedumgatt et al [3] made new topology of cascaded multilevel inverter. Javad Ebrahimi et al [4] developed a topology in which the dc voltage sources can be reduced. K.K.Gupta et al [5] proposed a new topology of multilevel inverter which increases the number of levels and decreases the switches. Damoun Ahmadi et al [6] made a multilevel inverter topology which decreases harmonics. Faete Filho et al [7] developed the harmonic elimination method for eleven level cascaded multilevel inverter. Mariusz Malinowski et al [8] present a survey of different topologies, control strategies and modulation techniques for cascaded multilevel inverter. Tiantong Hu et al [9] described an asymmetrical multilevel inverter and its controlling method. Domingo Ruiz-Caballero et al [10] presents a hybrid multilevel inverter for high power applications. Holmes D.G et al [11] proposed the multicarrier PWM strategies for multilevel inverter topologies. N.S.Choi et al [12] developed a PWM method for multilevel inverter topology.

2. Conventional System

The schematic diagram of nine level conventional systems is shown in Figure 1. In this method the carrier signals are given as the input and the nine level output can be obtain. It is the asymmetrical topology and it contains Two H Bridges, in which the voltage sources are Vdc, 3Vdc.

The simulation output of nine level conventional cascaded multilevel inverter is shown in Figure 2.

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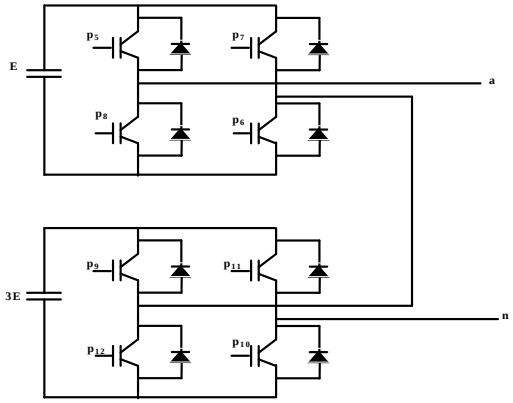

Figure 1. Nine level Conventional CMLI

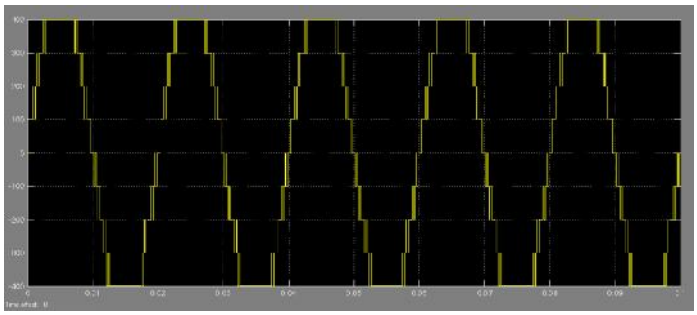

Figure 2. Simulation output of nine level Conventional CMLI

The total harmonic distortion (THD) analysis of the conventional method is shown in Figure 3.

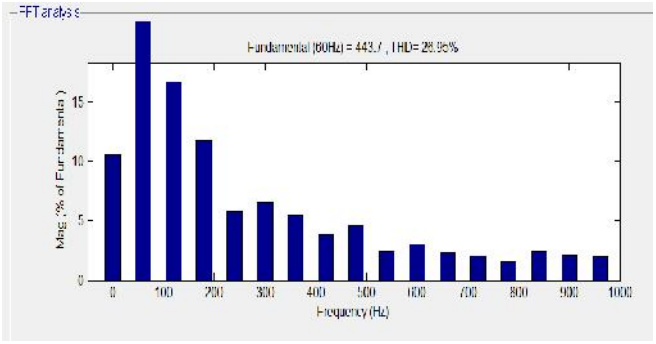

Figure 3. THD analysis for nine level Conventional CMLI

3. Embedded Controller Based Cascaded Multilevel Inverter

The next topology is nine level cascaded multilevel inverter based on the embedded controller. The switching states are given as the input by using the MATLAB/SIMULINK. The inputs are given in the form of Mat lab coding. This method can be producing the nine level output with reduced total harmonic distortion than the conventional method. The schematic diagram of embedded controller based CMLI is shown in Figure 4.

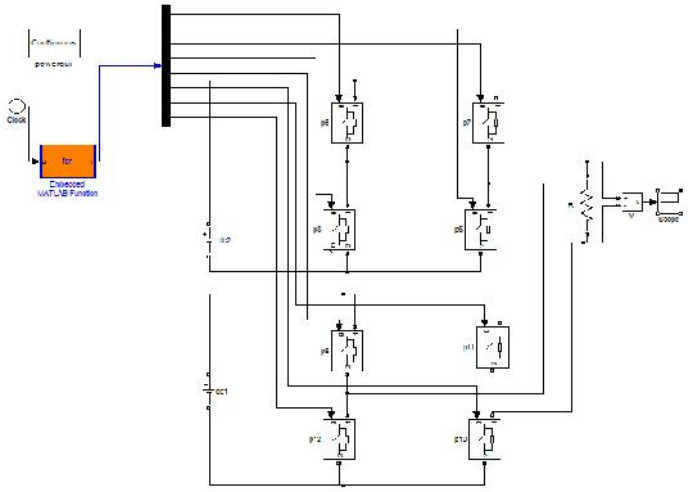

Figure 4. Embedded Controller based nine level Cascaded Multilevel inverter

The nine level simulation output of embedded controller based cascaded multilevel inverter is shown in Figure 5.

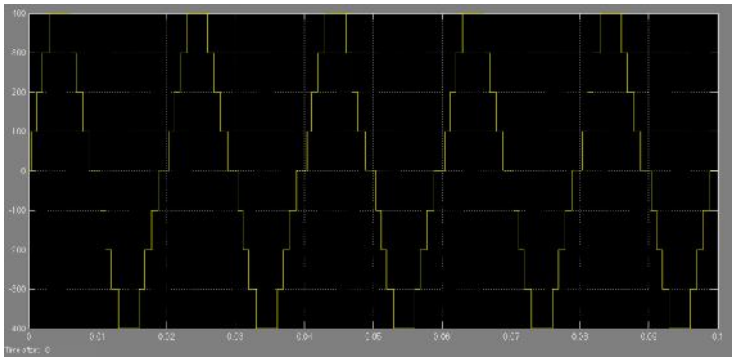

Figure 5. Simulation output of Embedded Controller based nine level CMLI

The THD analysis for the above method is shown in Figure 6.

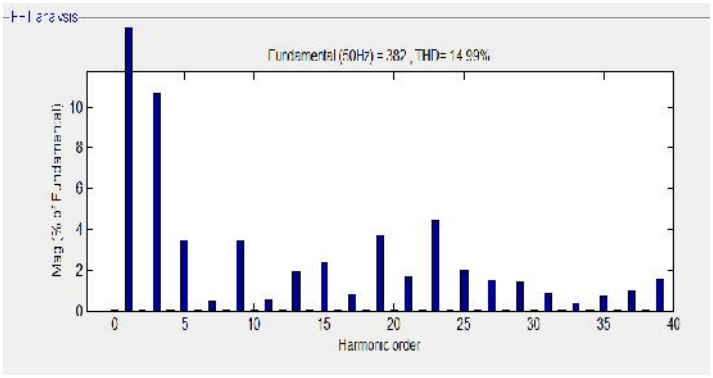

Figure 6. THD analysis for Embedded Controller based nine level CMLI

4. Proposed Flip flop Based Cascaded Multilevel Inverter

The proposed flip flops based nine level cascaded multilevel inverter is shown in Figure 7. In this method the Boolean equations are given as the input for the each switch of the CMLI. This asymmetric method contains eight switches and voltage sources are Vdc, 3Vdc. The Boolean equations can be forming by using the flip flops and the logic gates. Each switch requires number of logic gates. By using the switching states the Boolean equations can be formed. The total harmonic distortion of the flip flop based method can be reduced than the conventional and embedded controller based method. The performance of this method also increased than the previous methods. The switching losses also will be reduced.

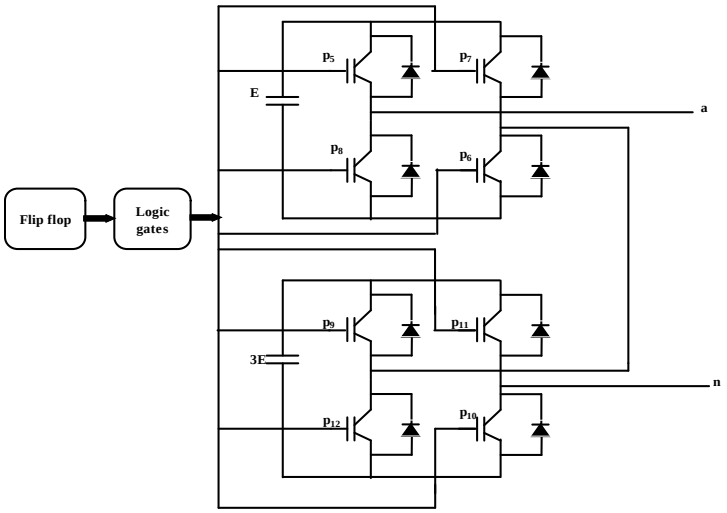

Figure 7. Nine level Cascaded Multilevel inverter based on Flip flops

Table 1. Switching states of proposed flip flop based nine level CMLI

Switching states								Output voltage
P1	P2	P3	P4	P5	P6	P7	P8	
1	1	0	0	1	1	0	0	4Vdc
0	1	0	1	1	1	0	0	3Vdc
0	0	1	1	1	1	0	0	2Vdc
1	1	0	0	0	1	0	1	Vdc
0	1	0	1	0	1	0	1	0Vdc
0	0	1	1	0	1	0	1	-Vdc
1	1	0	0	0	0	1	1	-2Vdc
0	1	0	1	0	0	1	1	-3Vdc
0	0	1	1	0	0	1	1	-4Vdc

The above table represents the switching states of the asymmetric cascaded multilevel inverter based on the flip flops and the logic gates. At the level of 4Vdc, the switches P1, P2, P5, and P6 will be turned ON and the remaining switches will be turned OFF. In the 3Vdc level P2, P4, P5 and P6 switches should be turned ON. The 2Vdc level contains P3, P4, P5 and P6 switches will be turned ON. At the level of Vdc, P1, P2, P6 and P8 switches are turned ON and P2, P4, P6, P8 switches must be turned ON in 0Vdc level. The Boolean equations can be formed by using the above switching states. The Boolean equations for this topology are listed below.

S1= D'C'B'A+D'CB'A'+DBA'+D'CBA (1)

S2=C'B'A'+C'BA+D'B'+DBA'+CB'A+D'A (2)

S3=DC'B'A+DCB'A'+D'BA'+DCBA (3)

S4=C'B'A'+C'BA+D'BA'+DB'+CB'A+DA (4)

S5=D'BA'+D'CB'+D'C'B (5)

S6=CBA+C'B'+D' (6)

S7=DBA'+DCB'+DC'B (7)

S8=CBA+C'B'+D (8)

The simulation output of flip flop based CMLI is shown in Figure 8.

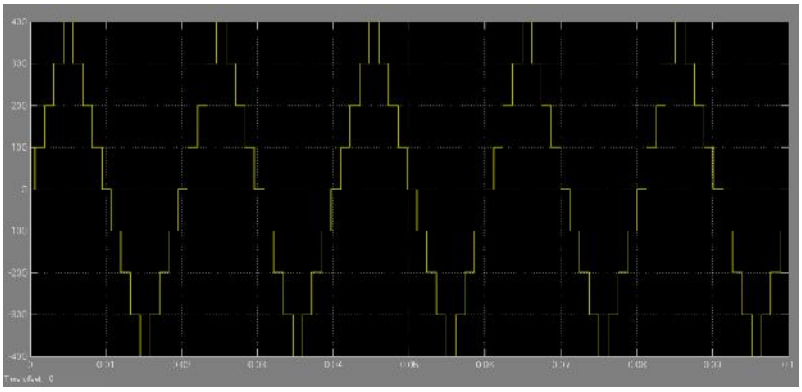

Figure 8. Simulation output of Proposed Nine level Cascaded Multilevel inverter

The THD analysis for flip flop based proposed method is shown in Figure 9.

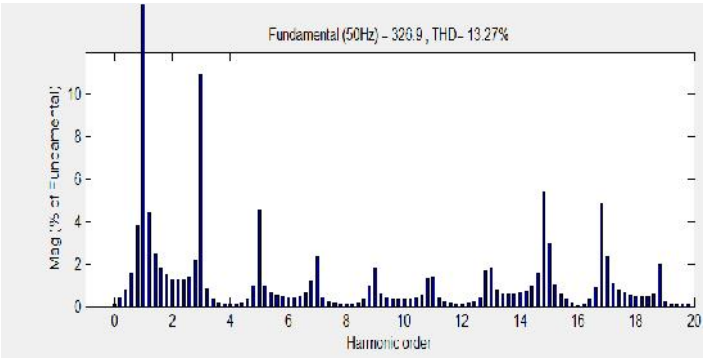

Figure 9. THD analysis for Flip flop based nine level CMLI

Table 2. THD values of three topologies

Multilevel inverter	Conventional CMLI	Matlab based CMLI	Proposed Flip flop based CMLI
Total Harmonic Distortion	26.95%	14.99%	13.27%

5. Conclusion

In this paper flip flop based nine level cascaded multilevel inverter is proposed. This topology is compared with the conventional method and the embedded controller based method. This topology can produce the nine level output which are nearer to the sinusoidal

waves. The total harmonic distortion of the proposed topology can be reduced than the conventional and the embedded controller method. This topology is also used to increase the performance of the system.

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