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Phase Disposition PWM Technique for Eleven Level Cascaded Multilevel Inverter with Reduced Number of Carriers

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Abstract

Applying pulse width modulation (PWM) techniques for cascaded multilevel inverters are very complex for topologies with reduced number of switches. In this paper for phase disposition (PD) pulse width modulation technique a new algorithm is proposed and implemented on eleven level cascaded multilevel inverter under reduced switches topology. In the proposed algorithm instead of N-1 carrier waves, the required number of switching pulses generated by considering number of carrier waves is equal to number of switches. This technique allows lower switching transition and it leads to reduced switching losses for topologies utilize minimum number of switches. 1.2 KHz carrier frequency is used to generate switching pulses and verified up to 100 kHz. The Total harmonic distortion is observed for various switching frequencies. The obtained output voltage levels using PD PWM technique proved mathematically. The performance of proposed algorithm is evaluated using Matlab/Simulink.

Keywords: *cascaded multilevel inverters, diagonal dc source, phase disposition (PD) PWM technique*

1. Introduction

In recent years several topologies are presented for cascaded multilevel inverter under reducing switches concept, some of them are symmetrical and asymmetrical. The advantages of above all structures is the low variety of dc voltage sources, which is the most important feature in determining cost of the inverter [1], multilevel converters have some particular disadvantages. They need a large number of power semiconductor switches, which increase the cost and control complexity and reduce the overall reliability and efficiency [2]. To minimize above mentioned disadvantages voltage levels are increased with minimum dc voltage sources [3] and switches. In multilevel inverters the power quality is improved as the voltage levels increases at the output voltage and can sustain the operation in case of internal fault [4]. Using series and parallel operation of dc voltage sources for eleven levels of output voltage topology presented in [5] utilizes 10switches and 3 dc voltage sources and bus voltage THD is 13.1% but with the topology presented in Figure 1, eleven voltage levels are obtained using only 9switches and 2 dc voltage sources, therefore the topology presented in Figure 1 is smaller because the number of switching devices are reduced and bus voltage THD is 9.2% is also less. PV cells, batteries, capacitors etc. can be used as voltage sources for the presented diagonal dc source cascaded MLI. The phase disposition technique produces fewer harmonic because it puts harmonic energy directly into a common mode carrier component which cancels across line to line output [6].

In this paper Phase disposition modulation technique is implemented with new algorithm to generate switching pulses to turn on S1, S2, S3, S4, S5 which connects dc voltage sources in series and parallel and the output voltage collected across RL load. In the proposed phase disposition algorithm N-6 carrier signals(equal to switches present in polarity generation circuit) are taken and are compared with sinusoidal reference to achieve gate pulses for generating eleven levels output. It allows lower switching transitions leads to reduced losses in

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the circuit. The total harmonic distortion observed for varying switching frequencies from1.2kHz to 100 kHz.

2. Mathematical Analysis of Diagonal Dcsource Cascaded Multi Level Inverter

The expected output voltages were calculated during each mode of operation by taking each switch resistance 1mΩ using Kirchhoff's laws. Based on the expected voltage across PQ the respective switches S1, S2, S3, S4 and S5 will be turned ON and OFF and correspondingly switching frequency of the carrier signals are selected.

Mode 1: When s3 and s5 are switched on the voltage across PQ

$$VPQ = 0 \quad (1)$$

Mode 2: When the switches s1, s3, and s5 are turned on the following equations can be written.

$$i1x + i2x + \cdots inx = v1 \quad (2)$$

$$i1x = i2x = ia \quad (3)$$

$$ia = \frac{v1}{2} \quad (4)$$

During this interval the voltage available across PQ is $\frac{v1}{2}$

Mode 3: When s1, s2, s3 and s5are switched on the following equation can be written.

$$i1x + i2x + .. inx = v1 \quad (5)$$

$$i1x = i2x = ib \quad (6)$$

$$ib = \frac{v1}{2} \quad (7)$$

The voltage present across Pn is $\frac{v1}{2}$ and,

$$i3x + i4x + \ldots inx = v2 - v1 \quad (8)$$

$$i3x = i4x = ic \quad (9)$$

$$ic = \frac{v2-v1}{2} \quad (10)$$

From above equation the voltage present across PQ is $=VPn + VnQ = \frac{v1}{2} + \frac{v2}{2} - \frac{v1}{2} = \frac{v2}{2}$.

Mode 4: When switches s1, s2 and s5 are switched on, the following equation can be written.

$$i5x + i6x + \cdots inx = v2 - v1 \quad (11)$$

$$i5x = i6x = id \quad (12)$$

$$id = \frac{v2-v1}{2} \quad (13)$$

The voltage present across PQ is $v1 + \frac{v2-v1}{2} = \frac{v1+v2}{2}$.

Mode 5: When switches s1, s2, s4, and s5 are switched on.

$$2i7x + i8x = v1 \quad (14)$$

$$i7x + 2i8x = v2 \quad (15)$$

Solving above equation we get voltage across PQ is:

$$VPQ = v1 + \frac{v2}{2} \quad (16)$$

Mode6: when s1, s2 and s4 are turned on the voltage across PQ is:

$$VPQ = \frac{v1}{2} + v2 \quad (17)$$

Where,

$I1x, i2x, i3x, \ldots . inx$ *are respective loop currents,* $v1, v2 \ldots$
Vn voltages applied across respective cell

3. Diagonal DC Source Cascaded Multi Level Inverter

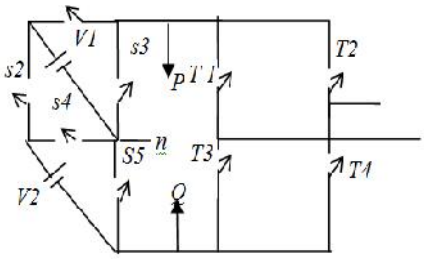

Figure 1. Diagonal DC Source Cascaded MLI

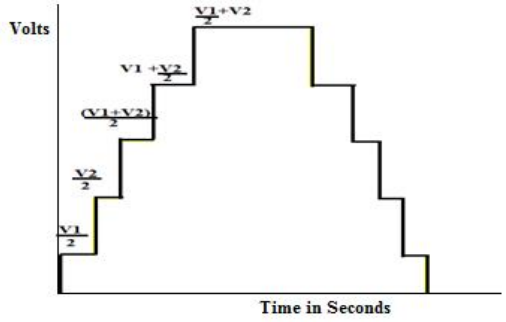

Figure 2. Output voltage across PQ

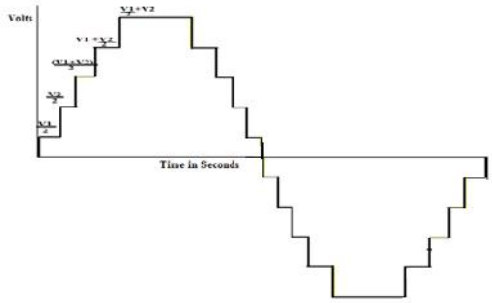

Figure 3. Output of polarity generation circuit

The diagonal dc source cascaded multilevel inverter consist of two circuits (1) Polarity generation is used for generating only positive voltage levels as shown in Figure 2. (2) Polarity conversion circuit is used for converting positive polarity into both positive and negative polarity voltage levels. The output of the polarity conversion circuit is shown in Figure 3.

The operation of diagonal dc source cascaded MLI divided into six modes i.e. mode0, mode1, mode2, mode3, mode4, mode5 the switching sequence in every mode and corresponding voltages listed in Table 1. The major advantage with the algorithm applied in phase disposition pwm is that the selected switching sequence allows half of the applied voltages across polarity generation circuit, this gives reduced voltage stresses across the switches.

Table 1. Switching sequence for eleven level diagonal DC source cascaded mli

Level	0	1	2	3	4	5
Mode						
1	S3,S5	S1,S3,S5	S1,S2,S3 ,S5	S1,S2,S5	S1,S2,S4,S5	S1,S2,S4
Output Voltage (Volts)	0	$\overline{S3,S}$ $\frac{V1}{2}$	$\overline{2,S3}$ $\frac{V2}{2}$	$\overline{51,S2,S5}$ $\frac{V1+V2}{2}$	$\overline{,S2,S4,S5}$ $V1+\frac{V2}{2}$	$\overline{S1,S}$ $\frac{V1}{2}+V2$

4. Proposed Phase Disposition PWM Technique Algorithm Based on Mathematical Analysis

In this paper the target is to generate switching pulses for switches S1, S2, S3, and S4and S5 shown in Figure 1 at the desired time intervals. First time attempt was made to generate switching pulses using phase disposition pulse width modulation technique, an algorithm is proposed for reducing switches topologies.

In Phase disposition PWM technique N-1 carrier waves are used to generate N level output in conventional cascaded H bridge topologies [7]. But with the proposed algorithm for generation of eleven level cascaded MLI under reduced switches topology the number of triangular carrier signals are equal to number of switches in polarity generation circuit, for generating eleven level only five triangular carrier signals are used.

Five triangular carrier signals are compared with sinusoidal reference signal at their respective time of intervals as shown in Figure 4. The selection of triangular carrier frequency plays key role for obtaining required width of pulses [8]. The generated pulses shown in Fig6.This technique greatly reduce the complexity in pwm circuit because of less number of carriers.

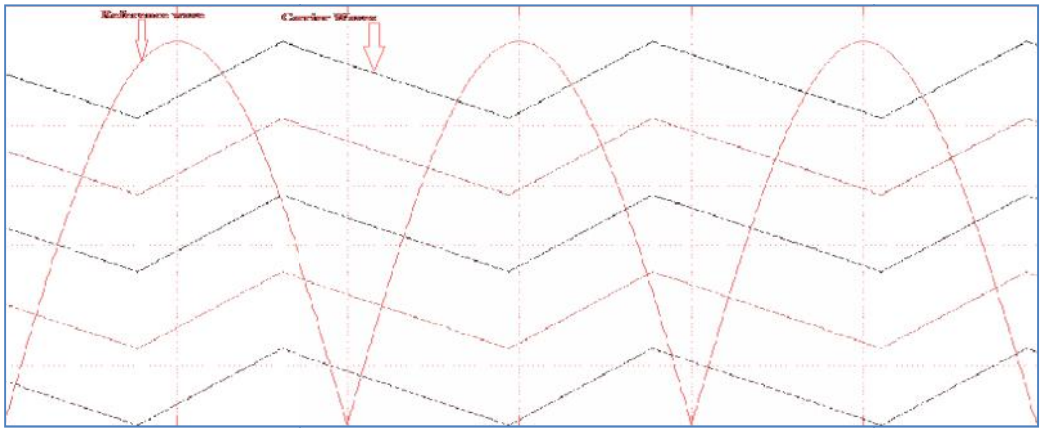

Figure 4. Reference and carrier signals in Proposed Phase Disposition PWM Technique for Eleven level Diagonal DC source Cascaded MLI

5. Switching Pulses Generation with the Proposed Phase Disposition PWM Technique Algorithm

The design of the inverter is done using various factors; these factors are obtained from various parameters that contribute the efficiency of inverter.

The switching frequency is estimated using frequency modulation index is given by $Mf = \frac{fc}{fr}$.Where *fc* and *fr* are carrier wave and reference wave frequency.

The amplitude modulation index is defined as:

$$M = \frac{Vr}{(n-1)Vc}$$

Where the Vm peak to peak value of the reference wave and Vc are the amplitude of the carrier wave The THD is measured as the ratio of all the harmonics in a switching system to the fundamental unit [9].

$$THD = \frac{\sqrt{\sum_{i=2}^{n} A}}{A}$$

Where, Ai is the ith voltage/current harmonic value. Pulse width modulated systems are usually characterized with power and harmonic losses which result from the switching and conduction losses of the switches/transistors/thyristors that are sed. The losses in the modulation techniques cause the average reduction in phase-phase voltages at each switching frequencies [10].

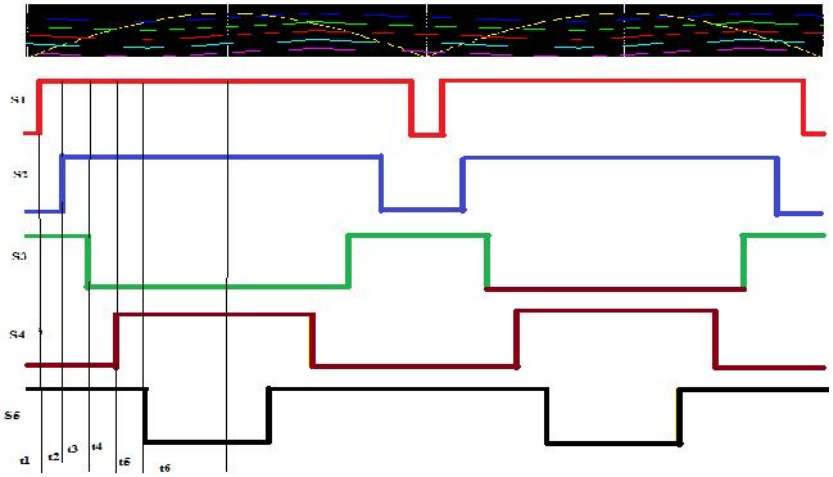

Figure 6. Switching Pulses in Proposed Phase Disposition PWM Technique

During each switching interval the magnitude of voltages present across PQ is represented below:

$0 \leq t \leq t1 = 0 volts$	*Switches S3, S5 are turned ON*
$t1 \leq t \leq t2 = \frac{v1}{2} volts$	*Switches S1, S3, S5 are turned ON*
$2 \leq t \leq t3 = \frac{v2}{2} volts$	Switches S1, S2, S3, and S5 are turned ON
$t3 \leq t \leq t4 = \frac{v1+v2}{2} volts$	Switches S1, S2, S5 are turned ON
$t4 \leq t \leq t5 = v1 + \frac{v2}{2} volts$	Switches S1, S2, S4, and S5 are switched ON
$t5 \leq t \leq t6 = \frac{v1}{2} + v2 volts$,	Switches S1, S2, S4 are switched ON

The above obtained voltage magnitudes during each interval are verified mathematically in section 2 and obtained voltage magnitudes matching with the simulated results.

6. Simulation Circuit

The diagonal DC source cascaded multilevel inverter circuit shown in Figure 1. To generate switching pulses Phase disposition PWM technique is employed. For generating required number of switching pulses under proposed algorithm the below simulink circuit is designed. To generate five switching pulses, five carrier signals compared with the positive peak of the sinusoidal signal. All carrier signals switching frequency is selected as 1.2 kHz and 50 Hz reference signal is compared with the carrier signals. The wave forms observed for a modulation index unity.

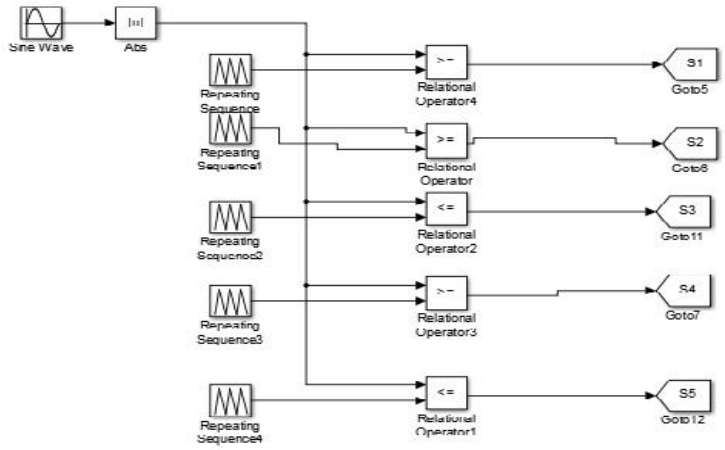

Figure 7. Phase Disposition PWM Circuit for generating switching pulses with the proposed algorithm

7. Results and Discussions

The proposed algorithm for Phase Disposition PWM technique simulated using Matlab/SimulinkR2013version. For observing proposed algorithm to generate required switching pulses eleven level diagonal dc source cascaded multilevel inverter is considered with RL load as R=45Ω and L=55mH. Voltage and Current wave forms are recorded and it was observed that with the proposed algorithm the THD is reduced. For the voltage wave the THD is 9.2% and the current THD is 3.86%, Variation of THD with respect to switching frequency listed in the Table 2. It is observed that the voltage THD is slightly increasing with the switching frequency at 100 kHz is 11.40% and the current THD is reducing with the switching frequency at 100 kHz switching frequency its value is only 0.73%. The magnitudes of voltages are matching with the mathematically calculated values.

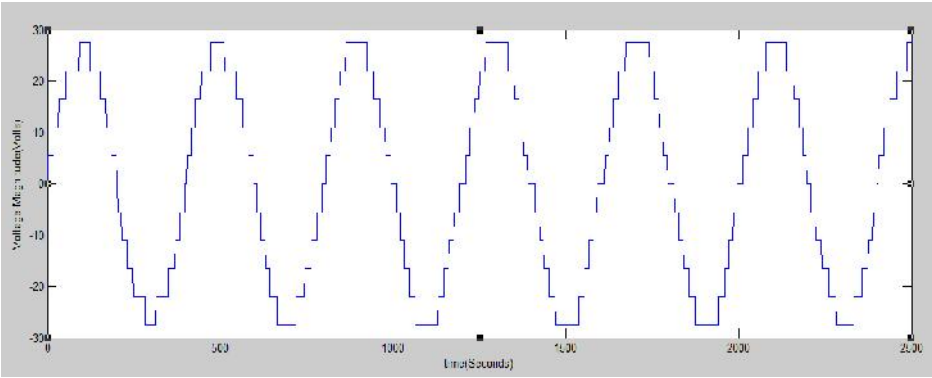

Figure 8. Voltage Wave Form of Eleven Level Diagonal Dc Source Multilevel Inverter with the Proposed Algorithm for Switching frequency (*fs*) =1.2 kHz

Table 2. Total Harmonic Distortion For Various Switching Frequencies (Fs)

Switching frequency(*fs*)	5 kHz	10 kHz	100 kHz
% Voltage THD	10.62	10.87	11.40
% Current THD	3.03	2.57	0.73

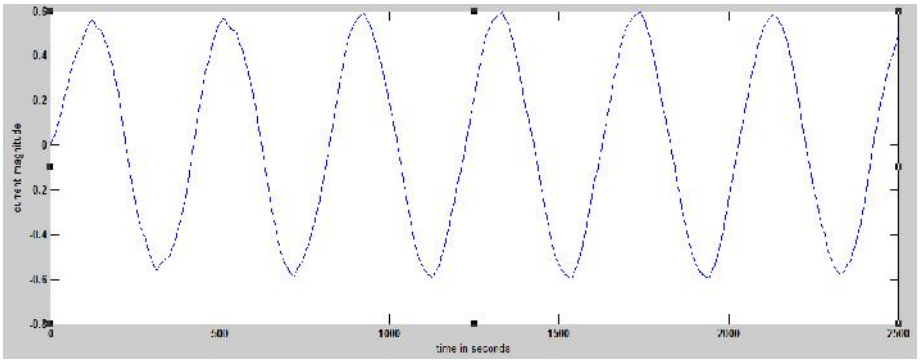

Figure 9. Current Wave Form of Eleven Level Diagonal DcSource Multilevel Inverter with the Proposed Algorithm for switching Frequency (fs) =1.2 kHz

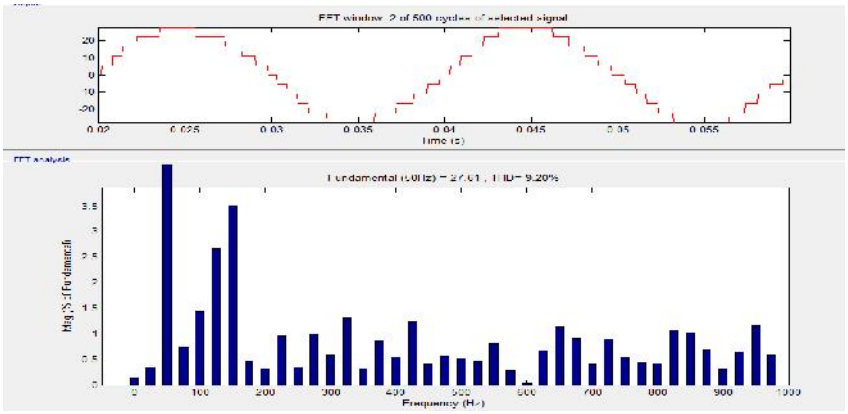

Figure 10. Voltage Waveform FFT at Switching Frequency (fs) =1.2 kHz

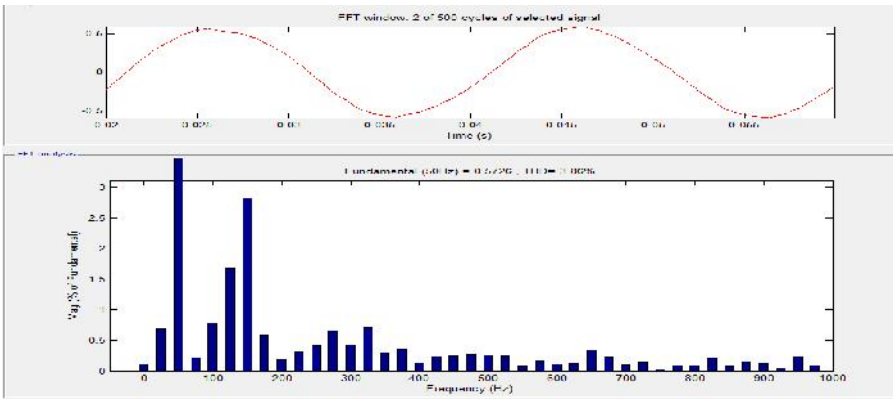

Figure 11. Current Wave FFT at a Switching Frequency (fs) = 1.2 kHz

8. Conclusion

In this paper new algorithm was proposed to Phase Disposition PWM technique and implemented on diagonal dc source cascaded multilevel inverter under reduced switches topology and it was verified for switching frequencies of 1.2kHz, 5kHz, 10kHz and 100kHz at unity modulation index using Simulink. The proposed modulation technique increase number of levels and reduce total harmonic reduction. The output voltage and current total harmonic

distortion percentages listed in Table 2. In the future the Simulink results are verified with hardware prototype.

Ackowneledgements

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