# High gain boost converter with modified voltage multiplier for stand alone PV system

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# Boost converters of high gain are used for photo voltaic systems to obtain high efficiency. These high gain Boost converters gives increased output voltage for a low input t voltage. The High gain boost converters have the following merits. Conduction losses input current ripple and stress across the switches is reduced while the efficiency is increases. The high gain of the converters with the above said merits is obtained by changing the duty cycle of switches accordingly. In this paper a boost converter working with interleaved concept along with a additional N-stage voltage Multiplier has been carried out by simulation using MATLAB/simulink and the mathematical modeling of various parameters is also done.

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# 1. INTRODUCTION

Non-conventional energy systems are becoming more efficient and affordable .These Renewable Energy sources is helping in increasing the energy security on an indigenous, inexhaustible and most importantly an independent source. It also increases the sustainability, reduce pollution and decrease the fossil fuel cost.

Solar power is the best reliable energy source when compared with other renewable sources. Once installed they require less maintenance with a considerable less pollution. A photovoltaic converts light energy into electric direct current energy. Photo voltaic is nowadays is used as a fast growing energy producing plant by continuous improvement in installation cost reduction.

Renewable energy systems produce low output voltage. Hence high gain dc-dc converters are used to increase the low input voltage to boosted output voltage. The output obtained from such high gain boost converters are fed to a suitable inverter which converts the dc voltage to ac voltage and used by ac loads. Figure 1 shows the block diagram of Stand Alone PV system. It shows the basic units required for the conversion of light energy into usable ac and dc power.

Boost converters are the basic converter topology for achieving increased output. A single photo voltaic panel can only produce 15-45 V dc that has to be stepped up to 400 V dc. An interleaved boost converter with coupled inductors and clamping capacitors are the emerging design technic used to increase the voltage output [1]. The conventional interleaved boost converter can be used for high-power applications and power factor correction [2], [4]. But these converters have some difficulty in obtaining stepped up voltage. Only with 0.9 duty cycle a boost converter produces high voltage gain which results in instability of the converter [3], [6], [8], [9]. Unfortunately, the voltage conversion ratio (i.e) the gain is limited and the voltage stresses across power switches are equal to output voltage [10]. The first section explains the

interleaved converter with modified voltage multiplier module , the second section explains the modes of operation and the third section shows the design calculations along with the simulation results.

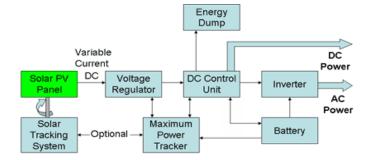


Figure 1. Block diagram of Stand Alone PV system

# 2. PROPOSED DC-DC CONVERTER TOPOLOGY

The proposed topology is an Interleaved Boost converter with modified voltage multiplier as shown in Figure 2. This combines the interleaved boost converter, the coupled inductor and switched capacitor function to provide the require output voltage at the desired power level. The modified topology is a two switch design, employing two coupled inductors, capacitors and diodes for an N stage voltage multiplier. The main advantages of this topology are (1) high gain without transformers; (2) two switch topology; (3) continuous input current (4) easily expanded to give higher voltage gain.

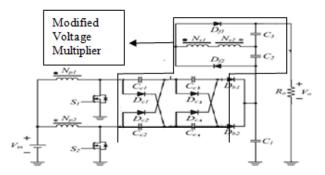


Figure 2. Circuit Diagram of Interleaved Converter with Modified Voltage Multiplier

# 3. MODES OF OPERATION

Operation principle of this converter is same as the converter with interleaving concept along with a voltage multiplier. The voltage multiplier is modified by adding one stage of voltage multiplier along with the existing topology. The multiplier circuit consisting of two feedback diodes and four clamping capacitors, is inserted between conventional interleaved boost converters and output side to form a modified interleaved boost converter. During switch OFF condition it works like fly back converter, and when switch is in ON condition works as a forward converter. The operating modes are shown in Figure 3 and explanation is given below.

MODE I:

The switching operation of the power switches are as shown in Mode I as in Figure 3(a) circit diagram. Inductor Lm1 continues to charge the coupled inductors. The stored energy in the leakage inductance Ls is supplied to the output terminal via a feedback diode Df2 which is alone forward biased. MODE II:

The switches and diodes conductions are as shown in Figure 3(b). Since the switches are in ON state the voltage source Vin is fed to the leakage inductors  $L_{k1}$  and  $L_{k2}$ . Hence the current through them increases linearly.

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#### MODE III:

In this mode the switch  $S_1$  is still ON and switch  $S_2$  begins to turn OFF. The clamping capacitor  $C_{c1}$  and  $C_{c3}$  clamps the potential on the switch  $S_2$ . The output voltage of the boost converter is doubled due to the energy transfer from input voltage (Vin), inductors  $L_{m2}$ ,  $L_{k2}$  and capacitors  $C_{c2}$ ,  $C_{c4}$ . MODE IV:

The distribution of current in the magnetizing circuits helps the current  $ini_{Dc2}$  decrease to zero naturally.Both power switches and all diodes remain in previous states except the clamp diodeD<sub>c2</sub>, as shown in Figure 3(d)

# MODE V:

The switching of switches and the biasing of diodes is as shown in Figure 3(e). The load across the output terminal is fed with the energy released from the series inductance  $L_s$  through diode  $D_{fl}$ . The secondary side of the winding  $N_{s1}$  and  $N_{s2}$  receives energy from  $L_{m2}$ . The currents in leakage inductors  $L_{k2}$  and  $L_{k1}$  increases and decreases respectively.

MODE VI:

The power electronic switches are still in ON condition and biasing of the diodes is as shown in Figure 3(f). Inductors  $L_{k1}$  and  $L_{k2}$  increases linearly by the input supply voltage. MODE VII:

The switching of the power switches is same as that of mode I. The diodes that are in reverse biased, are shown in Figure 3(g). The energy stored in inductor  $L_{ml}$  is mutually transferred to the secondary side inductor windings  $N_{s1}$ ,  $N_{s2}$ . The current in inductor  $L_s$  is passed through the capacitor  $C_2$  to the output terminal via diodeD<sub>f2</sub>. The clamping capacitor  $C_{c2}$  reduces the switch voltage stress of switch S<sub>1</sub>. The input voltage source, magnetizing inductor  $L_{m1}$ , the inductor  $L_{k1}$ , and clamp capacitor  $C_{c1}$ ,  $C_{c3}$  discharges the stored energy MODE VIII:

The diode currents  $i_{dc1}$  and  $i_{dc3}$  is reduced to zero This contributes to much reduction in conduction losses and the diode reverse recovery is completely nullified. Except for the clamping diodes  $D_{c1}$  and  $D_{c3}$  the switches and the other diodes remain in the preceding condition, as shown in Figure 3(h).

# 4. MATHEMATICAL ANALYSIS

#### 4.1. Output Voltage Gain

The output voltage is same as the voltage across the clamping capacitors  $C_c$ . It is given by,

$$V_{C_c} = \frac{2}{1-D} V_{in}$$
(1)

The voltages across the  $C_1$  and  $C_2$  are obtained using the principle of inductor voltage-second balance. Hence:

$$V_{C1} = \frac{2}{1-D}V_{in} + V_{C_c} = \frac{4}{1-D}V_{in}$$
(2)

The energy in the coupled inductors  $N_{p1}$  and  $N_{p2}$  are used to charge the filtering capacitors  $C_2$  and  $C_3$  at the output. When power switch  $S_2$  is in ON condition, the filter capacitor voltage ( $V_{C2}$ ) is equal to the voltages induced in  $N_{S1}$  and  $N_{S2}$ .Similarly when the power switch  $S_1$  is in ON, the filter capacitor's voltage  $V_{C3}$  is also equal to the voltage induced in  $N_{S1}$  and  $N_{S2}$ . Thus, voltages  $V_{C2}$  and  $V_{C3}$  can be is mathematically given as:

$$V_{C2} = V_{C3} = n. V_{in} \left( 1 + \frac{D}{1 - D} \right) = \frac{n}{1 - D} V_{in}$$
(3)

The voltage across the output can be derived from

$$V_0 = V_{c1} + V_{c2} + V_{c3} = \frac{2n+4}{1-D} V_{in}$$
(4)

The voltage step up ratio of the proposed converter is,

$$\frac{V_o}{V_{in}} = -\frac{2n+4}{1-D}$$
(5)

#### 4.2. Voltage Stress on Switches

The stress across the semiconductor switches are given as,

$$V_{S1} = V_{S2} = \frac{2}{1-D} V_{in} = \frac{1}{2n+4} V_o$$
(6)

From the above equation it is shown that a MOSFET with low voltage rating with less  $RDS_{on}$  can be employed to reduce the conduction losses. The voltage stress across the switch is reduced to one sixth even if the n is one. This considerable reduction in the conduction losses makes the proposed converter highly employable.

# 4.3. Voltage stress on diodes

The voltage stress on the diodes is equal to Vc1 derived as,  $V_{D(c \ 1 \ \& \ c2)} = V_{c1}$ , which is equal to  $V_{s1}$  or  $V_{s2}$ 

$$V_{Dc1} = V_{Dc2} = \frac{2}{1-D} V_{in} = \frac{1}{2n+1} V_{o}$$
(7)

For a turns ratio of 1 the voltage stress across the diodes is reduced to more than half of the output voltage. The stress on diode  $D_b$  is approximately equal to the stress on the switches and is derived as,

$$V_{Db1} = V_{Db2} = V_{C1} = V_{C2} = \frac{2}{1-D}V_{in} = \frac{1}{2n+4}V_0$$
 (8)

Similarly the stress on diode D<sub>f</sub> is

$$V_{Df1} = V_{Df2} = V_{c2} + V_{c3} = \frac{2nV_{in}}{(1-D)} = V_{Dc1}$$
(9)

#### when n is1

As the turns ratio increases the voltage stress on the diodes  $D_f$  increases but is always less than the output voltage [11].

#### 4.3.1 Selection of Capacitance and Inductance

The capacitance value is calculated from the following expression,

$$C = \frac{V_o DF}{R \Delta V_o}$$
(10)

Where,  $V_o$  the output voltage(V), D the duty ratio, F frequency (Hz), R resistance ( $\Omega$ ) and  $\Delta V_0$  represents the change in the output voltage (V).

The inductance value is given by

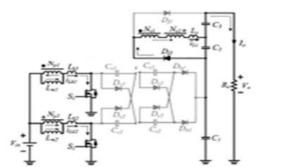
$$L = V_{in} * (V_0 - V_{in})$$
(11)

 $\Delta I_L * F_S * V_O$ 

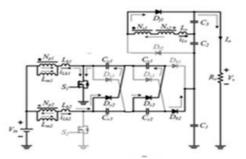
Where Current ripple,

$$\Delta I_{L} = (0.2 \text{ to } 0.4) * I_{OUTMAX} * V_{O}/V_{in}$$

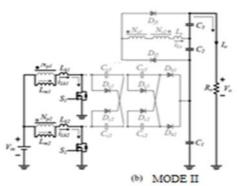
In this section, an interleaved boost converter with modified voltage multiplier is discussed. In the proposed system the voltage multiplier is been replaced by an N-stage voltage multiplier. By adding N-stage voltage multiplier to the existing converter gives the multiple of output voltage of interleaved converter with voltage multiplier. For example, for 2-stage voltage multiplier is implemented to converter gives double output voltage of converter.

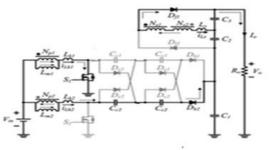




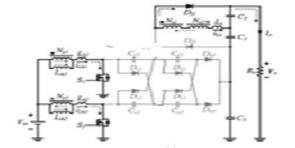


(c) MODE III

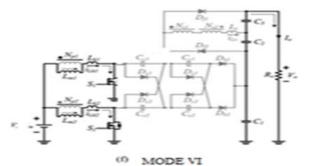




(d) MODE IV







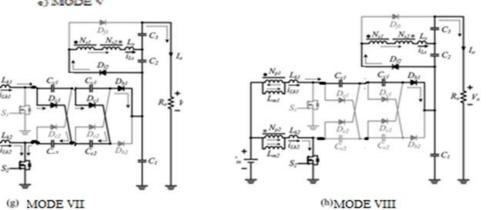


Figure 3. Operating modes of high gain interleaved boost converter with modified voltage multiplier

# 5. SIMULATION AND RESULTS

The proposed converter topology is simulated using MATLAB which is shown in Figure 4. The input voltage is 28 V and output voltage is 382 V, thereby the gain is 13 Figure 4 is the Simulation Circuit of Proposed converter in MATLAB.

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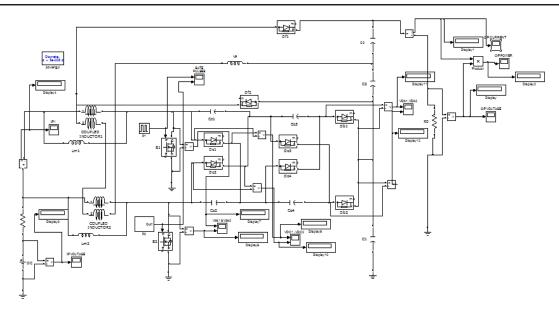


Figure 4. Interleaved Boost Converter with modified voltage multiplier

# 5.1. Input Voltage

Figure 5 shows an input voltage of 28V given as input to the proposed converter.

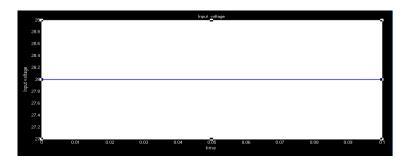


Figure 5. Input voltage 28V

# 5.2. Voltage Across The Switches

Figure 6 shows the voltages across the main switches  $S_1$  and  $S_2$  of interleaved converter with voltage multiplier as 131.4 V.

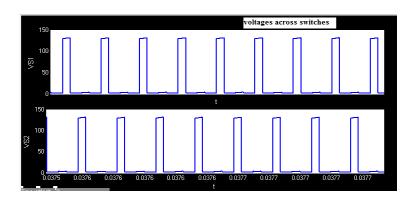


Figure 6. Voltages across the switches

# 5.3. Voltage Across Diodes

Figure 7 shows the simulated output waveforms of voltages across the clamping diodes.

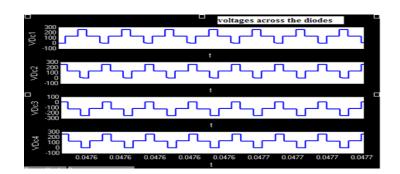


Figure 7. Voltages across the clamping diodes

# 5.4. Output Voltage

Figure 8 shows the output waveform of converter and output voltage as 382 V.

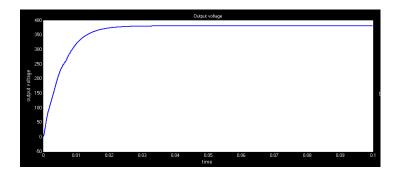


Figure 8. Output voltage of proposed converter

#### 6. CONCLUSION

In this paper an interleaved high gain DC-DC Boost Converter with a modified Voltage Multiplier is presented with mathematical analysis and the simulation results. The simulation results shows that for a an input voltage of 28V the output Voltage is 382 V with a duty cycle maintained at 0.65. The switching frequency is at 40 Hz. The gain is calculated as 13. The voltage stress across the switches is 131.4 which is approximately equal to 1/3 <sup>rd</sup> of the output voltage. Hence the voltage stress across the switch is reduced. The proposed converter has a very high step-up conversion gain of 13 through the voltage multiplier module. The interleaved structure reduces the input current ripple and distributes the current through each component. In addition, clamping capacitors does the function of recycling the leakage energy thus reducing the voltage stress across the power electronic switches.

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