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New Bipolar Hybrid Carrier PWM Strategies for Symmetrical Multilevel Inverter

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Abstract

In this paper, hybrid modulation methods suitable for H-bridge MLI are discussed. The results of experimental work using dSPACE system only are presented for three phase five level cascaded type inverter. Different hybrid carrier PWM (Pulse Width Modulation) strategies using sinusoidal reference, third harmonic injection reference, 60 degree reference and stepped wave reference for the chosen inverter are initially developed using SIMULINK. Strategies developed are then implemented in real time using dSPACE/RTI. The five level output voltages of the chosen MLI (MultiLevel Inverter) obtained using the dSPACE system based PWM strategies and the corresponding % THD (Total Harmonic Distortion) and V_{RMS} (fundamental) are presented and analyzed. It is seen that sinusoidal reference with PS+VF (Phase shift+Variable Frequency) and PS+PD (Phase Disposition) provides output with relatively low distortion. APOD+CO (Alternative Phase Dispostion+Carrier Overlapping) and CO+PD PWM strategy is found to perform better since it provides relatively higher fundamental RMS output voltage and relatively lower stress on the devices. It is displayed that THI (Third Harmonic Injection) reference with PS+VF and CO+PS provides output with relatively low distortion. APOD+CO and CO+PS PWM strategy is found to perform better since it provides relatively higher fundamental RMS output voltage and relatively lower stress on the devices. It is observed that 60 degree reference with PD+VF provides output with relatively low distortion. CO+PD PWM strategy is found to perform better since it provides relatively higher fundamental RMS output voltage and relatively lower stress on the devices. It is noted that stepped wave reference with APOD+PD and PD+VF provides output with relatively low distortion. APOD+CO and CO+PD PWM strategy is found to perform better since it provides relatively higher fundamental RMS (Root Mean Square) output voltage and relatively lower stress on the devices. The simulation and hardware results closely match with each other.

Keywords: *hybrid, THD, DSPACE, RTI, control desk*

1. Introduction

Multilevel voltage source inverters have recently emerged as very important alternatives in high power, medium voltage applications. The function of a MLI is to synthesize a desired AC output voltage from several DC voltage sources with extremely low distortion. The MLIs provide high output voltages with low harmonics without the use of transformers or series connected synchronized switching devices. As the number of output voltage levels increases, the harmonic content of the output voltage decreases significantly. Increasing the number of output voltage levels in the inverter without requiring higher ratings on individual devices can increase the power rating of load. MLIs offer several advantages. These include higher DC bus utilization, improved harmonic performance and reduced stress on power devices. MLIs find applications in adjustable speed drives, electric utilities and renewable energy systems. Initially the single phase cascaded MLI is implemented through FPGA. For each and every PWM strategies we need the separated coding to be written using verilog or xilink software. That coding should be downloading through emulater. So the problem identified is for a particular application the FPGA can be used. Then the memory available, processing speed is very less in FPGA. So the FPGA is replaced by dSPACE. The dSPACE is having more advantage compared to FPGA. In dSPACE either we may use DAC or IOs to interface the control circuit and power ciruit. In dSPACE there are many IOs, DAC, ADC and many interfacing ports are available. Compared to FPGA the DSPACE is easier to implement any power electronic circuits. Simulation studies on various multi-carrier PWM strategies for three phase cascaded type five level inverter followed by DSPACE based implementation are presented in this paper. The dSPACE DS 1103 is used

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to overcome the shortcomings of FPGA being usable for selective m_f only. Lee and Nojima [1] proposed a quantitative power quality and characteristic analysis of multilevel pulse width modulation methods for three level neutral point clamped medium voltage industrial drives. Gupta and Jain [2] suggested a topology for multilevel inverters to attain maximum number of levels from given dc sources. Najafi and Yatim [3] made a design and implementation of a new multilevel inverter topology. Roshankumar et al [4] discussed a five-level inverter topology with single dc supply by cascading a flying capacitor inverter and an H-bridge. Wu et al [5] developed two modulated digital control for three phase bidirectional inverter with wide inductance variation. José et al [6] discussed a generalized proportional integral tracking controller for a single phase multilevel cascade inverter. Younghoon Cho et al [7] proposed a carrier-based neutral voltage modulation strategy for multilevel cascaded inverters under unbalanced DC sources. Shweta Gautam and Rajesh Gupta [8] suggested a switching frequency derivation for the cascaded multilevel inverter operating in current control mode using multiband hysteresis modulation. Choi et al [9] discussed diagnosis and tolerant strategy of an open-switch fault for T-type three-level inverter systems. Nuntawat Thitichaiworakorn et al [10] made a experimental verification of a modular multilevel cascade inverter based on double-star bridge cells. Till Boller et al [11] proposed a neutral-point potential balancing using synchronous optimal pulsewidth modulation of multilevel inverters in medium-voltage high-power AC drives. Makoto Hagiwara and Hirofumi Akagi [12] made experimentation and simulation of a modular push–pull PWM converter for a battery energy storage system. Chang Wu and Chou [13] developed a solar power generation system with a seven-level inverter. Gupta and Jain [14] proposed a novel multilevel inverter based on switched DC sources. Espinosa et al [15] developed a new modulation method for a 13-level asymmetric inverter toward minimum THD. Makineni and Bhaskar [16] made a simulation on cascaded H-bridge multilevel inverter based DSTATCOM. Murali et al [17] also made a design and analysis on voltage source inverter for renewable energy applications. Babaei et al [18] introduced a single phase cascaded multi level inverter based on a new basic unit with reduced number of power switches. Grandi et al [19] analyzed and compared peak to peak ripple in a two level and multilevel PWM inverters. Ruderman in [20] discussed about voltage THD for single and three phase multilevel inverters. Bailu xiao [21] proposed a modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid connected applications. Jamaludin et al [22] proposed a multilevel voltage source inverter with optimized usage of bidirectional switches.

2. Cascaded Multilevel Inverter

The main feature of a cascaded MLI (CMLI) is its ability to reduce the voltage stress on each power device due to the utilization of multiple DC sources. Though there are several types of MLI, the configuration of Modular Structured Multilevel Inverter (MSMI) also called cascaded type is unique when compared to other types of multilevel inverter in the sense that it consists of several modules that require Separate DC Sources (SDCS). The function of this MLI is to synthesize a desired voltage from SDCS which may be batteries, fuel cells or solar cells. The number of modules (M) which is equal to the number of DC sources required depends on the number of levels (m) in the output of the MSMI. M and m are related by m=2M+1. For output voltage consisting of five levels, which are $+2V_{dc}$, $+V_{dc}$, 0,$-V_{dc}$ and $-2V_{dc}$, the number of modules required in the MSMI is two. Compared to other types of MLI, the MSMI requires less number of components with no extra clamping diodes or voltage balancing capacitors that only further complicate the overall inverter operation. Each module of MSMI has the same structure whereby it is represented by a single phase full bridge inverter. This simple modular structure not only allows practically unlimited number of levels for the MSMI by stacking up the modules but also facilitates its packaging. Figure 1 shows the three phase five level cascaded inverter.

The cascaded MLI can be used as compensator in power systems because it does not present unbalance problem in DC source. The structure of separate DC sources is well suited for various renewable energy sources such as fuel cell, photo voltaic cell and biomass cell. Table 1 displays switch states and voltage levels of five level cascaded inverter for R-phase. Figure 2 shows cyclic switching sequence for MSMI.

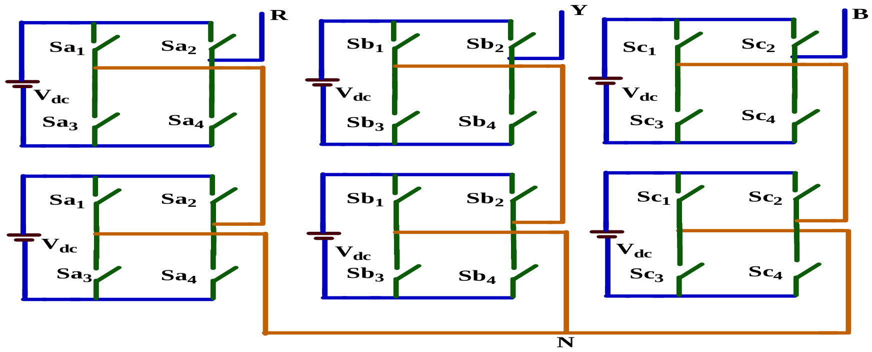

Figure 1. Three phase five level cascaded inverter

Table 1. Switch states and voltage levels of five level cascaded inverter for R-phase

S_{11}	S_{21}	S_{12}	S_{22}	Output (V_o)
1	0	1	0	$+2V_{dc}$
1	0	0	0	$+V_{dc}$
1	0	1	1	$+V_{dc}$
0	0	1	0	$+V_{dc}$
1	1	1	0	$+V_{dc}$
0	0	0	0	0
1	1	1	1	0
1	0	0	1	0
0	1	1	0	0
0	0	1	1	0
1	1	0	0	0
0	1	1	1	$-V_{dc}$
0	1	0	0	$-V_{dc}$
1	1	0	1	$-V_{dc}$
0	0	0	1	$-V_{dc}$
0	1	0	1	$-2V_{dc}$

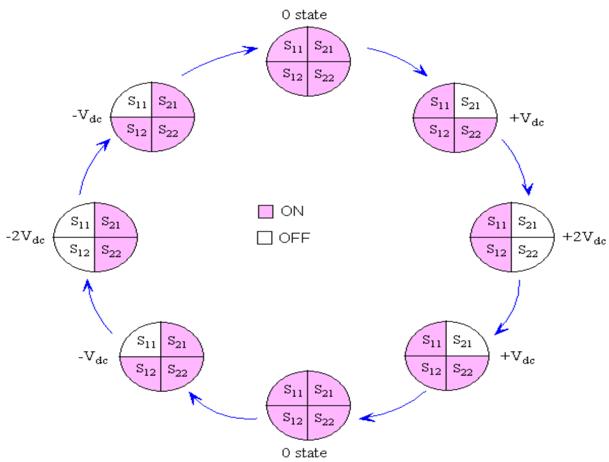

Figure 2. Cyclic switching sequence of chosen MSMI

3. Modulation Strategies

This paper presents the comparison of results of hybrid carrier PWM techniques for the chosen three phase CMLI. In general for a five level inverter four carriers are needed for symmetrical five level inverter. The proposed work focuses on the hybrid carrier technique. The upper two carriers operate at different PWM strategies compared to the lower two carriers. PD, APOD, CO, VF and PS multi-carrier PWM strategies are chosen in this work and the proposed carrier arrangement uses combination of any two strategies among the five. As far as the particular reference wave is concerned, there is also multiple CFD (Control Freedom Degree) including frequency, amplitude, phase angle of the reference wave.

The chosen CMLI is controlled with (APOD + CO), (APOD + PS), (APOD + VF), (CO + VF), (CO + PS), (PD + VF), (PS + PD), (PS + VF), (APOD + PD) and (CO + PD) hybrid PWM with triangular carrier and sine, THI, 60 degree and stepped wave references and the variation of %THD and V_{RMS}(fundamental) of the output voltage are observed for various modulation indices m_a.

3.1. Carrier Arrangement for Various References

The following strategies are employed in this paper.

3.1.1. (APOD + CO) Hybrid PWM Strategy

This strategy requires each of the two carrier waves in the upper half side to be phase displaced from each other by 180 degrees alternately. The vertical offset of carriers for chosen inverter can be illustrated in Figure 3 to 6. It can be seen that the two carriers in the lower half side overlap with each other and the reference sine wave is placed at the middle of the four carriers.

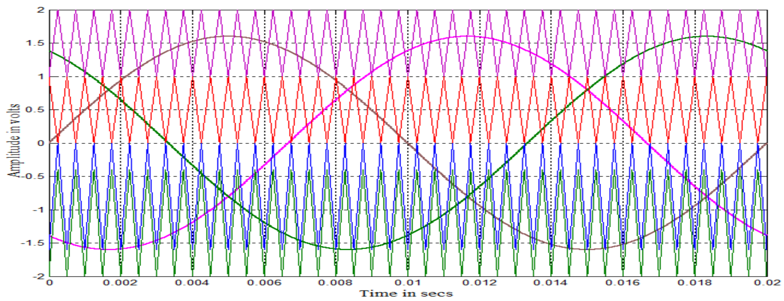

Figure 3. Sample Carrier arrangement for (APOD + CO) hybrid PWM strategy (m_a = 0.8, m_f = 40) with sine reference

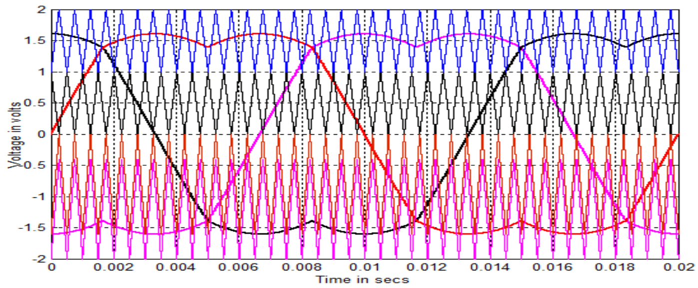

Figure 4. Sample Carrier arrangement for (APOD + CO) hybrid PWM strategy (m_a = 0.8, m_f = 40) with THIPWM reference

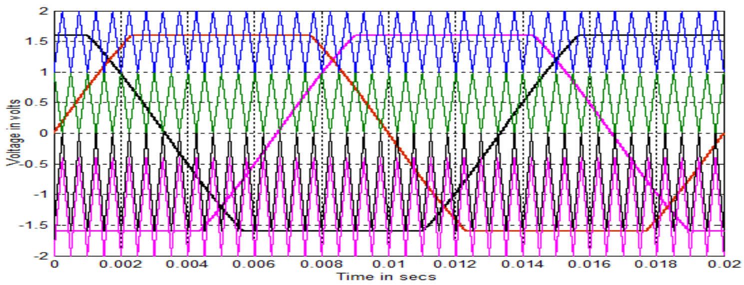

Figure. 5 Sample Carrier arrangement for (APOD + CO) hybrid PWM strategy (m_a = 0.8, m_f = 40) with 60 degree reference

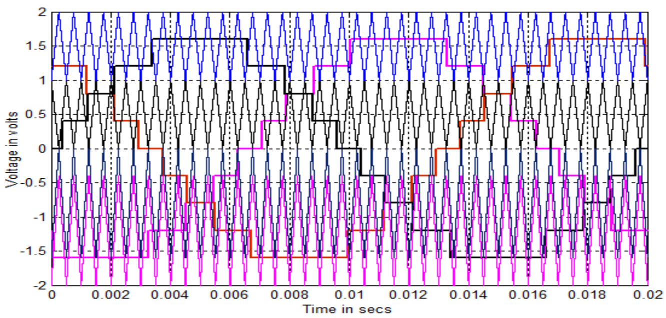

Figure 6. Sample Carrier arrangement for (APOD + CO) hybrid PWM strategy (m_a = 0.8, m_f = 40) with stepped wave reference

4. Simulation Results

Simulation is performed using MATLAB-SIMULINK. It is observed that (PS+APOD) PWM with sinusoidal reference, (PS+VF) PWM with THI reference, (PD+VF) PWM with 60 degree reference and (APOD+PS) PWM with stepped wave reference provide output with relatively low distortion. It is also seen that (CO+VF) PWM strategy with sine reference, (APOD+CO) and (CO+PS) PWM with third harmonic injection, (CO+PD) PWM with 60 degree PWM reference and (APOD+CO) PWM with stepped wave reference are found to perform better since they provide relatively higher fundamental RMS output voltage.

The chosen three topologies of five level inverter are simulated using SIMULINK - power system block set. Simulations are performed for different values of m_a ranging from 0.6 to 1 and resistive load of 100Ω. Simulated output voltage of chosen MLI with (APOD+CO) PWM strategy is displayed only for a sample value of m_a=0.8. m_f is chosen as 40 as a trade off in view of the following reasons: (i) to reduce switching losses (which may be high at large m_f) (ii) to reduce the size of the filter needed for the closed loop control, the filter size being moderate at moderate frequencies (iii) to effectively utilize the available dSPACE system for hardware implementation. The corresponding %THD and RMS values of output voltage is measured using FFT (Fast Fourier Transform) block of SIMULINK and tabulated.

Table 2 and Figure 20 show the comparison of %THD of output voltage (by simulation) with different hybrid bipolar PWM switching strategies for various modulation indices and sinusoidal reference. Table 3 shows the comparison of %THD of output voltage with different hybrid bipolar PWM switching strategies for various modulation indices and third harmonic injection reference. Table 4 show the comparison of %THD of output voltage with different hybrid bipolar PWM switching strategies for various modulation indices and 60 degree PWM reference. Table 5 shows the comparison of %THD of output voltage with different hybrid bipolar PWM switching strategies for various modulation indices and stepped wave reference.

Variations of RMS value of fundamental output voltage for various modulation indices (0.6-1) are listed in Table 3 (Figure 21), 5, 7 and 9 respectively for sine, THI, 60 degree and stepped wave references. Figure 7, 9, 11 and 13 show the output voltages of cascaded MLI with (APOD+CO) hybrid PWM with sine, THI, 60 degree and stepped wave references respectively and Figure 8, 10, 12 and 14 show corresponding FFT plot for m_a = 0.8. From simulated FFT plot it is seen that dominant harmonics are present in (APOD+CO) as follows:

(i) 2^{nd}, 3^{rd}, 35^{th} to 40^{th} with sine reference
(ii) 2^{nd}, 3^{rd}, 9^{th}, 31^{st}, 33^{rd} to 40^{th} with THI PWM reference
(iii) 2^{nd}, 3^{rd}, 5^{th}, 7^{th}, 33^{rd} to 38^{th} , 40^{th} with 60 degree reference
(iv) 2^{nd}, 3^{rd}, 15^{th}, 21^{st}, 23^{rd}, 35^{th} to 40^{th} with stepped wave reference.

The following parameter values are used for simulation: V_{dc} = 100V and R (load) = 100 ohms, f_c = 2000Hz and f_m = 50 Hz.

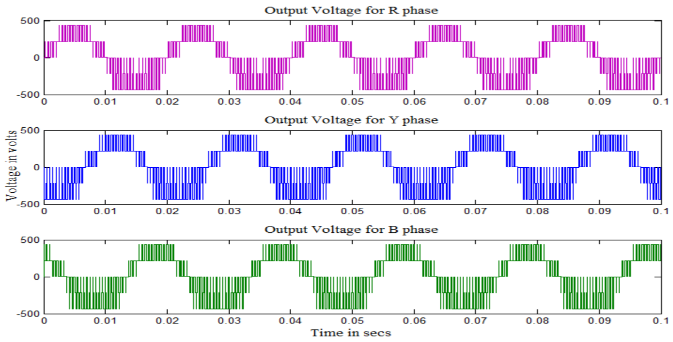

Figure 7. Output voltage of cascaded MLI with (APOD+CO) PWM strategy (sine ref.)

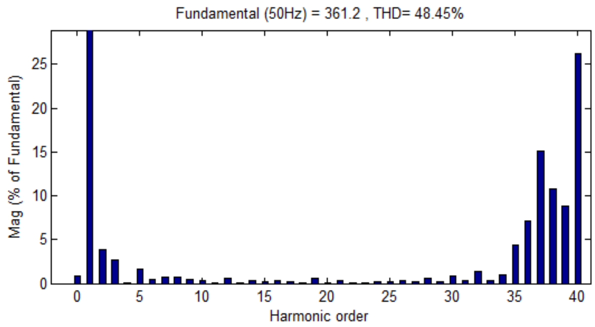

Figure 8. FFT plot of cascaded MLI with (APOD+CO) PWM strategy for R-phase (sine ref.)

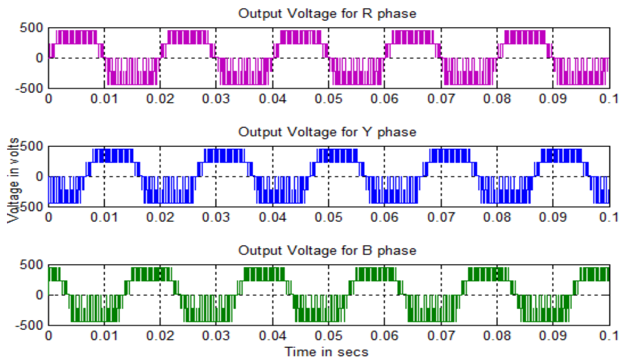

Figure 9. Output voltage of cascaded MLI with (APOD+CO) PWM strategy (THI ref.)

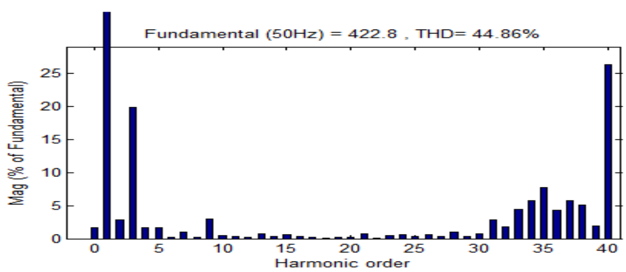

Figure 10. FFT plot of cascaded MLI with (APOD+CO) PWM strategy for R-phase (THI ref.)

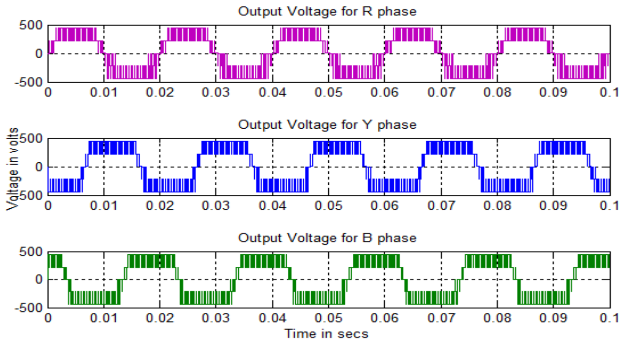

Figure 11. Output voltage of cascaded MLI with (APOD+CO) PWM strategy(60 degree PWM ref.)

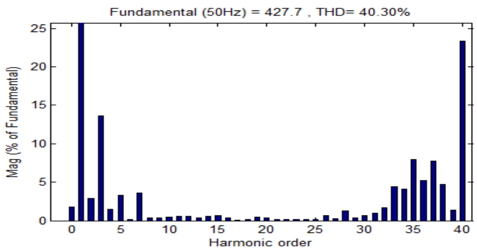

Figure 12. FFT plot of cascaded MLI with (APOD+CO) PWM strategy for R-phase (60 degree PWM ref.)

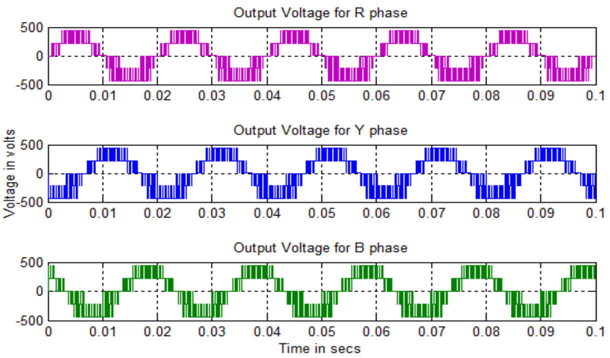

Figure 13. Output voltage of cascaded MLI with (APOD+CO) PWM strategy (stepped wave ref.)

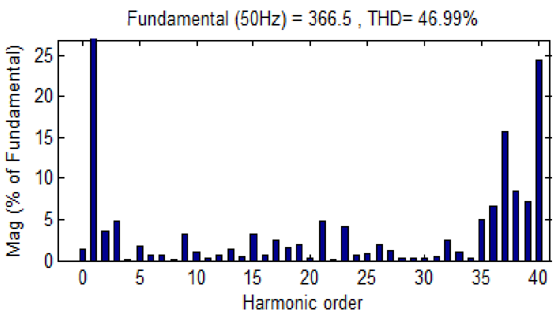

Figure 14. FFT plot of cascaded MLI with (APOD+CO) PWM strategy for R-phase (stepped wave ref.)

Table 2. % THD of output voltage (R-phase) of cascaded MLI for various values of m_a with sine ref (By simulation)

m_a	APOD+CO	APOD+PD	APOD+PS	APOD+VF	CO+PD	CO+PS	CO+VF	PD+VF	PS+PD	PS+VF
1	33.47	27.36	27.15	27.32	33.49	33.32	33.46	27.01	26.9	26.91
0.9	40.52	33.89	33.67	33.25	40.46	40.3	40.35	33.48	33.52	33.38
0.8	48.45	38.62	38.41	38.56	48.22	48.08	48.15	38.31	38.41	38.35
0.7	59.04	42.21	42.13	42.44	58.53	58.55	58.75	42.30	42.19	42.42
0.6	69.27	44.42	44.44	44.57	68.91	68.91	69.01	44.63	44.45	44.61

Table 3. V_{RMS} (fundamental) of output voltage (R-phase) of cascaded MLI for various values of m_a with sine ref (By simulation)

m_a	APOD+CO	APOD+PD	APOD+PS	APOD+VF	CO+PD	CO+PS	CO+VF	PD+VF	PS+PD	PS+VF
1	315	310.6	310.8	310.5	314.6	314.8	314.5	310.7	310.9	310.9
0.9	286.4	276.8	279.6	279.8	286.8	286.6	286.8	280	279.8	279.9
0.8	255.4	248.5	248.2	248.7	255.4	255.1	255.6	249	248.1	248.3
0.7	219.2	217.5	217	217.1	220	219.5	219.6	216.9	217.1	216.7
0.6	185	186.4	186.5	186.4	186	186.1	186	186.1	186.6	186.6

Table 4. %THD of output voltage (R-phase) of cascaded MLI for various values of m_a with THIPWM ref (By simulation)

m_a	APOD+CO	APOD+PD	APOD+PS	APOD+VF	CO+PD	CO+PS	CO+VF	PD+VF	PS+PD	PS+VF
1	31.07	29.08	28.87	29.06	31.26	31.08	31.24	28.88	28.96	26.95
0.9	37.31	36.07	35.64	36.04	37.39	33.99	37.36	35.88	36.01	35.98
0.8	44.86	41.46	41.35	41.42	44.35	36.99	44.32	41.17	41.27	41.24
0.7	55.25	44.28	44.10	44.14	55.19	55.04	55.07	43.91	43.98	43.84
0.6	64.81	43.10	42.61	43.07	64.8	64.60	64.78	42.85	42.85	42.82

Table 5. V_{RMS} (fundamental) of output voltage (R-phase) of cascaded MLI for various values of m_a with THIPWM ref (By simulation)

m_a	APOD+CO	APOD+PD	APOD+PS	APOD+VF	CO+PD	CO+PS	CO+VF	PD+VF	PS+PD	PS+VF
1	363.5	360.1	359.6	360	362.8	362.4	362.8	359.8	359.4	359.2
0.9	333	324.5	324.6	324.4	332.7	340.7	332.6	324.3	324.3	324.2
0.8	299	288.2	288.5	288.4	299	332.7	299.1	288.4	287.9	288
0.7	259.3	252.6	252.7	252.8	258.6	258.7	258.8	252.7	257.4	252.9
0.6	218.1	216.3	215.8	216.4	218.8	218.2	218.9	216.4	216	216.1

Table 6. %THD of output voltage (R-phase) of cascaded MLI for various values of m_a with 60 degree ref (By simulation)

m_a	APOD+CO	APOD+PD	APOD+PS	APOD+VF	CO+PD	CO+PS	CO+VF	PD+VF	PS+PD	PS+VF
1	26.98	22.92	30	25.46	34.87	26.47	26.62	22.68	29.88	25.37
0.9	34.49	31.70	37.84	33.61	41.03	34.09	34.04	31.23	37.42	33.67
0.8	40.30	37.77	43.49	40.04	45.40	39.83	39.85	37.59	43.39	39.88
0.7	52.49	41.98	46.80	43.81	56.80	52.21	52.36	41.78	47.13	43.63
0.6	62.79	42.94	46.70	43.88	66.58	62.57	62.70	42.46	46.91	43.95

Table 7. V_{RMS} (fundamental) of output voltage (R-phase) of cascaded MLI for various values of m_a with 60 degree ref (By simulation)

m_a	APOD+CO	APOD+PD	APOD+PS	APOD+VF	CO+PD	CO+PS	CO+VF	PD+VF	PS+PD	PS+VF
1	365.2	364.3	384.1	374.6	389.1	365.7	365.6	364.2	384.1	374.8
0.9	323.5	327.6	345.9	337.4	355.5	333.5	333.3	327.9	342.6	337.3
0.8	302.4	291.5	307.5	299.8	323.9	303	302.9	291.5	307.6	300
0.7	260.3	255.1	269	262.3	279.1	260.9	261.2	255.3	269.3	262.4
0.6	220.6	218.6	230.6	224.7	236.7	220.9	220.9	218.7	230.7	224.8

Table 8. %THD of output voltage (R-phase) of cascaded MLI for various values of m_a with stepped wave ref (By simulation)

m_a	APOD+CO	APOD+PD	APOD+PS	APOD+VF	CO+PD	CO+PS	CO+VF	PD+VF	PS+PD	PS+VF
1	31.92	23.86	24.35	23.98	31.56	32.05	31.65	24.49	23.96	24.10
0.9	39.60	32.95	32.77	33.12	39.91	39.84	40.04	33.36	33.01	33.18
0.8	46.99	39.02	38.83	38.90	48.15	47.95	48.03	38.83	39.29	39.18
0.7	58.07	42.02	42.30	41.57	58.73	58.73	58.28	41.20	42.36	41.92
0.6	68.80	45.95	46.04	46.49	69.26	69.18	69.62	46.83	45.71	46.26

Table 9. V_{RMS} (fundamental) of output voltage (R-phase) of cascaded MLI for various values of m_a with stepped wave ref (By simulation)

m_a	APOD+CO	APOD+PD	APOD+PS	APOD+VF	CO+PD	CO+PS	CO+VF	PD+VF	PS+PD	PS+VF
1	315.9	314.7	312.1	314.9	320.5	317.9	320.7	315.5	317	317.2
0.9	287	282	280.7	282.3	287.6	286.3	286	283.1	283.3	283.6
0.8	259.2	250.3	251	250.9	255.8	256.5	256.3	252.2	250.6	251.2
0.7	224.5	219.9	221.4	220.9	220	221.5	221	222.6	219.4	220.3
0.6	189.3	188.6	189.2	188.6	186.7	187.3	186.7	189.6	187.8	187.8

4. Experimental Results

This section presents the results of experimental work (Figure15) carried out on chosen CMLI using dSPACE DS1103 controller board. The results of the experimental study are shown in the form of the oscillograms of PWM outputs and corresponding harmonic spectrum of chosen MLI. Experiments are performed with appropriate m_f (same as in simulation studies) and for different values of m_a. The corresponding %THD and V_{RMS} (fundamental) output voltages are calculated (from the FFT spectrum obtained), tabulated and analyzed. The experimental output voltages and the corresponding harmonic spectra are shown for only one sample value of m_a=0.8 of cascaded five level inverter topology.

Figure 16-19 show the sample experimental output voltages and FFT of chosen CMLI obtained using dSPACE/RTI for (APOD + CO) hybrid PWM with sine, THI, 60 degree and stepped wave references respectively. After suitably scaling down the simulation values, in view of laboratory constraints, the peak-to-peak output voltage obtained experimentally is 40V. Variations of RMS value of fundamental output voltage of cascaded MLI using triangular carriers for various modulation indices and for different hybrid PWM strategies with various references are shown in Table 11, 13, 15 and 17 respectively. Table 10, 12, 14 and 16 show the experimental %THD for hybrid PWM strategies. The following parameter values are used for experimentation: V_{dc}=20V, R(load)=100Ω, f_c=2000 Hz and f_m=50Hz, m_f=40 for bipolar (APOD + CO) PWM, (APOD + PS) PWM, (APOD + VF) PWM, (CO + VF) PWM, (CO + PS) PWM, (PD + VF) PWM, (PS + PD) PWM, (PS + VF) PWM, (APOD + PD) PWM and (CO + PD) PWM strategies with triangular carriers and various references.

Figure 15. Hardware setup of three phase five level cascaded inverter

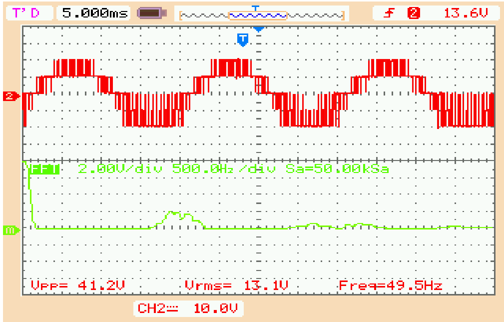

Figure 16. Output voltage and FFT plot of cascaded MLI with (APOD+CO) PWM strategy for R-phase (sine ref.)

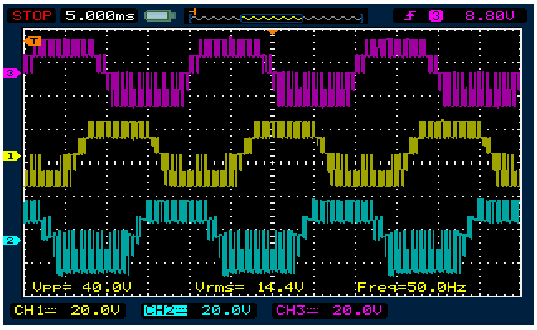

Figure 17. Output voltage of cascaded MLI with (APOD+CO) PWM strategy (THI ref.)

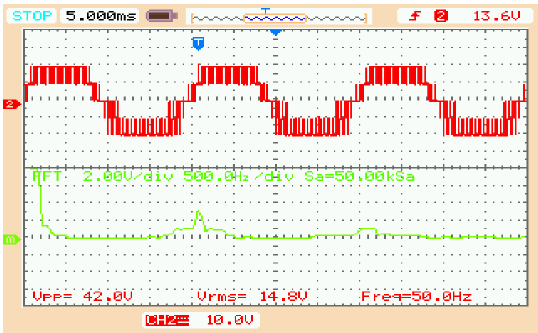

Figure 18. Output voltage and FFT plot of cascaded MLI with (APOD+CO) PWM strategy for R-phase (60 degree ref.)

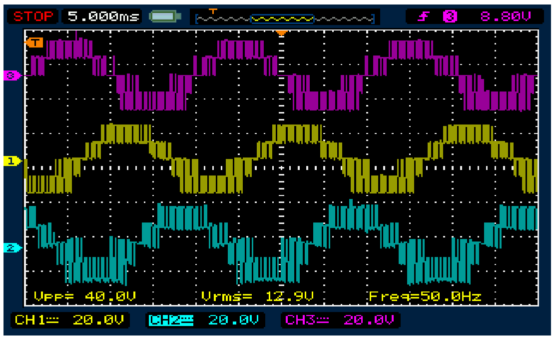

Figure 19. Output voltage of cascaded MLI with (APOD+CO) PWM strategy (stepped wave ref.)

Table 10. % THD of output voltage (R-phase) of cascaded MLI for various values of m_a with sine ref (By experimentation)

m_a	APOD +CO	APOD+P D	APOD+P S	APOD+V F	CO+P D	CO+P S	CO+V F	PD+V F	PS+P D	PS+V F
1	22.93	22.41	8.77	15.03	10.20	19.92	13.46	3.636	1.739	0.7462
0.9	26.89	25.05	12.13	17.24	13.51	20.40	14.38	3.703	1.904	0.8695
0.8	34.35	33.08	21.12	18.63	15.15	20.45	18.45	6.097	3.38	4.854
0.7	35.7	36.58	22.38	20.37	18.90	22.72	18.51	6.84	4.895	5.281
0.6	36.9	38.28	26.42	22.58	23.21	25	19.06	7.425	9.523	7.936

Table 11. V_{RMS} (fundamental) of output voltage (R-phase) of cascaded MLI for various values of m_a with sine ref (By experimentation)

m_a	APOD +CO	APOD+P D	APOD+P S	APOD+V F	CO+P D	CO+P S	CO+V F	PD+V F	PS+P D	PS+V F
1	14.9	14.5	14.2	14.5	14.7	14.7	14.9	14.6	14.3	14.2
0.9	14	13.6	13.4	13.5	14	13.8	13.9	13.5	13.3	13.4
0.8	13.1	12.3	12.3	12.4	13.2	13.2	13	12.3	12.6	12.6
0.7	11.9	11.1	11.4	11	11.9	12	11.8	11	11.5	11.5
0.6	10.9	9.98	10.3	9.98	11.1	11	10.8	10.1	10.5	10.3

Table 12. %THD of output voltage (R-phase) of cascaded MLI for various values of m_a with THIPWM ref (By experimentation)

m_a	APOD +CO	APOD+P D	APOD+P S	APOD+V F	CO+P D	CO+P S	CO+V F	PD+V F	PS+P D	PS+V F
1	13.42	5.063	3.70	7.27	2.95	1.87	9.493	2.597	3.2	1.6
0.9	17.75	7.272	10.59	11.26	6.329	5.434	11.97	5.128	6.172	1.851
0.8	20.56	12.5	11.34	11.90	6.66	9.740	13.42	9.036	8.053	2.255
0.7	21.54	13.98	12.5	12.93	16.26	12.04	22.05	9.090	8.955	6.666
0.6	22.55	21.55	13.07	12.98	18.79	19.84	24.59	9.375	9.090	9.219

Table 13. V_{RMS} (fundamental) of output voltage (R-phase) of cascaded MLI for various values of m_a with THIPWM ref (By experimentation)

m_a	APOD +CO	APOD+P D	APOD+P S	APOD+V F	CO+P D	CO+P S	CO+V F	PD+V F	PS+P D	PS+V F
1	16.9	16.5	16.2	16.5	16.9	16.6	16.7	16.6	16.2	16.2
0.9	15.8	15.4	15.1	15.4	15.8	15.4	15.8	15.4	14.9	15
0.8	14.4	13.9	14.1	14.0	14.8	14.5	14.8	14.1	14.1	14.1
0.7	13.3	12.8	13	12.6	13.3	13.8	13.6	12.8	13.4	13.3
0.6	12.3	11.6	12	11.6	12.3	12.6	12.2	11.7	12.5	12.5

Table 14. %THD of output voltage (R-phase) of cascaded MLI for various values of m_a with 60 degree ref (By experimentation)

m_a	APOD +CO	APOD+P D	APOD+P S	APOD+V F	CO+P D	CO+P S	CO+V F	PD+V F	PS+P D	PS+V F
1	15.97	9.803	2.702	12.04	4.464	17.64	10.48	3.267	4.065	2.479
0.9	22.38	11.97	3.592	12.90	9.58	19.86	17.85	4.464	5.343	3.03
0.8	22.43	12.06	13.46	14.95	10.89	20.68	19.23	4.724	6.097	3.03
0.7	23.64	17.71	14.18	17.32	19.40	21.89	25.92	4.895	8.00	8.053
0.6	36	19.36	16.66	18.88	20.32	34.88	29.41	6.034	8.57	17.14

Table 15. V_{RMS} (fundamental) of output voltage (R-phase) of cascaded MLI for various values of m_a with 60 degree ref (By experimentation)

m_a	APOD +CO	APOD+P D	APOD+P S	APOD+V F	CO+P D	CO+P S	CO+V F	PD+V F	PS+P D	PS+V F
1	16.9	16.7	16.7	16.6	16.8	17	16.8	16.8	16.4	16.5
0.9	15.6	15.3	15.3	15.5	15.6	15.1	15.6	15.3	15	14.9
0.8	14.8	14.2	14.2	14.3	14.6	14.5	14.3	14.3	14	14
0.7	13.4	12.7	12.7	12.7	13.4	13.7	13.5	12.7	13.1	13.2
0.6	12.5	11.6	11.6	11.7	12.3	12.9	11.9	11.6	12.3	12.1

Table 16 %THD of output voltage (R-phase) of cascaded MLI for various values of m_a with stepped wave ref (By experimentation)

m_a	APOD +CO	APOD+P D	APOD+P S	APOD+V F	CO+P D	CO+P S	CO+V F	PD+V F	PS+P D	PS+V F
1	27.64	20.54	3.921	13.69	12.5	24.83	19.35	6.060	5.882	1.8
0.9	28.18	26.20	4.8	17.39	17.26	26.78	25.36	6.896	6.349	3.053
0.8	31.19	26.71	19.23	19.08	19.60	28.22	26.92	8.072	7.575	3.968
0.7	34.35	35.08	20.68	24	20.31	30.76	33.33	14.28	7.920	9.523
0.6	35.97	44.98	25.86	24.31	23.85	32.37	33.61	16.89	17.36	12.60

Table 17. V_{RMS} (fundamental) of output voltage (R-phase) of cascaded MLI for various values of m_a with stepped wave ref (By experimentation)

m_a	APOD +CO	APOD+P D	APOD+P S	APOD+V F	CO+P D	CO+P S	CO+V F	PD+V F	PS+P D	PS+V F
1	14.9	14.6	14.5	14.6	15.3	15.1	15.5	14.8	14.4	14.7
0.9	13.9	13.1	13	13.1	13.9	13.9	13.8	13.2	13.2	13.1
0.8	12.9	12.4	12.5	12.4	12.9	13	12.9	12.4	13.9	12.5
0.7	12.3	11.4	11.6	11.5	12	12.4	11.9	11.6	11.9	11.9
0.6	10.9	9.78	10.2	9.87	10.9	11.2	10.5	9.91	10.1	10

4. Conclusion

Ten chosen hybrid PWM strategies have been developed and tested for different modulation indices ranging from 0.6 -1 for three phase MLI. Various performance indices like (i) % THD and harmonic spectra indicating purity of the output voltage, (ii) CF (Crest Factror) which is a measure of the stress on the device, (iii) LOH (Lower Order Harmonics) suggesting indirectly the size and cost of the filter and, (iv) V_{RMS} (fundamental) indicating the amount of DC bus utilization have been evaluated, presented and analyzed. Compared to the SPWM (Sinusoidal Pulse Width Modulation) technique the advanced PWM techniques such as THI, 60 degree PWM and stepped wave references gives higher fundamental RMS voltage. By using DSPACE it is easy to generate the pulse for the switches. Both model and program oriented simulation files can be interfaced easily. Appropriate PWM strategies may be employed depending on the performance measure required in a particular application of the MLI taken up for study in this work.

References

[1] Lee K, Nojima G. Quantitative Power Quality and Characteristic Analysis of Multilevel Pulse Width Modulation Methods for Three Level Neutral Point Clamped Medium Voltage Industrial Drives. *IEEE Transactions on Industry Apllications*. 2012; 48(4): 1364-1373.

[2] Gupta KK, Jain S. Topology for Multilevel Inverters to Attain Maximum Number of Levels from Given DC Sources. *IET Power Electron*. 2012; 5(4): 435-446.

[3] Najafi E, Yatim AHM. Design and Implementation of a New Multilevel Inverter Topology. *IEEE Transactions on Industrial Electronics*. 2012; 59(1): 4148-4154.

[4] P Roshankumar P, Rajeevan P, Mathew K, Gopakumar K, Leon JI, Franquelo LG. A Five-Level Inverter Topology with Single DC Supply by Cascading a Flying Capacitor Inverter and an H-Bridge. *IEEE Transactions on Power Electronics*. 2012; 27(8): 3505-3515.

[5] Wu TF, Chang CH, Lin LC, Chang YC, Chang YR. Two Modulated Digital Control for Three Phase Bidirectional Inverter with Wide Inductance Variation. *IEEE Transactions on Power Electronics*. 2013; 28(4): 1598-1607.

[6] José Antonio Juárez-Abad, Jesús Linares-Flores, Enrique Guzmán-Ramírez. Generalized Proportional Integral Tracking Controller for a Single-Phase Multilevel Cascade Inverter: An FPGA Implementation. *IEEE Trans. Ind. Inform*. 2014; 10(1): 256-266.

[7] Younghoon Cho, Thomas LaBella, Jih-Sheng Lai, Matthew K Senesky. A Carrier-Based Neutral Voltage Modulation Strategy for Multilevel Cascaded Inverters Under Unbalanced DC Sources. *IEEE Trans. Ind. Electron*. 2014; 61(2): 625-636.

[8] Shweta Gautam, Rajesh Gupta. Switching Frequency Derivation for the Cascaded Multilevel Inverter Operating in Current Control Mode Using Multiband Hysteresis Modulation. *IEEE Trans. Power Electron.* 2014; 29(3): 1480-1489.

[9] Ui-Min Choi, Kyo-Beum Lee, Frede Blaabjerg. Diagnosis and Tolerant Strategy of an Open-Switch Fault for T-Type Three-Level Inverter Systems. *IEEE Trans. Ind. Appl.* 2014; 50(1): 495-508.

[10] Nuntawat Thitichaiworakorn, Makoto Hagiwara, Hirofumi Akagi. Experimental Verification of a Modular Multilevel Cascade Inverter Based on Double-Star Bridge Cells. *IEEE Trans. Ind. Appl*. 2014; 50(1): 509-519.

[11] Till Boller, Joachim Holtz, Akshay K Rathore. Neutral-Point Potential Balancing Using Synchronous Optimal Pulsewidth Modulation of Multilevel Inverters in Medium-Voltage High-Power AC Drives. *IEEE Trans. Ind. Appl*. 2014; 50(1): 549-557.

[12] Makoto Hagiwara, Hirofumi Akagi. Experiment and Simulation of a Modular Push–Pull PWM Converter for a Battery Energy Storage System. *IEEE Trans. Ind. Appl*. 2014; 50(2): 1131-1140.

[13] Jinn-Chang Wu, Chia-Wei Chou. A Solar Power Generation System With a Seven-Level Inverter. *IEEE Trans. Power Electron.* 2014; 29(7): 3454-3462.

[14] Krishna Kumar Gupta, Shailendra Jain. A Novel Multilevel Inverter Based on Switched DC Sources. *IEEE Trans. Ind. Electron*. 2014; 61(7): 3269-3278.

[15] Eduardo E Espinosa, Jose R Espinoza, Pedro E Melín, Roberto O Ramírez, Felipe Villarroel, Javier A Muñoz, Luis Morán. A New Modulation Method for a 13-Level Asymmetric Inverter Toward Minimum THD. *IEEE Trans. Ind. Appl.* 2014; 50(3): 1924-1933.

[16] Rammohan Rao Makineni, CN Bhaskar. Simulation of cascaded H-bridge Multilevel Inverter based DSTATCOM. *Telkomnika Indonesian Journal of Electrical Engineering*. 2014; 12(8): 5720-5728.

[17] M Murali, A Arulmozhiyal, P Sundaramoorthy. A Design and Analusis of voltage source inverter for renewable energy applications. *Telkomnika Indonesian Journal of Electrical Engineering*. 2014; 12(12): 8114-8119

[18] E Babaei, S Laali, Z Bayat. A Single-Phase Cascaded Multilevel Inverter Based on a New Basic Unit With Reduced Number of Power Switches. *IEEE Trans. Power Electron.* 2015; 62(3): 922-929.

[19] G Grandi, J Lon carski, O Dordevic. Analysis and comparison of peak to peak current ripple in two level and multilevel PWM inveters. *IEEE Tran. on Industrial Electronics.* 2015; 62(5): 2721-2730.

[20] A Ruderman. About voltage total harmonic injection for single and three phase multilevel inverters. *IEEE trans, on Industrial Electronics.* 2015; 62(3): 1548-1551.

[21] Bailu xiao, Lijun hang, Jun mei, C Riley. Modular cascaded H-bridge multilevel PV inverter with distributed MPPT for grid connected applications. *IEEE trans, on Industrial Applications.* 2015; 51(2): 1722-1731.

[22] J Jamaludin, N Abd rahim. Hew wooiping, multilevel voltage source inverter with optimized usage of bidirectional switches. *IET Power Electronics.* 2015; 8(3): 378-390.

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