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# An Approach of PFC in BLDC Motor Drives Using BLSEPIC Converter

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***Abstract***

*This paper presents the analysis and design of on front end bridgeless single-ended primary-inductance converter (BLSEPIC) based power factor rectification, with output voltage regulation and high frequency isolation working in discontinuous conduction mode. The switching loss in VSI is minimized by an electronic commutation of Brushless DC motor (BLDCM) is used to operate in a low-frequency operation. To improve the efficiency, the diode bridge rectifier is replaced with the alternate bridgeless topologies which offers less conduction losses, advised by the international power quality standards, a wide range of speed control is obtained with improved power quality BLDC motor drive is proposed and simulated in MATLAB/SIMULINK.*

***Keywords:*** *BLDC motor, DCM, power factor correction, bridgeless SEPIC, power-quality*



## 1. Introduction

A Brushless DC motor (BLDCM) possesses many advantages such as high efficiency, silent operation, varied speed range and low maintenance requirements. It is a kind of three phase synchronous motor with permanent magnets on the rotor and trapezoidal back EMF is obtained [1-4]. It requires a three-phase voltage source inverter (VSI) to be operated as an electronic commutator based on the rotor position signals of the BLDC obtained using Hall Effect Sensors. The three-phase VSI of the BLDC drive is fed from single-phase AC mains through a diode bridge rectifier followed by a smoothening DC capacitor, which draws an uncontrolled charging current for the DC capacitor resulting in a pulsed current. So, many power quality problems arise such as poor power factor, high Total Harmonic Distortion (THD) of AC mains current and its high crest factor. Moreover, there are many international PQ standards such as IEC 61000, IEEE 519 etc [5]. Which emphasize on low harmonic contents and near unity PF current to be drawn from AC mains by various loads.

Therefore, an improved power quality converter based drive is almost essential for the BLDC [6]. There has been some efforts for use of power factor correction(PFC) converters for the power quality enhancement, however it uses, a two-stage PFC drives which consist of a boost converter for PFC at front-end followed by another DC – DC converter in second stage for voltage regulation. At second stage usually a fly back or a forward converter has been used for low power application and a full-bridge converter for higher power applications [7]. A Single Ended Primary Inductor Converter (SEPIC), as a single stage PFC converter, is proposed for Power Factor Correction in a BLDC motor [16].

## 2. Proposed Control Scheme for bridgless PFC Converter

Bridgeless PFC topologies are currently gaining interests generally, due to the difficulty of implementation and control of bridgeless PFC converters, but a bridgeless topology can reduce conduction losses from rectifying bridges with overall system efficiency can be increased, with a bridgeless topology has the advantage of THD decreasing from input diode reduction. The bridgeless converter circuit shown in Figure 1 is typically popular for bridgeless topologies, in which the converter operates separately over positive and negative cycles. This circuit is simple and easy to implement, therefore there are fewer limitations to choosing the

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main passive components. This circuit can be adapted into a single-switch bridgeless converter, which has low conduction loss and requires fewer components.

### 2.1. Power Stage Specification

The power stage specification of the bridgeless SEPIC PFC converter, as shown in Figure 1, is designed with following power stage specification:

1) Input voltage ( $V_{in}$) :95 ~135 *V RMS* at 60 Hz
2) Output voltage ($V_o$ ) : 50 V
3) Output power ( $P_0$ ) : 150 W
4) Switching frequency ( $F_s$ ) : 100 kHz
5) Power Factor (PF) : > 0.95

### 2.2. Components Selections

The components were selected according to the following rationale.

1) Energy transfer capacitor $C_1$: 0.47$\mu$F
2) The two inductors current ripple steering effect depends on the $C_1$ capacitance
3) Output capacitor Co: 3mF
4) The magnitude of the regulated output voltage ripple is decided by the $C_2$ capacitance.
5) Input inductor $L_1$ & output inductor $L_2$: 600µH
6) The inductor current ripple of is decided by the size of the $L_1$ inductance.

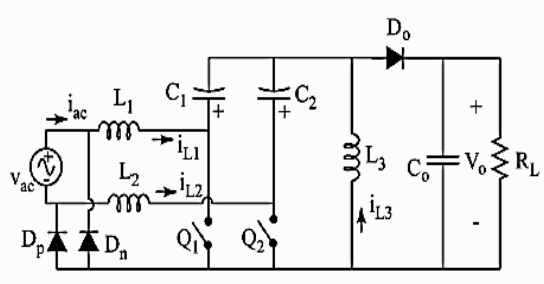


Figure 1. Control scheme of the proposed Bridgeless SEPIC converter

## 3. Modeling of Bridgeless Sepic PFC Converter

### 3.1. Bridgeless SEPIC Converter Model

Single-ended primary-inductor converter (SEPIC) is a type of DC-DC converter allowing the electrical voltage at its output to be greater than, less than, or equal to that at its input; the output of the SEPIC is controlled by the duty cycle of the control transistor. A SEPIC is similar to a traditional buck- boost converter, but has advantages of having non-inverted output. The amount of energy exchanged is controlled by switch.

The single-switch bridgeless SEPIC PFC converter has only one active switch that makes the topology simple, but the modelling is complicated with the two inductors and two capacitors. Figure 2(a) and (b) depict the operations for each cycle of the switch on-time and the switch off-time in the positive half cycle. $L_1$ only conducted during the positive half cycle, and $L_2$ is left uncontrolled. Even though the desired sensing current is the only current through $L_1$, the actual sensing current is the sum of currents flowing into $L_1$ and $L_2$. The current flowing in $L_2$ creates an undesired ripple of the sensed current during positive half line cycle.

Inductances of $L_1$ and $L_2$ should be selected with consideration of these ripples. Alternative difference of this topology is the undesired circulating current from the capacitive coupling loop, as shown in Figure 2(a) and (b). The circulating current causes power loss but does not significantly affects the total efficiency, so, in this it will not be considered. Although the two features mentioned above affect the system performance, thus the effects are not significantly impact the model of the system. Thus, the input and output voltage is considered to be constant voltages due to the exploration of the small-signal linear model which was performed while assuming a quasi-static condition, because the switching frequency is much higher than the line frequency.

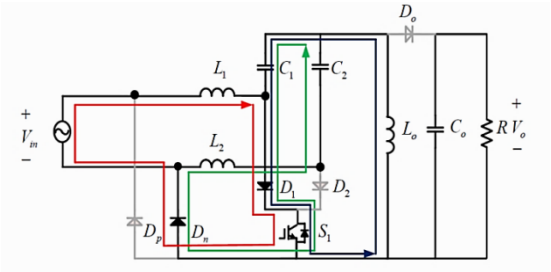


Figure 2(a). Bridgeless SEPIC PFC Converter (switch-on)

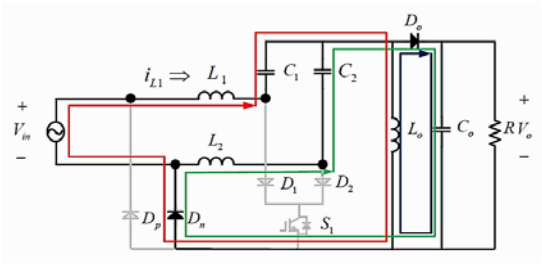


Figure 2(b). Bridgeless SEPIC PFC Converter (switch-off)

### 3.2. Switch on Stage of SEPIC Converter

The Figure 3 shows the on-time diagram for switch $S_1$, for which switch $S_1$ is on, and diode $D_1$ is off. The input side inductor $L_1$ is charged from the input voltage in this stage, the charged $C_1$ transfers energy into the output side inductor Lo, and Lo is charging in this stage. In addition, the load current comes from the charged output capacitor Co. Based on the inductor volt-second balance and the capacitor charge balance is obtained.

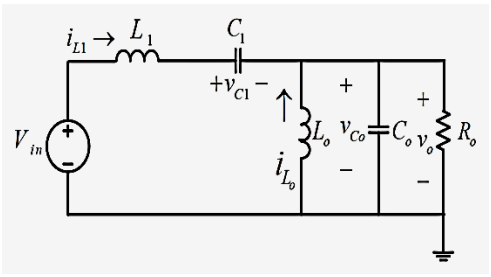


Figure 3. Operation of the SEPIC Converter Switch On-Stage

The voltage across $L_1$ and its input voltage Vin are same.

$$L_1 = \frac{di_{L1}}{dt} = V_{in}$$

The voltage across Lo and the voltage across capacitor, $C_1$.are same.

$$L_0 \frac{di_{L0}}{dt} = v_{c1} (\approx V_{in})$$

The current through $C_1$ and the current through inductor $L_2$ are same.

$$C_1 \frac{dV_{c1}}{dt} = -i_{L0}$$

The current through $C_2$ and the load current is the same.

$$C_0 \frac{dv_{c0}}{dt} = -\frac{v_0}{R} = -\frac{v_{c0}}{R}$$

### 3.3. Switch-Off stage of SEPIC Converter

The Figure 4 shows the off-state diagram for switch S1, in which switch S1 is off and the diode D1 is on. Inductor L1 charges the capacitor C1 and provides the load current. The Inductor L2 is connected and the output capacitor Co get charged which provides the load current are obtained according to the volt-sec balance and the capacitor charge balance.

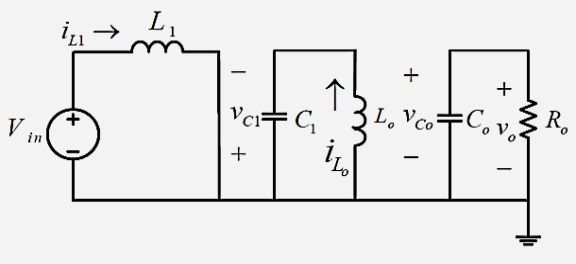


Figure 4. Operation of the SEPIC Converter Switch Off-Stage

The voltage across L1 and the input voltage are same as the Vin.

$$L_1 \frac{di_{L1}}{dt} = v_{in} - v_{c1} - v_{c0}$$

The voltage across Lo and the voltage across capacitor $C_1$ are same.

$$L_0 \frac{di_{L0}}{dt} = -v_{c0}$$

The current through $C_1$ and the current through inductor $L_2$ are same.

$$C_1 \frac{dv_{c1}}{dt} = i_{L1}$$

The current through Co and the currents through both inductors and the current of the load substrate.

$$C_0 \frac{dv_{c0}}{dt} = i_{L1} + i_{L0} - \frac{v_{c0}}{R}$$

A stabilized system is not easy to achieve with a second resonance point due to the significant high quality-factor of it. The un-damped resonance causes oscillations in the input current with the same frequency of the second resonance point. The oscillating current makes the system unstable.

## 4. Simulation Result

The proposed BLDCM drive is modelled in Matlab- Simulink environment and its performance is evaluated with load The DC link voltage is kept constant at 400 V with an input AC RMS voltage of 225V. The components of SEPIC converter are selected on the basis of power quality constraints at supply mains and allowable ripple in DC-link voltage as discussed as shown in Figure 5.

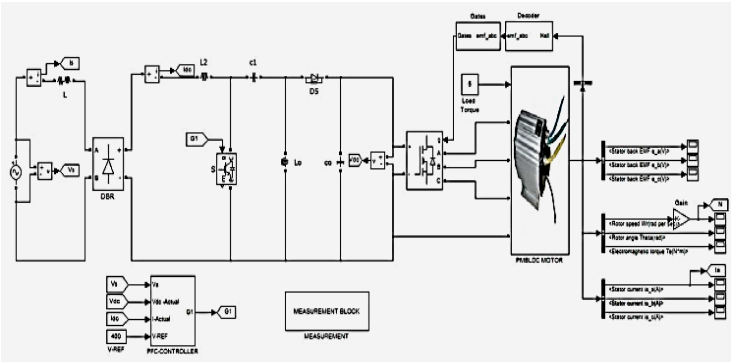


Figure 5. Simulation Diagram of the Proposed Circuit

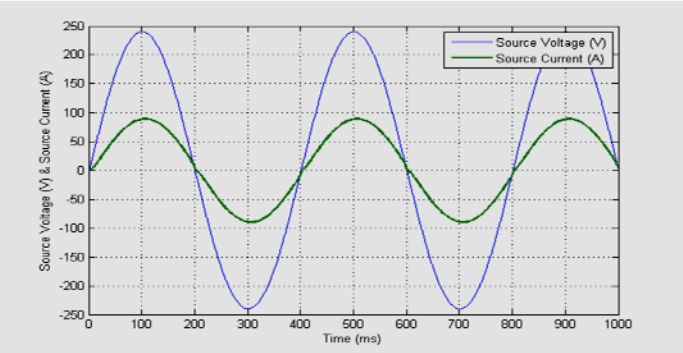


Figure 6. Source voltage and source current of a BLDCM drive representing unity power factor at peak source voltage of 240V

The controller gains are tuned to get the desired power quality parameters. The performance evaluation is made on the basis of various power quality parameters i.e. THD of current (THD %) at input AC mains, power factor and input AC current (Is). Figure 6 shows the current (I) waveform at input AC mains is in phase with the supply voltage (Vs) representing nearly unity power factor. The waveforms of power factor of BLDC motor drive are shown in Figure 7.

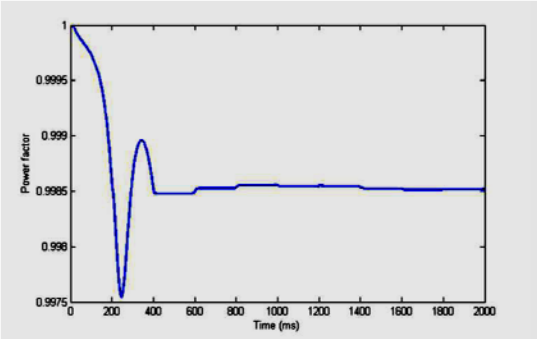


Figure 7. Power factor of the BLDC motor at peak source voltage of 240V

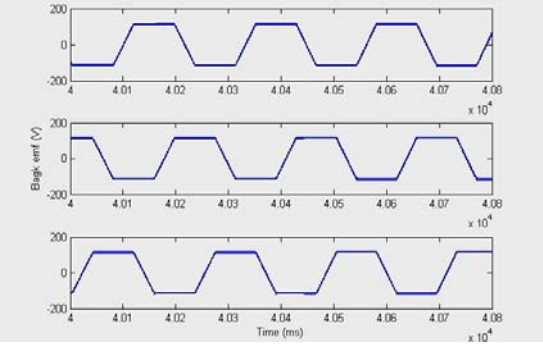


Figure 8. Trapezoidal back emf of the BLDC motor

Figure 8-10 show variation of current and its THD at AC mains with AC input voltage. The total harmonic distortions of AC mains current is observed well below 5% in most of the cases and satisfies the international standards along with nearly unity PF in wide range of AC input voltage.

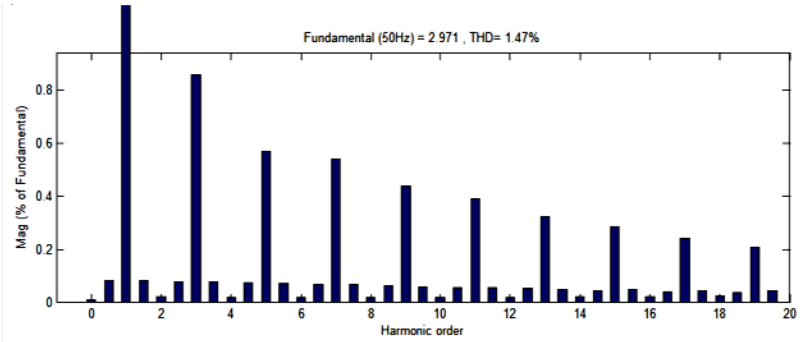


Figure 9. FFT analysis of a BLDCM drive at peak source voltage of 240V

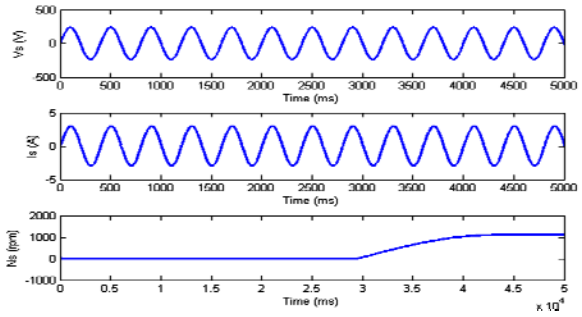


Figure 10. Performance of the PMBLDCM drive at peak source voltage of 240V

Table 1. PQ Parameters of a BLDCM at Variable Input AC Voltage

| (Vs) | (Is) | RPM | (THD %) | (PF) |
|---|---|---|---|---|
| 300 | 3.714 | 1354 | 1.94 | 0.9991 |
| 270 | 3.333 | 1220 | 1.71 | 0.9989 |
| 209 | 1.049 | 1030 | 1.30 | 0.9988 |
| 178 | 2.225 | 970 | 1.14 | 0.9987 |
| 120 | 1.486 | 690 | 0.98 | 0.9984 |
| 88 | 1.114 | 560 | 0.90 | 0.9982 |
| 56 | 0.723 | 381 | 1.24 | 0.9980 |
| 30 | 0.371 | 230 | 0.96 | 0.9985 |

The performance of the proposed BLDC motor drive is evaluated under varying input AC voltage to demonstrate the effectiveness of the proposed in various practical situations as in Table 1.

## 5. Conclusion

The Power quality of the BLDC motor drive had improved using SEPIC converter with the utilization of MATLAB Simulink software. The PFC converter has ensured reasonable high power factor close to unity in wide range of input voltage. The parameters shown in the Figure 6 to Figure10 represents an improved power quality, smooth speed control of the BLDCM drive. The THD of AC mains current is within specified limits of international norms. The performance of the drive is very good in the wide range of input AC voltage with desired power quality parameters At input supply voltage and wide range of speed is ensured reasonable high power factor close to unity with PFC converter. The international standard of THD for AC main current is satisfied as 5% in most of the cases in BLDC motor drive. Moreover an improved power quality with less torque ripple, smooth speed control of the BLDC motor drive which shown by performance parameters.

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