TELKOMNIKA Indonesian Journal of Electrical Engineering
Vol. 14, No. 1, April 2015, pp. 103 ~ 109
DOI: 10.11591/telkomnika.v14i1.7469

Scaling Model for Silicon Germanium Heterojunction Bipolar Transistors

Engelin Shintadewi Julian*, Rudy S. Wahjudi
Electrical Engineering Department, Trisakti University,
Jl. Kiai Tapa No. 1 Jakarta Barat Indonesia 11410,
*Corresponding author, e-mail: eshintadewij@yahoo.com

Abstract

In the past half-century, scaling has been used to improve semiconductor devices performance. In this paper, we study the effects of scaling on SiGe(C) heterojunction bipolar transistors (HBTs) performances i.e. cutoff frequency (f_T), maximum frequency of oscillation (f_{max}) and gate delay (τ_g). The SiGe HBT scaling models are developed from more than twenty years accumulated reported data. The results show that the peak cutoff frequency shows an increasing trend with emitter width scaling with a factor of ~$W_E^{-0.719}$, the peak maximum frequency of oscillation shows an increasing trend with emitter width scaling with a factor of ~$W_E^{-0.723}$ and the gate delay shows a decreasing trend with emitter width scaling with a factor of ~$W_E^{0.778}$.

***Keywords**: HBT, SiGe, scaling, model*

1. Introduction

Semiconductor devices have continuously been scaled down in size over the past few decades. Smaller devices are needed for several reasons. The main reason to make transistors smaller is to add more devices in a given chip area. This results in chips with more functionality in a smaller area. Smaller ICs allow more chips per wafer, reducing the chip price. It is also expected that smaller devices has better performance. The number of transistors per chip has been doubled every 2 years and was first obserbed by Gordon Moore in 1965 and is commonly reffered as Moore's law. For example, the number of transistors in Intel microprocessors has doubled every 26 months. The 4004 processor introduced in 1971 has 2300 transistors while the Xeon processor introduced in 2007 has 820 million transistors [1].

Figure 1 and 2 show the performance trends of Si-based bipolar transistors, which include SiGe and SiGeC HBTs. The data points are accumulated for more than two decades since early 1980s to 2000s [2]. The cutoff frequency trend in Figure 1 shows that in two decades, the cutoff frequency is increased by a factor of 30, from less than 10 GHz to more than 350 GHz. The trend of the gate delay in Figure 2 shows that over the past two decades the gate delay has been reduced by a factor of 1/25, from more than 100 ps to less than 4 ps. The Si-based bipolar transistors are suitable for RF and mixed-signal applications, which need high device speed but do not require device density as high as the digital applications. These performance trends are the evident results of constant improvement efforts, ultimately by vertical and lateral scaling, supported by material and structural innovations.

Over the past half-century, scaling has been the key to the improvement of semiconductor device performance. Scaling has worked for all types of transistors, including the SiGe dan SiGeC heterojunction bipolar transistors (HBTs). SiGe HBTs have SiGe as the base material which have smaller bandgap than that of Si. The SiGe base gives new degrees of freedom for the design of SiGe HBTs and allows much higher values of cutoff frequency to be achieved than in conventional silicon BJTs. The improvement in SiGe HBTs performance is shown by the reported SiGe HBTs with cutoff frequency exceeding 350 GHz [3].

Scaling rules are design rules which must be followed while scaling down geometry of semiconductor devices and interconnect lines. They provide device design parameters and performance parameters for a given saling factor based on certain requirements and constraints. Scaling rules for CMOS devices have been extensively developed and used as a

Received January 5, 2015; Revised March 3, 2015; Accepted March 20, 2015

tool for CMOS performance improvement. Even though scaling rules for bipolar transistors have not been extensively used in bipolar transistor performance improvement, there have been several efforts to developed scaling rules for bipolar transistor i.e. by Solomon and Tang [4], Bellaouar, Rosseel and Raje [3]. While there are rules to estimate the gate delay, as far as our knowledge there are no direct scaling rules to estimate the cutoff frequency and maximum frequency of oscillation. In this work, the scaling models to estimate the cutoff frequency (f_T), maximum frequency of oscillation (f_{max}) and gate delay (τ_g) for SiGe(C)-heterojunction bipolar transistors is developed based on published data over the span of of two decades.

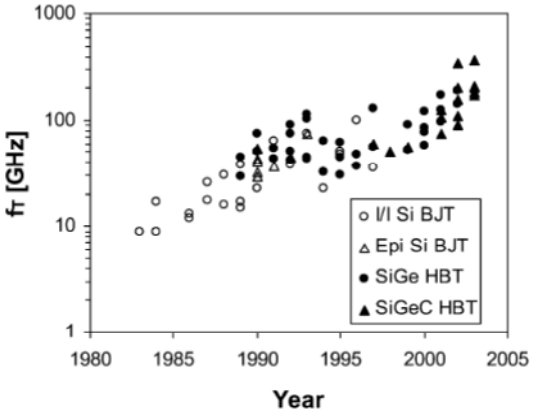

Figure 1. The trend of cutoff frequency (f_T) for Si-based transistors [3]

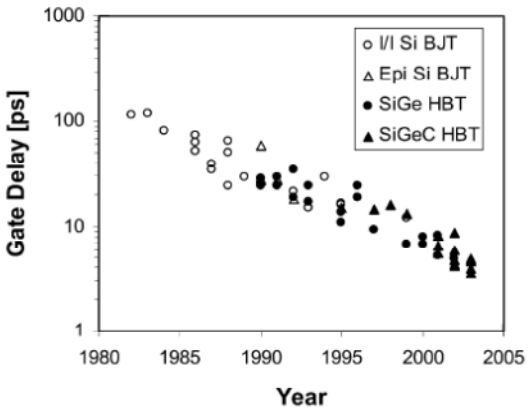

Figure 2. The trend of gate delay (τ_g) for Si-based transistors [3]

2. State of the Art of Bipolar Transistor Scaling Rules and Scaling Model Development

2.1. State of the Art Bipolar Transistor Scaling Rules

A theory for scaling bipolar transistors for ECL circuits has been developed by Solomon and Tang since 1979 and is shown in Table 1 [4]. The basic concept in this scaling theory is to reduce the dominant resistance and capacitance components in a coordinated manner so that the dominant delay components are reduced proportionally as the horizontal dimensions of the transistor are scaled down. In this way, if a transistor is optinlized for a given circuit design point before scaling, the transistor remains more or less optimized after scaling.

Table 1. Solomon and Tang scaling rules

Parameter	Scaling Rules
Feature size or emitter-stripe width W_E	$1/\kappa$
Base doping N_B	$\kappa^{1.6}$
Base width W_B	$1/\kappa^{0.8}$
Collector doping N_C	κ^2
Collector current density J_C	κ^2
Gate delay τ_g	$1/\kappa$

Scaling factor $\kappa > 1$

The others bipolar transistor scaling rules have been developed by Bellaouar, Rosseel and Raje, however despite the different constraints and approaches assumed, overall trends suggested bu these scaling rules for key bipolar parameters are not significantly far apart [3]. For example, when emitter stripe width is scaled by $1/\kappa$, the gate delay is expected to decrease by $1/\kappa$.

2.2. Data Collection and Mathematical Model Development

Before the scaling models for SiGe(C) HBTs are developed, the relation of lateral emitter width W_E to the cutoff frequency (f_T), maximum frequency of oscillation (f_{max}) and gate delay (τ_g) data are collected from secondary sources, i.e. from published papers over the span of two decades, from 1989 – 2010 [5] – [67]. The scaling models are assumed to have a simple power equation, for example the cutoff frequency (f_T)

$$f_T = AW_E^{\ B} \tag{1}$$

Linearization of Equation (1) yields:

$$\log f_T = \log A + B \log W_E \tag{2}$$

Least square linear regression is then applied for fitting the best line to data, and yields:

$$n \log A + \left(\sum \log W_{E,i}\right) B = \sum \log f_{T,i} \tag{3}$$

$$\left(\sum \log W_{E,i}\right) \log A + \left(\sum \log W_{E,i}^2\right) B = \sum log W_{E,i} \log f_{T,i} \tag{4}$$

3. Results and Analysis

The correlation between the peak cutoff frequencies (f_T) and emitter stripe widths (W_E) are presented in Figure 3, which shows compiled published data obtained from SiGe and SiGeC HBTs over the past two decades. The peak cutoff frequency shows an increasing trend with emitter width scaling, with a factor of ~$WE^{-0.719}$. It should be noted, though, that the data points in the plot are spread and the correlation factor (R^2) is 0.49, which means there are strong relationship beetwen f_T and W_E.

Figure 4 shows the trend of peak maximum frequency of oscillation f_{max} over the emitter width, with correlation factor (R^2) 0.58, which is better correlated than the cutoff frequency trend. A scaling factor of ~$W_E^{-0.723}$ is extracted, which is similar to cutoff frequency trend. Contrary to our expectation base on our previous results [69], the peak cutoff frequency and the peak maximum frequency of oscillation have similar increasing trend with emitter width scaling.

The correlation between the gate delay and emitter width are presented in Figure 5, which exhibits a decreasing trend with emitter width scaling, with a factor of ~$W_E^{0.7782}$ and the correlation factor is 0.58. The trend is lower than expected from scaling rules i.e. 1/κ, however the trend is slightly higher than compared to Rieh with ~$W_E^{0.725}$ [3].

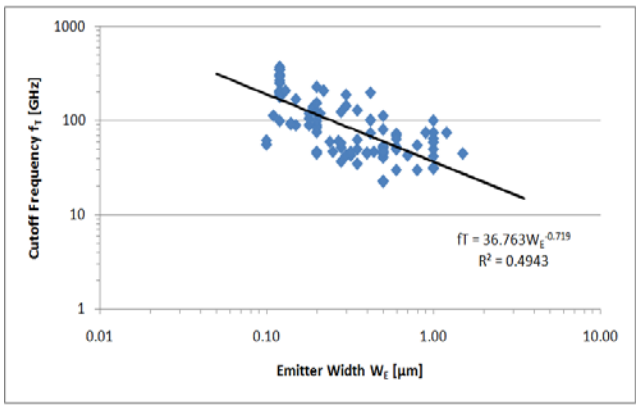

Figure 3. Scaling trend for peak cutoff frequency (f_T); Trend equations over W_E are also shown, along with correlation factor R

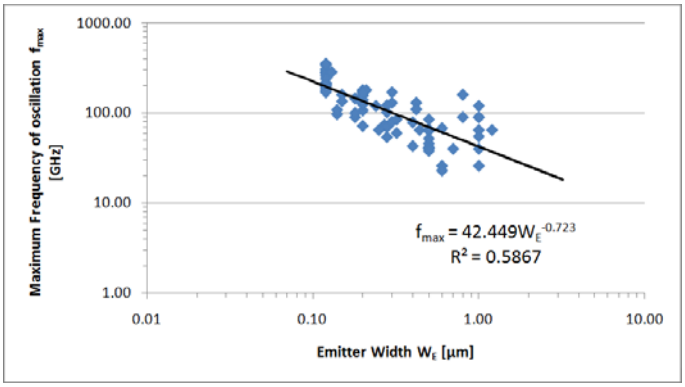

Figure 4. Scaling trend for peak maximum frequency of oscillation f_{max}

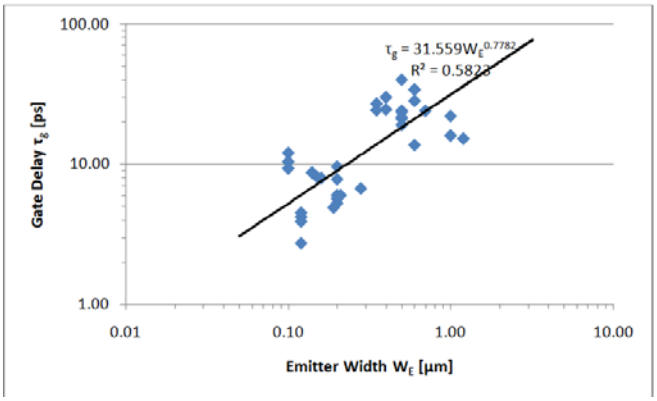

Figure 4. Scaling trend for the gate delay τ_g

4. Conclusion

1) It is shown that lateral scaling has beneficial effects on device performances such as cutoff frequency, maximum frequency of oscillation and gate delay.

2) The peak cutoff frequency shows an increasing trend with emitter width scaling with a factor of $\sim W_E^{-0.719}$.

3) The peak maximum frequency of oscillation shows an increasing trend with emitter width scaling with a factor of $\sim W_E^{-0.723}$.

4) The gate delay shows a decreasing trend with emitter width scaling with a factor of $\sim W_E^{0.778}$.

References

[1] Intel Corporation. Microprocessor Quick Reference Guide. www.intel.com/pressroom/kits/quickreffam.htm. 2010.

[2] Rieh JS, Greenberg D, Stricker A, Freeman G. *Scaling of SiGe Heterojunction Bipolar Transistors*. Proc. of the IEEE. 2007; 93(9): 1522-1538.

[3] Rieh JS, Jagannathan B, Chen H, Schonenberg KT, Angell D, Chinthakaindi A, Florkey J, Golan F, Greenberg D, Jeng SJ, Khater M, Pagette F, Schnabel C, Smith P, Stricker A, Vaed K, Volant R, Ahlgren D, Freeman G, Stein K, Subbanna S. *SiGe HBTs with Cut-off Frequency of 350 GHz*. IEDM Tech. Digest. 2002: 771–774.

[4] Solomon PM, Tang DD. *Bipolar circuit scaling*. Dig. Int. Solid-State Circuits Conf. 1979: 86-87.

[5] Crabbe EF, Patton GL, Stork JMC, Comfort JH, Meyerson BS, Sun JYC. *Low temperature operation of Si and SiGe bipolar transistors*. IEDM Tech. Dig. 1990: 17-20.

[6] Comfort JH, Patton GL, Cressler JD, Lee W, Crabbe EF, Meyerson BS, Sun JYC, Stork JMC, Lu PF, Burghartz JN, Warnock J, Scilla G, Toh KY, D'Agostino M, Stanis C, Jenkins K. *Profile leverage in self-aligned epitaxial Si or SiGe base bipolar technology*. IEDM Tech. Digest. 1990: 21-24.

[7] Burghartz JN, Comfort JH, Patton GL, Cressler JD, Meyerson BS, Stork JMC, Sun JY-C, Scilla G, Warnock J, Ginsberg BJ, Jenkins K, Toh KY, Harame DL, Mader SR. *Sub-30 ps ECL circuits using high-f Si and SiGe epitaxial base SEEW transistors*. IEDM Tech. Digest. 1990: 297-300.
[8] Comfort JH, Crabbe EF, Cressler JD, Lee W, Sun JYC, Malinowski J, D'Agostino M, Burghartz JN, Stork JMC, Meyerson BS. *Single crystal emitter gap for epitaxial Si- and SiGebase transistors*. IEDM Tech. Digest.1991: 857–860.
[9] Pruijmboom A, Terpstra D, Timmering CE, de Boer WB, Theunissen MJJ, Slotboom JW, Hueting RJE, and Hageraats JJEW. *Selective-epitaxial base technology with 14 ps ECL gate delay, for low power wide-band communication systems.* IEDM Tech. Digest. 1995: 747–750.
[10] Crabbe EF, Meyerson BS, Stork JMC, Harame DL. *Vertical profile optimization of very high frequency epitaxial Si and SiGe-base bipolar transistors*. IEDM Tech. Digest. 1993: 83–86.
[11] Narozny P, Dambkes H, Kibbel H, Kasper E. Si/SiGe heterojunction bipolar transistor made by molecular-beam epitaxy. *IEEE Trans. Electron Devices*, 1989; 36(10): 2363–2366.
[12] Fischer SE, Cook RK, Knepper RW, Lange RC, Nummy K, Ahlgren DC, Revitz M, Meyerson BS. *A 45 GHz strained layer SiGe heterojunction bipolar transister fabricated with low temperature epitaxy*. IEDM Tech. Digest. 1989: 890-892.
[13] Patton GL, Comfort JH, Meyserson BS, Crabbe EF, Scilla GJ, Fresart ED, Stork JMC, Sun JYC, Harame DL, Burghartz JN. 75-GHz ft SiGe-base heterojunction bipolar transistor. *IEEE Electron Device Lett.* 1990; 11(4): 171-173.
[14] Cressler JD, Comfort JH, Crabbe EF, Patton GL, Lee W, Sun JYC, Stork JMC, and Meyerson BS. Sub-30-ps ECL circuit operation at liquid-nitrogen temperature using self-aligned epitaxial SiGe-base bipolar transistors. *IEEE Electron Device Lett*. 1991; 12(4): 166-168.
[15] Crabbe EF, Comfort JH, Lee W, Cressler JD, Meyerson BS, Megdanis C, Sun JYC, Stork JMC. 73-GHz self-aligned SiGe-base bipolar transistors with phosphorus-doped polysilicon emitters. *IEEE Electron Device Lett.* 1992; 13(5): 259-261.
[16] Gruhle A, Kibbel H, Konig U, Erben U, Kasper E. MBEgrown Si/SiGe HBTs with high β, f_T, and f_{max}. *IEEE Electron Device Lett*. 1992; 13(4): 206–208.
[17] Crabbe EF, Comfort JH, Cressler JD, Sun JYC, Stork JMC. High-low polysilicon-emitter SiGe-base bipolar transistors. *IEEE Electron Device Lett*. 1993; 14(10): 478-480.
[18] Kasper E, Gruhle A, Kibbel H. *High speed SiGe-HBT with very low base sheet resistivity*. IEDM Tech. Digest. 1993: 79–81.
[19] Harame DL, Stork JMC, Meyerson BS, Hsu KYJ, Cotte J, Jenkins KA, Cressler JD, Restle P, Crabbe EF, Subbanna S, Tice TE, Scharf BW, Yasaitis JA, *Optimization of SiGe HBT technology for high speed analog and mixed-signal applications*. IEDM Tech. Digest. 1993: 71–74.
[20] Burghartz JN, Jenkins KA, Grutzmacher DA, Sedgwick TO, Stanis CL. High-performance emitter-up/down SiGe HBTs. *IEEE Electron Device Lett*. 1994; 15(9): 360-362.
[21] Schuppen A, Gruhle A, Erben U, Kibbel H, Konig U. *Multi emitter finger SiGe-HBTs with f_{max} up to 120 GHz*. IEDM Tech. Digest. 1994: 377–380.
[22] Schuppen A, Erben U, Gruhle A, Kibbel H, Schumacher H, Konig U. *Enhanced SiGe heterojunction bipolar transistors with 160 GHz-f_{max}*. IEDM Tech. Digest.1995: 743–746.
[23] Meister TF, Schafer H, Franosch M, Molzer W, Aufinger K, Scheler U, Walz C, Stolz H, Boguth S, Bock J. *SiGe base bipolar technology with 74 GHz f and 11 ps gate delay*. IEDM Tech. Digest. 1995: 739-742.
[24] Kondo M, Oda K, Ohue E, Shimamoto H, Tanabe M, Onai T, Washio K. *Sub-10-fJ ECL/68-mA 4.7-GHz divider ultra-lowpower SiGe base bipolar transistors with a wedge-shaped CVD-SiO isolation structure and a BPSG-refilled trench*. IEDM Tech. Digest. 1996: 245–248.
[25] Ahlgren D, Gilbert M, Greenberg D, Jeng SJ, Malinowski J, Nguyen-Ngoc D, Schonenberg K, Stein K, Groves R, Walter K, Hueckel G, Colavito D, Freeman G, Sunderland D, Harame DL, Meyerson B. *Manufacturability demonstration of an integrated SiGe HBT technology for the analog and wireless marketplace*. IEDM Tech. Digest. 1996: 859–862.
[26] Washio K, Ohue E, Oda K, Tanabe M, Shimamoto H, Onai T. *A selective-epitaxial SiGe HBT with SMI electrodes featuring 9.3-ps ECL-gate delay*. IEDM Tech. Digest. 1997: 795-798.
[27] Oda K, Ohue E, Tanabe M, Shimamoto H, Onai T, Washio K, *130 GHz-f_T SiGe HBT technology*. IEDM Tech. Digest. 1997: 791-794.
[28] King CA, Frei MR, Mastrapasqua M, Ng KK, Kim YO, Johnson RW, Moinian S, Martin S, Cong H-I, Klemens FP, Tang R, Nguyen D, Hsu T-I, Campbell T, Molloy SJ, Fritzinger LB, Ivanov TG, Bourdelle KK, Lee C, Chyan Y-F, Carroll MS, Leung CW. *Very low cost graded SiGe base bipolar transistors for a high performance modular BiCMOS process*. IEDM Tech. Digest. 1999: 565–568.
[29] Washio K, Kondo M, Ohue E, Oda K, Hayami R, Tanabe M, Shimamoto H, Harada T. *A 0.2-μm self-aligned SiGe HBT featuring 107-GHz f_T and 6.7-ps ECL*. IEDM Tech. Digest. 1999: 557-560.
[30] Freeman G, Ahlgren D, Greenberg D, Groves R, Huang F, Hugo G, Jagannathan B, Jeng S, Johnson J, Schonenberg K, Volant R, Subbanna S. *A 0.18 μm 90 GHz f_T SiGe HBT BiCMOS, ASIC compatible, copper interconnect technology for RF and microwave applications*. IEDM Tech. Digest. 1999: 569–572.

[31] Washio K, Ohue E, Shimamoto H, Oda K, Hayami R, Kiyota Y, Tanabe M, Kondo M, Hashimoto T, Harada T. *A 0.2-μm 180-GHz-f 6.7-ps-ECL SOI/HRS self aligned SEG SiGe HBT/CMOS technology for microwave and high-speed digital applications*. IEDM Tech. Digest. 2000: 741–744.
[32] Carroll M, Ivanov T, Kuehne S, Chu J, King C, Frei M, Mastrapasqua M, Johnson R, Ng K, Moinian S, Martin S, Huang C, Hsu T, Nguyen D, Singh R, Fritzinger L, Esry T, Moller W, Kane B, Abeln G, Hwang D, Orphee D, Lytle S, Roby M, Vitkavage D, Chesire D, Ashton R, Shuttleworth D, Thoma M, Choi S, Lewllen S, Mason P, Lai T, Hsieh H, Dennis D, Harris E, Thomas S, Gregor R, Sana P, Wu W. *COM2 SiGe modular BiCMOS technology for digital, mixed-signal, and RF applications*. IEDM Tech. Digest. 2000: 145-148.
[33] Bock J, Meister TF, Knapp H, Zoschg D, Schafer H, Aufinger K, Wurzer M, Boguth S, Franosch M, Stengl R, Schreiter R, Rest M, Treitinger L. *SiGe bipolar technology for mixed digital and analogue RF applications*. IEDM Tech. Digest. 2000: 745–748.
[34] Racanelli M, Schuegraf K, Kalburge A, Kar-Roy A, Shen B, Hu C, Chapek D, Howard D, Quon D, Wang F, U'ren G, Lao L, Tu H, Zheng J, Zhang J, Bell K, Yin K, Joshi P, Akhtar S, Vo S, Lee T, Shi W, Kempf P. *Ultra high speed SiGe NPN for advanced BiCMOS technology*. IEDM Tech. Digest. 2001: 15.3.1–15.3.4.
[35] Ohue E, Hayami R, Oda K, Shimamoto H, and Washio K. *5.3-ps ECL and 71-GHz static frequency divider in self-aligned SEG SiGe HBT*. Proc. Bipolar/BiCMOS Circuits and Technology Meeting. 2001: 26-29.
[36] Washio K, Ohue E, Oda K, Hayami R, Tanabe M, Shimamoto H. A 50-GHz static frequency divider and 40-Gb/s MUX/DEMUX using self-aligned selective-epitaxial-growth SiGe HBTs with 8-ps ECL. *IEEE Trans. Electron Devices*. 2001; 48(7): 1482-1487.
[37] Washio K, Ohue E, Hayami R, Kodama A, Shimamoto H, Miura M, Oda K, Suzumura I, Tominari T, Hashimoto T. *Ultrahigh-speed scaled-down self-aligned SEG SiGe HBTs*. IEDM Tech. Digest. 2002: 767-770.
[38] Kiyota Y, Hashimoto T, Udo T, Kodama A, Shimamoto H, Hayami R, Washio K. *190-GHz fT, 130-GHz fmax SiGe HBTs with heavily doped base formed by HCL-free selective epitaxy*. Proc. Bipolar/BiCMOS Circuits and Technology Meeting. 2002: 139-142.
[39] Osten HJ, Lippert G, Knoll D, Barth R, Heinemann B, Rucker H, Schley P. *The effect of carbon incorporation on SiGe heterobipolar transistor performance and process margin*. IEDM Tech. Digest.1997: 803–806.
[40] Knoll D, Heinemann B, Osten HJ, Ehwald B, Tillack B, Schley P, Barth R, Matthes M, Park KS, Kim Y, Winkler W. *Si/SiGe:C heterojunction bipolar transistors in an epi-free well, single-polysilicon technology*. IEDM Tech. Digest.1998: 703–706.
[41] Ehwald KE, Knoll D, Heinemann B, Chang K, Kitchgessner J, Mauntel R, Lim IS, Steele J, Schley P, Tillack B, Wolff A, Blum K, Winkler W, Pierschel M, Jagdhold U, Barth R, Grabolla T, Erzgraber HJ, Hunger B, Osten HJ. *Modular integration of high-performance SiGe:C HBTs in a deep submicron, epi-free CMOS process*. IEDM Tech. Digest. 1999: 561-564.
[42] Bock J, Schafer H, Knapp H, Zoschg D, Aufinger K, Wurzer M, Boguth S, Stengl R, Schreiter R, Meister TF. *High-speed SiGe:C bipolar technology*. IEDM Tech. Digest. 2001: 15.5.1–15.5.4.
[43] Oda K, Ohue E, Suzumura I, Hayami R, Kodama A, Shimamoto H, Washio K. *Self-aligned selective-epitaxial-growth Si Ge C HBT technology featuraing 170-GHz fmax*. IEDM Tech. Digest. 2001: 332–335.
[44] Heinemann B, Knoll D, Barth R, Bolze D, Blum K, Drews J, Ehwald KE, Fischer GG, Kopke K, Kruger D, Kurps R, Rucker H, Schley P, Winkler W, Wulf H-E. *Cost-effective high-performance high-voltage SiGe:C HBTs with 100 GHz f_T and BV_{CEO} x f_T products exceeding 220 GHz*. IEDM Tech. Digest. 2001: 15.6.1–15.6.4.
[45] Jagannathan B, Meghelli M, Rylyakov AV, Groves RA, Chinthakindi AK, Schnabel CM, Ahlgren D, Freeman G, Stein KJ, Subbanna S. A 4.2-ps ECL ring-oscillator in a 285-GHz fmax SiGe technology. *IEEE Electron Device Lett*. 2002; 23(9): 541–543.
[46] Knoll D, Heinemann B, Ehwald KE, Rucker H, Tillack B, Winkler W, Schley P. *BiCMOS integration of SiGe:C heterojunction bipolar transistors*. Proc. Bipolar/BiCMOS Circuits and Technology Meeting. 2002: 162–166.
[47] Bock J, Schafer H, Knapp H, Zoschg D, Aufinger K, Wurzer M, Boguth S, Rest M, Schreiter R, Stengl R, Meister TF. *Sub 5 ps SiGe bipolar technology*. IEDM Tech. Digest. 2002: 763–766.
[48] Heinemann B, Rucker H, Barth R, Bauer J, Bolze D, Bugiel E, Drews J, Ehwald K-E, Grabolla T, Haak U, Hoppner W, Knoll D, Kruger D, Kuck B, Kurps R, Marschmeyer M, Richter HH, Schley P, Schmidt D, Scholz R, Tillack B, Winkler W, Wolnsky D, Wulf H-E, Yamamoto Y, Zaumseil P. *Novel collector design for high-speed SiGe:C HBTs*. IEDM Tech. Digest. 2002: 775–778.
[49] Grahn JV, Fosshaug H, Jargelius M, Jonsson P, Linder M, Malm BG, Mohadjeri B, Pejnefors B, Radamson HH, Sanden M, Wang YB, Landgren G, Ostling M. A low-complexity 62-GHz fT SiGe heterojunction bipolar transistor process using differential epitaxy and in situ phosporus-doped poly-Si emitter at very low thermal budget. *Solid State Electronics*. 2000; 44: 349-554.

[50] Jeng SJ, Jagannathan B, Rieh JS, Johnson J, Schonenberg KT, Greenberg D, Stricker A, Chen H, Khater M, Ahlgren D, Freeman G, Stein K, Subbanna S. A 210-GHz fT SiGe HBT with a Non-Self-Aligned Structure. *IEEE Electron Dev. Lett.* 2001; 22(11).
[51] Zhang S, Niu G, Cressler JD, Joseph AJ, Freeman G, Harame DL. The Effects of Geometrical Scaling on the Frequency Response and Noise Performance of SiGe HBTs. *IEEE Trans. Electron Devices*. 2002; 46(3): 429 – 435.
[52] Jagannathan B, Khater M, Pagette F, Rieh J-S, Angell D, Chen H, Florkey J, Golan F, Greenberg DR, Groves R, Jeng SJ, Johnson J, Mengistu E, Schonnenberg KT, Schnabel CM, Smith P, Stricker A, Ahlgren D, Freeman G, Stein K, Subbanna S. Self-Aligned SiGe NPN Transistors With 285 GHz fmax and 207 GHz fT in a Manufacturable Technology. *IEEE Electron Device Lett*. 2002; 23(5): 238–260.
[53] Joseph AJ, Dunn J, Freeman G, Harame DL, Coolbaugh D, Groves R, Stein KJ, Volant R, Subbanna S, Marangos VS, Onge SSt, Eshun E, Cooper P, Johnson JB, Rieh J-S, Jagannathan B, Ramachandran V, Ahlgren D, Wang D, Wang X. Product Applications and Technology Directions With SiGe BiCMOS. *IEEE Journal of Solid Stated Circuits*. 2003; 38(9): 1471-1478.
[54] Johansen J, Jin B, Cressler JD, Cui Y, Niu G, Liang Q, Rieh JS, Freeman G, Ahlgren D, Joseph A. *On the Scaling Limits of Low-Frequency Noise in SiGe HBTs*. International Semiconductor Device Research Symposium. 2003: 12-13.
[55] Orner BA, Liu QZ, Rainey B, Stricker A, Geiss P, Gray P, Zierak M, Gordon M, Collins D, Ramachandran V, Hodge W, Willets C, Joseph A, Dunn J, Rieh J-S, Jeng S-J, Eld E, Freeman G, Ahlgren D. *A 0.13um BiCMOS Technology Featuring a 200/280 GHz (fT/fmax) SiGe HBT*. IEEE BCTM. 2003: 203 - 206.
[56] Rieh J-S, Jagannathan B, Chen H, Schonenberg K, Jeng S-J, Khater M, Ahlgren D, Freeman G, Subbanna S. *Performance and Design Considerations for High Speed SIGe HBTs of fT/fmax=375/210 GHz*. Intl. Conf on Indium Phosphide and Related Materials. 2003: 374 - 377.
[57] Magnee PHC, Hurkx GAM, Agarwal P, van Noort WD, Donkers JJTM, Melai J, Aksen E, Vanhoucke T, Vijayaraghavan MN. *SiGe:C HBT technology for advanced BiCMOS processes*. 12th GaAs Symposium. 2004: 243 – 246.
[58] Chen T, Kuo W-ML, Zhao E, Liang Q, Jin Z, Cressler JD, Joseph AJ. On the High-Temperature (to 300 C) Characteristics of SiGe HBTs. *IEEE Trans. Electron Devices*. 2004; 51(11): 1825-1832.
[59] Stricker AD, Johnson JB, Freeman G, Rieh JS. Design and optimization of a 200 GHz SiGe HBT collector profile by TCAD. *Applied Surface Science*. 2004; 224: 324–329.
[60] Joseph A, Lanzerotti L, Liu X, Sheridan D, Johnson J, Liu Q, Dunn J, Rieh JS, Harame D. *Advances in SiGe HBT BiCMOS Technology*. IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems. 2004: 1-4.
[61] Khater M, Rieh JS, Adam T, Chinthakindi A, Johnson J, Krishnasamy R, Meghelli M, Pagette F, Sanderson D, Schnabel C, Schonenberg KT, Smith P, Stein K, Stricker A, Jeng SJ, Ahlgren D, Freeman G. *SiGe HBT Technology with fmax/fT = 350/300 GHz and Gate Delay Below 3.3 ps*. IEDM. 2004.
[62] Rieh JS, Greenberg D, Khater M, Schonenberg KT, Jeng S-J, Pagette F, Adam T, Chinthakindi A, Florkey J, Jagannathan B, Johnson J, Krishnasarny R, Sanderson D, Schanbel C, Smith P, Stricker A, Sweeney S, Vaed K, Yanagisawa T, Ahlgren D, Stein K, Freeman G. *SiGe HBTs for Millimeter-Wave Applications with Simultaneously Optimized fT and fmax of 300 GHz*. IEEE Radio Frequency Integrated Circuits Symposium. 2004: 394 - 397.
[63] Rieh JS, Jagannathan B, Greenberg DR, Meghelli M, Rylyakov A, Guarin F, Yang Z, Ahlgren DC, Freeman G, Cottrell P, Harame D. SiGe Heterojunction Bipolar Transistors and Circuits Toward Terahertz Communication Applications. *IEEE Trans. On Microwave Theory and Techniques*. 2004; 52(10).
[64] Krithivasan R, Lu Y, Cressler JD, Rieh JS, Khater MH, Ahlgren D, Freeman G. Half-Terahertz Operation of SiGe HBTs. *IEEE Electron Dev. Lett*. 2006; 27(7): 567-569.
[65] Rieh J-S, Khater M, Freeman G, Ahlgren D. SiGe HBT without Selectively Implanted Collector (SIC) Exhibiting fmax = 310 GHz and BVCEO = 2 V. *IEEE Trans. On Electron Dev*. 2006; 53(9): 2407-2409.
[66] Yuan J, Cressler JD, Krithivasan R, Thrivikraman T, Khater MH, Ahlgren DC, Joseph AJ, Rieh JS. On the Performance Limits of Cryogenically Operated SiGe HBTs and Its Relation to Scaling for Terahertz Speeds. *IEEE Trans. On Electron Dev*. 2009; 56(5): 1007-1019.
[67] Yuan J, Moen KA, Cressler JD, Rücker H, Heinemann B, Winkler W. SiGe HBT CML Ring Oscillator With 2.3-ps Gate Delay at Cryogenic Temperatures. *IEEE Trans. On Electron Dev*. 2010; 57(5): 1183-1187.
[68] Julian ES. Silicon Germanium Heterojunction Bipolar Transistor for Digital Aplication. *Telkomnika*, 2012; 10(3): 493 – 498.