

## Design and implementation of modified multilevel sepic converter for PV applications

T. Arunkumari, I. Jagadeesh, V. Indragandhi

School of Electrical Engineering, Vellore Institute of Technology, Vellore, India

---

### Article Info

#### Article history:

Received Sep 20, 2018

Revised Nov 18, 2018

Accepted Feb 28, 2019

---

#### Keywords:

High voltage conversion

Irradiation

Multilevel sepic converter

Photo voltaic

Ripple voltage

---

### ABSTRACT

In this manuscript, a DC-DC converter of modified multilevel sepic model with single switch is proposed here. The designed converter combines the voltage tripler circuit, which improves the voltage gain and reduces the voltage ripple of the system. Another feature of the designed converter is reduces the voltage stress and utilized for PV based applications. The operation of the designed converter in Continuous-Conduction Mode (CCM) is discussed. The converter boosts the PV input voltage of 30 V to 400 V output voltages. The efficiency attained by the designed converter is 94%. The Theoretical analysis of the designed converter is presented and it is done with MATLAB simulink. To analyse the performance of this DC-DC converter a model was developed and tested. From the experimental results obtained, it is analysed that the converter performs better and suitable for PV based application.

Copyright © 2019 Institute of Advanced Engineering and Science.  
All rights reserved.

---

### Corresponding Author:

V. Indragandhi,

School of Electrical Engineering,

Vellore Institute of Technology, Vellore, India.

Email: arunindra08@gamil.com

---

## 1. INTRODUCTION

The changes of rising oil costs and progressively stressing level of contamination appeared differently in relation to the new arrangements of feasible improvement to make elective and sustainable power sources more alluring. Financial motivators and gigantic progression in electronic innovation advance the utilization of PV frameworks. These frameworks show a straightforward and advantageous arrangement from a financial perspective. The utilization of a converter on these photovoltaic frameworks is much additionally convincing as it builds their effectiveness and diminishes their expenses. However, the reduced voltage of these non-conventional energy technologies requires for high efficacy high step-up DC-DC converter [1].

Hypothetically, increased voltage level ratio could be acquired by the ordinary DC- DC model converters, for example, voltage-lift sort and step-up mode converters with large duty ratio [2]. Though, these converters are not reasonable competitors in large advance up application in light of the fact that the main flexibility to expand the voltage ratio is the duty -cycle that ought to be large and this would fall apart the reliability of the DC converter. Outrageous duty ratio forces little off-times and less switching frequency. Additionally the semi-conductors experience the ill effects of huge highest currents and huge voltage strain which prompt use control switches which changes with huge on-state protection (RDS-ON). At that point together switching and on-state fatalities are expanded and the transformation effectiveness is diminished. Many high boosts up voltage converters are proposed to raise the voltage ratio and efficiency of the converter which is categorized in to three zones. The primary category utilizes the Switched Capacitor (SC), switched-inductor, Voltage-Multiplier Cells (VMCs) which combines with voltage lift technique [3-9].

Parallel organized arrangement of cockcroft-walton VMCs has been implemented to improve the voltage ratio limit in a stretchy path [10]. The voltage sources of all storage capacitors along the VMCs are

similar which raises the elasticity of the model. An Integrated Double Boost SEPIC (IDBS) mode converter is projected as a large step-up mode converter in [11]. Variant and categorization of tapped-inductor mode converters are represented in [12]. Parallel and stacked mode coupled-inductor step up mode converters have been designed in [13-15], correspondingly. This designs converters are ease and cost reasonable with only single-active switch. The gain of the voltage can be improved through duty cycle and the High Frequency Coupled Inductor (HFCI) turns. The authors in [16-17], have incorporated a half-wave VMC of a storage capacitor and a active diode hooked on the converter of position [20].

The coupled mode inductor works as a forward mode transformer to accuse the storage capacitor in turn-on condition and as a fly-back mode inductor to free vitality to the output source in turn-off condition. Thus, magnetic source core use is increased. In [18], two ways half-wave VMCs are located on together sides of the secondary-winding. By incorporation of HFCI and a half wave VMC in sequence mode with the power MOSFET, a easy high voltage ratio DC-DC mode converter has been derived in [19]. The single switch sepic converter with VM has been proposed in [21].The converter in [22], involves the coupled-inductor, the voltage-lift circuit mode and the clamping mode circuit. The model in [23] is shaped by paralleling a usual boost type converter and a coupled-inductor boost mode converter by contributing the power-MOSFET. This converter character not only reduces ripple current, but also quadratic-voltage gain ratio of the converter. However, due to parallel working of this design, the efficacy is not promised. Switched capacitor model and inductor model are utilized to improve the gain [24-26]

The manuscript is organized as below. In Section 2, the operation of the proposed converter in CCM and DCM mode is explained. In Section 3 the design and analysis of the proposed converter is explained. In Section 4 Comparative analysis of proposed converter with conventional converter is explained. In Section 5 experimental results are evaluated. Conclusion is followed by Section 6.

**2. OPERATION OF THE PROPOSED CONVERTER**

The proposed circuit is represented in Figure 2. The converter design consists of main switch  $S_1$ , inductors  $L_1, L_2$ , diodes  $D_1, D_2, D_3, D_4, D_5$  and  $D_6$ , capacitors  $C_1, C_2, C_3, C_4, C_5$  and output capacitor  $C_6$ . The VT circuit is combined with sepic converter to improve the voltage gain level of the converter. The switching voltage in the semiconductor device is reduced. Capacitors operate as similar operation in conventional boost converter.

**2.1. Continuous Conduction Mode Operation**

The proposed converter operates in two modes. The modes of operations are shown in Figure 1 and Figure 2. *Mode I [t0-t1]*: When the switch  $S_1$  is turned-on diodes  $D_2, D_4$  and  $D_6$  is turned ON. Diode  $D_1, D_3$  and  $D_5$  are reverse biased. The voltage  $V_{in}$  is delivered to  $L_1$  and  $V_{C3} - V_{C2} - V_{C1}$  is delivered to  $L_2$ . These inductors help in storing the energy. The Output capacitor  $C_0$  discharges the required energy to the load for its operation. When the switch turns off, this mode ends. Also the diode  $D_3$  and  $D_0$  current attains zero at  $t=t_1$ .

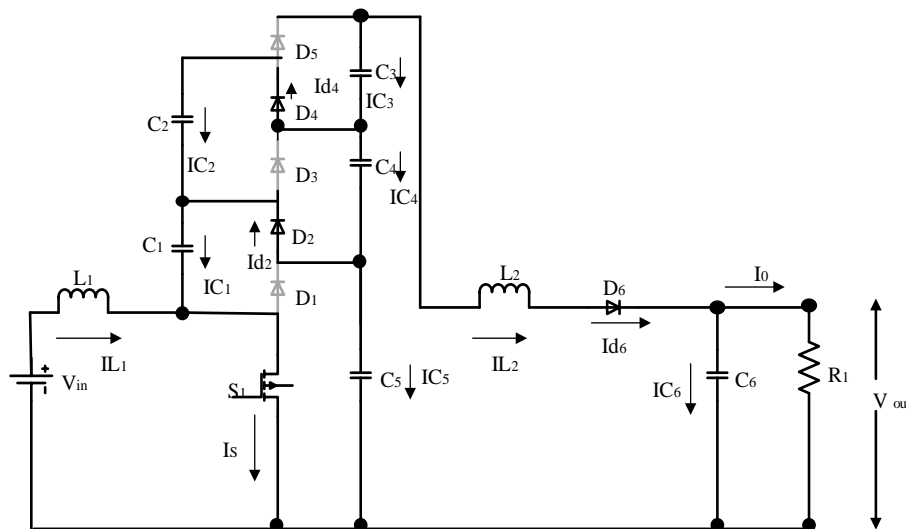


Figure 1. Proposed DC-DC converters turn on mode

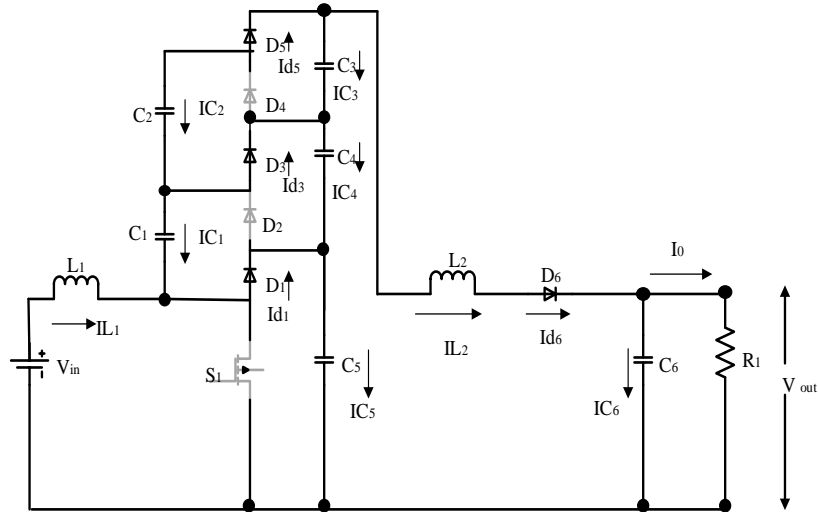


Figure 2. Proposed DC-DC converters turn off mode

*Mode II [t1–t2]:* When the switch  $S_2$ , is turned OFF, the diodes  $D_2$  and  $D_4$  are in OFF condition. The diodes  $D_1, D_3$  and  $D_5$  are in forward condition. The capacitors are charged by the inductor  $L_1$  and  $L_2$ . The load receives the energy by discharging mode of the capacitor. This operation ends when Switch is turned ON. The next cycle continues.

The main operational waveform is represented in Figure 3. The total capacitive voltage is equal to the output voltage of the converter.

$$V_o = V_{C3} + V_{C4} + V_{C5} + V_{C6} \tag{1}$$

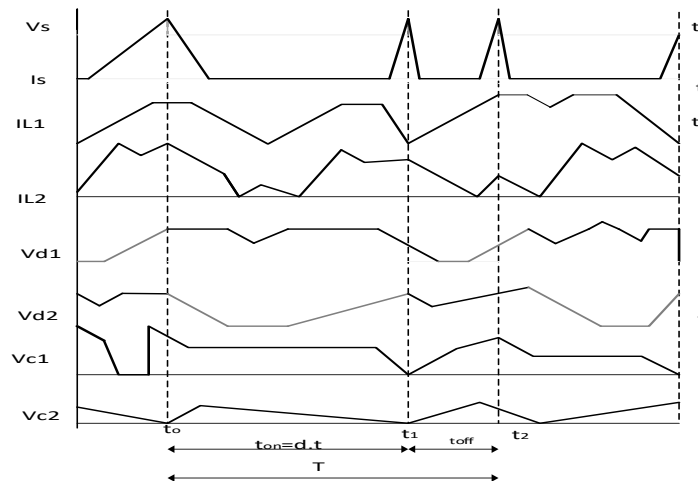


Figure 3. CCМ operation waveforms

### 3. ANALYSIS OF THE PROPOSED CONVERTER

In this section the theoretical analysis of the proposed sepic converter is explained by following with design procedural of the converter proposed.

#### 3.1. Static Gain and Switching Voltage Analysis:

At steady condition, the inductor value is considered as null and the equation is termed as below and hence in CCМ operation, the inductor  $L_1$  is given as

$$V_{in} d = V_{C6} - 3V_{in}(1-D) \tag{3}$$

Here  $d$  is duty cycle, input voltage is  $V_{in}$ . On rearranging the values in (3), and the capacitor  $C_0$  value is obtained same as static gain of the converter.

$$V_{C6} = \frac{3V_{in}}{1-D} \tag{4}$$

The inductor  $L_2$  is zero at steady state condition,

$$(V_{C6} - V_{C1})D = (V_0 - V_{C6})(1-D) \tag{5}$$

From 1, capacitor 1 voltage is given by,

$$V_{C1} = V_0 - V_{C2} - V_{C3} - V_{C6} \tag{6}$$

By substituting the 3 & 4 in 5 the static gain is derived as,

$$\frac{V_0}{3V_{in}} = \frac{(1+D)}{(1-D)} \tag{7}$$

The duty cycle equation of the converter proposed is given as,

$$\frac{1-D}{1+D} = \frac{3V_{in}}{V_0} \tag{8}$$

The capacitor voltage in  $C_2, C_3$  are given as

$$V_{C2} = \frac{D \cdot 3V_{in}}{1-D} \tag{9}$$

$$V_s = \frac{3 \times V_{in}}{1-D} \tag{10}$$

The static gain of the proposed converter is compared with multilevel sepic converters in Figure 4 and from Figure 5, it is observed that the proposed converter attains required voltage gain with reduced duty cycle  $D=0.775$ . It's given that the switching voltage of the sepic converter is the sum of input and output voltage as of boost converter.

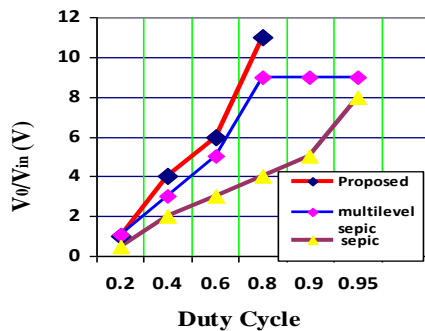


Figure 4. Voltage gain analysis

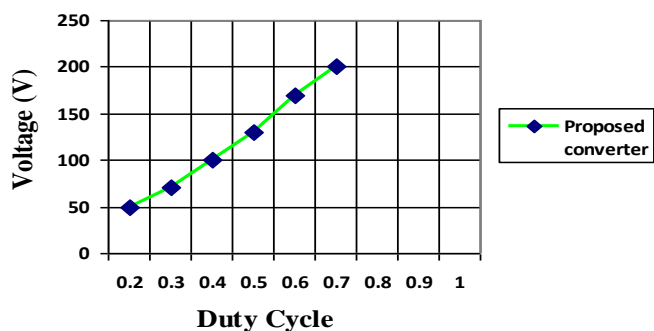


Figure 5. Switching voltage of proposed converter

### 3.2. Design Analysis of the Proposed Converter:

On the basis of the analytical expression of the converter operation, the component design values are selected.

#### 3.2.1 Duty Cycle Calculation:

The proposed converters step up and step down of voltage varies due to the duty cycle control. And also it is dependent on elements in the circuit. The output of the proposed converter is given as,

$$V_0 = \frac{D \times 3V_{in}}{1-D} \quad (11)$$

On taking the diode voltage drop in to account,

$$V_0 + V_d = \frac{D \times 3V_{in}}{1-D} \quad (12)$$

On simplifying,

$$D = 1 - \frac{nV_{in}}{V_0} \quad (13)$$

The attained duty cycle is 0.775.

#### 3.2.2 Inductor Selection and Capacitor Selection:

The inductance values are identified with the help of input current ripples. i.e.  $\Delta I_{L1}$  and  $\Delta I_{L2}$ . The values of the input current ripples are 5mA. Voltage ripple ( $\Delta v_c$ ) is used to calculate the capacitance value. The ripple value is obtained by the 10% of the input voltage value.

$$L_1 = \frac{D \times 3V_{in}}{f \times \Delta I_{L1}} \quad (14)$$

$$I_{ripple} = I_{out} \times \frac{V_{out}}{3V_{in}} \times 40\% \quad (15)$$

$$C_1 = C_2 = C_3 = \frac{I_0}{f \times \Delta V_C} \quad (16)$$

The ripple voltage is obtained by,

$$\Delta V_C = \frac{I_0}{C_0 f} \quad (17)$$

$$C_0 = \frac{P_0}{4\pi f_g V_0 \Delta V_0} \quad (18)$$

## 4. RESULTS AND ANALYSIS

In proposed converter output voltage ripple level is much small and the steady state is attained at earliest. The maximum over shoot is 0% and the transient response analysis is better than multilevel sepic converter. The output voltage is reliable and hence switching operation is good with reduced conduction loss and switching loss. The inductive voltage occurs only in positive value. From the Figure 13, the output voltage attained from proposed converter is less in ripple, the maximum over shoot is 0%, the settling time is 0.5ms and the steady state error is 0.6%. This output signifies that the converter operates in stable state. The parameter of the proposed converter is depicted in Table 2. Hence these converter well suits for PV applications and it boost up the PV voltage to the application level.

Table 2. Proposed Converter parameters

Components	Parameter
Input voltage	30 V
Output voltage	400 V
Input current	15.2 A
Output current	1 A
Inductor $L_1, L_2$	205, 180 $\mu$ H
Capacitor $C_1, C_2, C_4$	2.2 $\mu$ F
Capacitor $C_3$	2.2 $\mu$ F
Capacitor $C_0$	40 $\mu$ F
Resistor	400 $\Omega$

#### 4.1. Hardware Analysis

The experimental results obtained from the proposed converter are measured using Digital Signal Oscilloscope (DSO). The input voltage source of 30 V is obtained from regulated power supply. The dspac 1104 model controller is utilized to generate switching pulse for MOSFET switch. The duty cycle is generated by utilizing the switching frequency limit of 24 kHz. The real-time results obtained are exposed in Figure 6-13

In Figure 6 the output voltage is represented. From the analysis, it can be noted that the proposed converter is capable to produce an output voltage of 380 V from input of 30 V from the hardware which is approximately equal to simulation output voltage range. The output voltage waveform is represented in three ways such as peak time, turn on time and turn off time as shown in Figure 6 – Figure 9.

In Figure 13 the voltage across drain and source, switch voltage is depicted. The capacitor voltages are shown stage wise, and  $C_1$  and  $C_2$  levels are depicted in Figure 9-10. The values are 128 V, 125 V. Then the  $C_3$  and  $C_4$  voltages are depicted in Figure 10 the voltage ranges are 130 V, 127 V. The experiment reports attained are similar to the simulation results. The proposed converter exhibits better efficiency compared to conventional sepic. It also has less switching loss, conduction loss, ripple for various load condition.

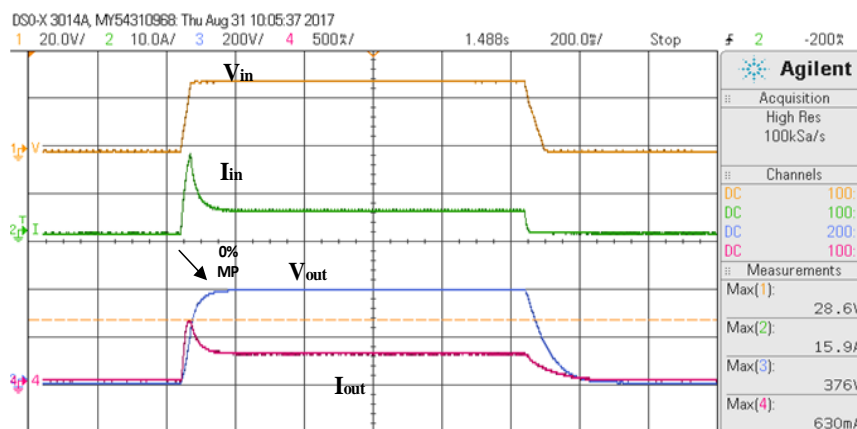


Figure 6. Complete response of the topology

Here in Figure 7, it's shown that when switch turns on, the voltage and current rises, capacitor charges. Simultaneously when switch turns off, the voltage, current lowers and capacitor starts discharging. The maximum peak overshoot is 0%. It's proved that same simulation results are same as hardware results, when the switch turns-off, the input voltage and current falls down. According to the switching operation the output varies

The duty cycle of the converter is 19.38% and it is verified from the above result. Also from the above result it is depicted that the attained efficiency of the proposed converter is 94%. Hence the efficiency is proved by both theoretical and hardware analysis. And also the ripple voltage and current are less compared to other converter and it is proven with hardware results.

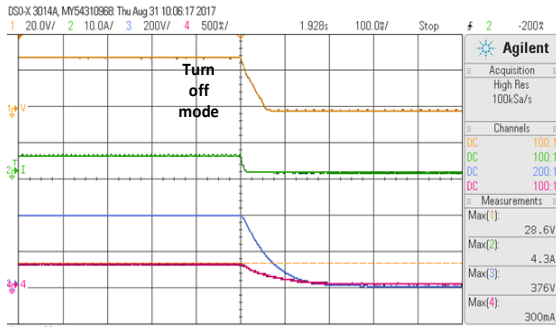


Figure 7. Turn off response of the system

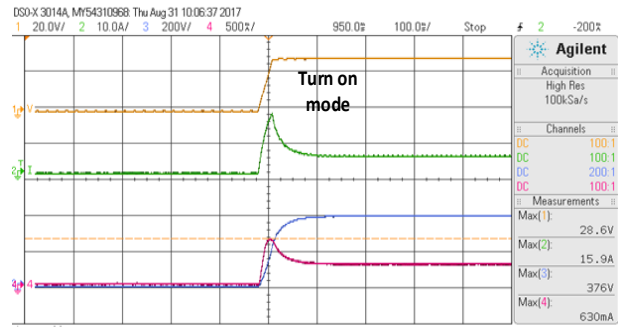


Figure 8. Turn On response of the system

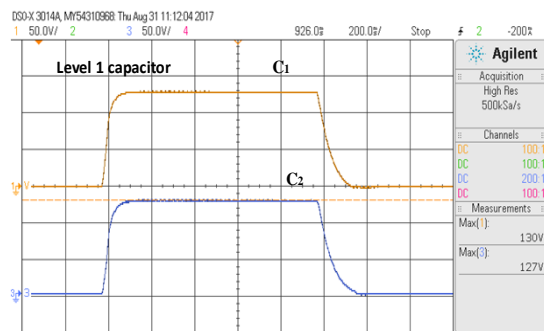


Figure 9. Stage 1 capacitor voltage

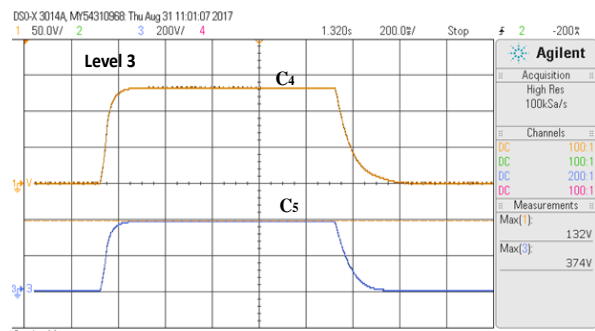


Figure 10. Stage 2 capacitor voltage

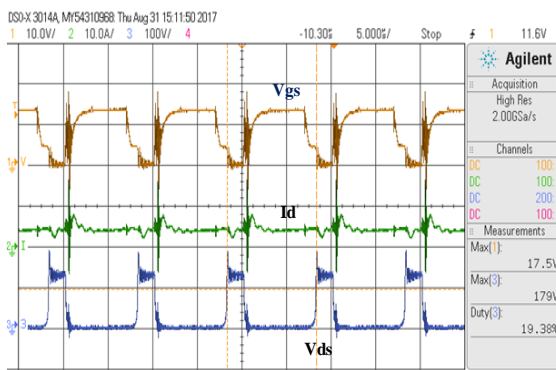


Figure 11. Gate response of the system

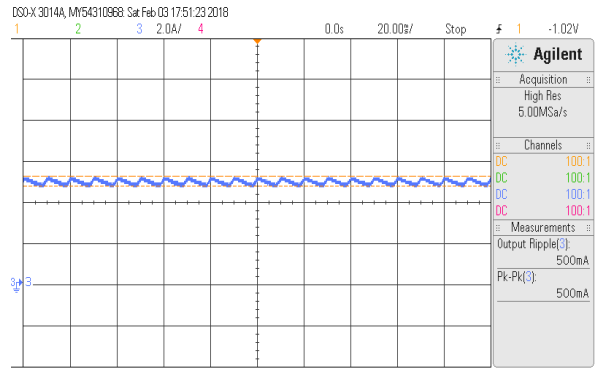


Figure 12. Ripple current waveform of the proposed converter

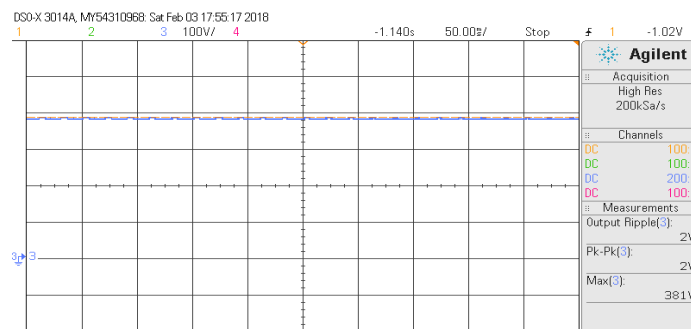


Figure 13. Ripple voltage waveform of the proposed converter

## 5. CONCLUSION

In this manuscript high step up voltage gain *modified* multilevel sepic converter has been proposed. The working and operation of the proposed converter in CCM mode is explained. The operation of the converter is detailed by the waveform depiction. The proposed model attains high static gain with reduce switching and conduction loss. The concept of VT has been embedded to improve the boosting of voltage ratio with efficiency. The steady state and design analysis has been explained. The simulation analysis of the proposed converter is presented clearly on comparing with multilevel sepic converter results. The transient response analysis of the proposed converter is explained. A prototype has been developed in laboratory and verified the working of converter. The experimental results prove that the proposed converter attains high stepping of voltage with tripling of voltage level with an efficiency of 94% with reduced switching stress.

## REFERENCES

- [1] Arunkumari, T. and Indragandhi, V., An overview of high voltage conversion ratio DC-DC converter configurations used in DC micro-grid architectures. *Renewable and Sustainable Energy Reviews*, Vol 77, pp.670-687 Sep 2017.
- [2] Farhat, M., Barambones, O. and Sbita, L., 2017. A new maximum power point method based on a sliding mode approach for solar energy harvesting. *Applied Energy*, Vol 185, pp.1185-1198, Jan 2017.
- [3] Abutbul, O., Gherlitz, A., Berkovich, Y. and Ioinovici, A., 2003. Step-up switching-mode converter with high voltage gain using a switched-capacitor circuit. *IEEE Transactions on circuits and systems I: Fundamental theory and applications*, Vol 50, no 8, pp.1098-1102, Aug 2007.
- [4] Rosas-Caro, J.C., Ramirez, J.M., Peng, F.Z. and Valderrabano, A., 2010. A DC-DC multilevel boost converter. *IET Power Electronics*, Vol 3 no.1, pp.129-137, Jan 2010.
- [5] Fardoun, A.A. and Ismail, E.H., 2010. Ultra step-up DC-DC converter with reduced switch stress. *IEEE transactions on industry applications*, vol 46 no 5, pp.2025-2034 Sep 2010.
- [6] Nouri, T., Babaei, E. and Hosseini, S.H., 2013. A generalized ultra step-up DC-DC converter for high voltage application with design considerations. *Electric Power Systems Research*, Vol 105, pp.71-84 Dec 13.
- [7] Nouri, T., Hosseini, S.H., Babaei, E. and Ebrahimi, J., 2014. Generalised transformerless ultra step-up DC-DC converter with reduced voltage stress on semiconductors. *IET Power Electronics*, Vol 7 no 11, pp.2791-2805, Aug 2014.
- [8] Zhu, M. and Luo, F.L., 2008. Series SEPIC implementing voltage-lift technique for DC-DC power conversion. *IET Power Electronics*, Vol 1 no1, pp.109-121, Mar 2008.
- [9] Young, C.M., Chen, M.H., Chang, T.A., Ko, C.C. and Jen, K.K., 2013. Cascade Cockcroft-Walton voltage multiplier applied to transformerless high step-up DC-DC converter. *IEEE transactions on industrial electronics*, Vol 60 no2, pp.523-537, Feb 2017.
- [10] Sabzali, A.J., Ismail, E.H. and Behbehani, H.M., High voltage step-up integrated double Boost-Sepic DC-DC converter for fuel-cell and photovoltaic applications. *Renewable Energy*, Vol 82, pp.44-53, Oct 2015.
- [11] Williams, B.W., 2014. Unified synthesis of tapped-inductor dc-to-dc converters. *IEEE Transactions on Power Electronics*, Vol 29 no 10, pp.5370-5383, Oct 2014.
- [12] Vazquez, N., Estrada, L., Hernandez, C. and Rodriguez, E., The tapped-inductor boost converter. In *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on* pp. 538-543. IEEE, June 2007.
- [13] Zhao, Q. and Lee, F.C., 2003, February. High performance coupled-inductor DC-DC converters. In *Proc. IEEE APEC* Vol. 1, pp. 109-113.
- [14] Berkovich, Y. and Axelrod, B., Switched-coupled inductor cell for DC-DC converters with very large conversion ratio. *IET power electronics*, vol 4 no 3, pp.309-315 Oct 2014.
- [15] Wu, T.F., Lai, Y.S., Hung, J.C. and Chen, Y.M., 2008. Boost converter with coupled inductors and buck-boost type of active clamp. *IEEE Transactions on Industrial Electronics*, Vol 55no 1, pp.154-162, Jan 2008.
- [16] Zhao, Y., Li, W. and He, X., 2012. Single-phase improved active clamp coupled-inductor-based converter with extended voltage doubler cell. *IEEE transactions on power electronics*, Vol 27 no 6, pp.2869-2878 Jun 2012.
- [17] Ajami, A., Ardi, H. and Farakhor, A., 2015. A novel high step-up DC/DC converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications. *IEEE Transactions on Power Electronics*, Vol 30 no 8, pp.4255-4263 Aug 2015.
- [18] Tang, Y., Fu, D., Kan, J. and Wang, T., 2016. Dual switches DC/DC converter with three-winding-coupled inductor and charge pump. *IEEE Transactions on Power Electronics*, Vol 31 no 1, pp.461-469, Jan 2016.
- [19] Lai, C.M., Pan, C.T. and Cheng, M.C., 2012. High-efficiency modular high step-up interleaved boost converter for DC-microgrid applications. *IEEE Transactions on Industry Applications*, Vol 48 no 1, pp.161-171 Jan 2012.
- [20] Tseng, K.C., Huang, C.C. and Shih, W.Y., 2013. A high step-up converter with a voltage multiplier module for a photovoltaic system. *IEEE transactions on power electronics*, Vol 28 no 6, pp.3047-3057 June 2013.
- [21] Saravanan, S. and Babu, N.R., 2017. Analysis and implementation of high step-up DC-DC converter for PV based grid application. *Applied Energy*, Vol.190, pp.64-72. Mar 2017.
- [22] Ajami, A., Ardi, H. and Farakhor, A., 2015. A novel high step-up DC/DC converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications. *IEEE Transactions on Power Electronics*, Vol 30 no 8, pp.4255-4263 Aug 2015.



- [23] Hu, X. and Gong, C., 2014. A high voltage gain DC–DC converter integrating coupled-inductor and diode–capacitor techniques. *IEEE transactions on power electronics*, Vol 29 no 2, pp.789-800, Feb 2014.
- [24] Siwakoti, Y.P., Blaabjerg, F. and Loh, P.C., 2016. High Step-Up Trans-Inverse (Tx– 1) DC–DC Converter for the Distributed Generation System. *IEEE Transactions on Industrial Electronics*, Vol 63 no 7, pp.4278-4291, Jul 2016.
- [25] Logesh, R., 2017. Resources, configurations, and soft computing techniques for power management and control of PV/wind hybrid system. *Renewable and Sustainable Energy Reviews*, Vol 69, pp.129-143, Mar 2017.
- [26] Gandhi, v., Subramaniaswamy, v. and Logesh, r., 2017. Topological review and analysis of dc-dc boost converters. *Journal of Engineering Science and Technology*, Vol 12 no 6, pp.1541-1567, Jun 2017.