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Performance Enhancement of Bidirectional Noc Router with and without Contention for Reconfigurable Coarse Grained Architecture

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ABSTRACT

Network on Chip (NoC) router plays a vital role in System on Chip (SoC) applications. Routing operation is difficult to perform inside the SoC chip. Because it contains millions of chips in one single Integrated Circuit (IC), in which every chip consists of millions of transistors. Hence NoC router is designed to enable efficient routing operation in the SoC board. NoC router consists of Network Interconnects (NI), Crossbar Switches, arbiters, a routing logic and buffers. Conventional unidirectional router is designed by priority based Round Robin Arbiter (RRA). It produces more delay to find the priority, which comes from various input channels and more area is consumed in unidirectional router. Also if any path failure occurs, it cannot route the data through other output channel. To overcome this problem, a novel bidirectional NoC router with and without contention is proposed, which offers less area and high speed than the existing unidirectional router. A novel bidirectional NoC router consists of round robin arbiter, Static RAM, switch allocator, virtual channel allocator and crossbar switch. The proposed bidirectional router can route the data from any input channel to each and every output channel. So it avoids conflict situation and path failure problems. If any path fails, immediately it will take the alternative path through the switch allocator. The proposed routing scheme is applied into the coarse grained architecture for improving the speed of the interconnection link between two processing elements. Simulation is performed by ModelSim6.3c and synthesis is carried out by Xilinx10.1.

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1. INTRODUCTION

System on a chip (SoC) is the design methodology currently used by VLSI designers, based on extensive IP core reprocess. Cores do not make up System on Chips alone; they have to include an interconnection architecture and interfaces to peripheral devices. Usually, [1] the interconnection architecture is based on dedicated wires or shared busses. Dedicated wires are effective only for systems with a small number of cores, since the number of wires in the system increases dramatically as the number of cores grows. Therefore, dedicated wires have poor reusability and flexibility. A shared bus is a set of wires common to several cores. This scheme is reusable and more scalable, when compared to devoted wires. On the other hand, busses authorize only one communication transaction at a time. Thus, all cores share the same communication bandwidth in the system and scalability is limited to a few dozen IP cores [2]. Using separate busses interconnected by bridges or hierarchical bus architectures may reduce some of these constraints, since different busses may account for protocols, different bandwidth needs and also expand communication

parallelism. Nonetheless, scalability remains a problem for hierarchical bus architectures. A network on chip (NoC) appears as a probably better solution to implement future on-chip interconnection architectures. In the most commonly found organization, a NoC is a collection of interconnected switches. These switches have the IP core connected to them. NoCs present better bandwidth, scalability and performance than shared busses.

2. BACKGROUND

Routers are responsible for: (i) receiving incoming packets; (ii) storing packets; (iii) routing these packets to a given output port; (iv) sending packets to others switches. To achieve these tasks, four most important components compose a crossbar switch [3]: a router, to describe a way between input and output channel (function i); buffers are temporary storage devices to store the intermediate data (function ii); an arbiter to grant access to a given port when multiple input requests arrive in parallel (function iii); and a flow control module to regulate the data transfer to the next switch (function iv). The architecture and dataflow control will change the design of NoC arbiter considerably. The arbitration should assured the fairness in avoid starvation, scheduling and offer high speed. The NoC's switches should offer high throughput and cost-effective contention resolution technique when several packets from different input channels vie for the same output channel. A fast arbiter is one of the most dominant factors for high speed NoC switches [4]. For the exceeding reasons, the analyses of the speed of the arbiters are considerably meaningfulness in the design of NoC (Network-on- chips). Efficient FPGA Based Bidirectional Network on Chip Router through Virtual Channel Regulator proposed [5] and then bi-directional NoC router provides low power and area utilization.

The NoC router is a heart of the on chip network, which undertakes critical assignment of coordinating the data flow. The network router operation revolves approximately two fundamental rules: (a) the associated control logic and (b) the data path. The data path contains number of input and output channels to make easy packet switching and traversal [6]. Usually 5 X 5 input and output routers are used in NoC router. Out of five ports four ports are in cardinal direction (North, South, East, West) and one port is connected to its local (PE) Processing Element Like in any other network, router is the vital component for the design of message back-bone of a NoC router [7]. In a packet switched network router, the working principle of the router is to transmit an incoming packet to the destination port if it is directly connected to it, or to transmit the packet to another router connected to it. It is significant that design of a NoC router should be as simple as possible because implementation cost increases with an increase in the design complexity of a router. The design of router mainly consists of five parts: 1. Buffer, 2. Arbiter, 3. Crossbar, 4. Routing Logic and 5. Channel Control Logic. In this paper, we have design bidirectional router with and without contention situation by introducing virtual channel allocator, switch allocator and Round robin arbitration schemes. Organization of this paper is given below: Introduction about System on Chip (SoC) and Network on Chip (NoC) are presented in section 1. Design of unidirectional router is performed in section 2. The Proposed bidirectional router is designed in section 3. Results of unidirectional and bidirectional routers are compared and discussed in section4. Conclusion of this research work is presented in section 5.

3. CONVENTIONAL UNIDIRECTIONAL ROUTER

Unidirectional router is used to perform the routing operation in single direction. Main drawbacks of this routing logic are path fails occur, dead lock and live lock problem. The 5X5 Round Robin Arbiter consists of number of OR gates, AND gates and D flip-flops. Conventional unidirectional router structure is shown in Figure 1, which consists of Round Robin Arbiter, First in First out (FIFO) buffers and crossbar switches. Arbiter is used to grant the data based on the priority [8]. Higher Priority data will be routed first. A FIFO buffer is used to store the data few times. It’s look like temporary storage device. These FIFO buffers are used in both input and output channel sides. Crossbar switches is used to transfer the data, which comes from the arbiter. Channel control logic is incorporated in this router to send the control signal to crossbar switches. For example, input channel A can route the data through corresponding output channel A only, and cannot route the data via output channel B. Hence it is called unidirectional router.

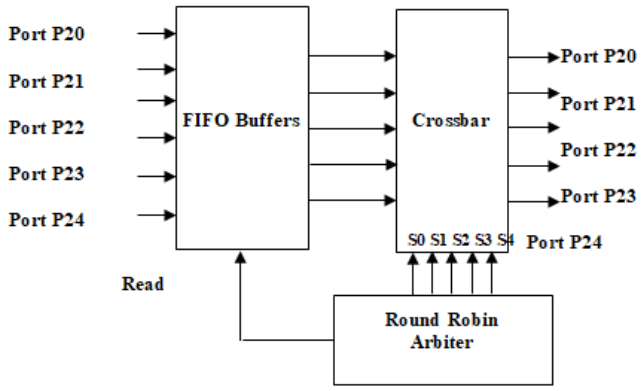

Figure 1. Block diagram of conventional unidirectional router

4. PROPOSED BIDIRECTIONAL NOC ROUTER

Network on Chip (NoC) router plays an important role in the system on chip (SoC) based applications. Normally routing operation is not easy to perform inside the Soc Chip. Soc contains millions of chip within single integrated circuits; each integrated circuit contains millions of transistor. Routing operation is important the SoC architecture, because the information transferred through routing logic [9]. So need to design an efficient routing logic functions. NoC router consists of the following components, Network Interconnects (NI), crossbar switches, arbiters, buffer and routing logic. Unidirectional router and bidirectional router are the two types of router mostly used in the NoC architecture. In the unidirectional router operates in a single direction. It does not communicate on both sides; information travels to only one direction. Drawbacks of this routing logic are path failure, dead lock problem and live lock problem. The main aim of the routing logic creates the path between the source and the destinations. Routing logic prevents the deadlock, live lock and starvation problem. Deadlock is defined as the cyclic dependency among nodes requiring access to the collection of sources [10]. Live lock is the process of circulating the packets to the network without ever making any progress towards their destinations. Starvation problem is occurred for the packet requesting the buffer when the output channel is allocated to another packet [11]. Routing algorithm can be classified into three criteria, a) where the routing decisions are taken, b) how the path defined, c) path length. The unidirectional router includes Round Robin arbiter, First in First out (FIFO) buffers and crossbar switches. Arbiter is used to access the data based on the priority. Higher priority data will be routed first in the architecture. A buffer is a temporary storage device. FIFO buffer is used to store the packet or data temporally. Both the input and output channels use the buffer. Data is transferred by using crossbar switches. Crossbar switches receive the control signal from the router with channel control logic.

A contention is one of the issues being done in the routing logic. A contention is nothing but competition for resources when two or more nodes are trying to transmit a message in the same channel at the same time [12]. To avoid the contention situation by introducing the bidirectional network on chip router. The proposed bidirectional router consists of In Out port, static RAM, Round Robin Arbiter, Routing logic and channel control module. Arbiter chooses one output from the number of inputs based on the logic used. Arbiter present in the crossbar switch contains the same number of input and output. Data, request and destination are the three quantities come from the crossbar input. The input data will be routed at the output side, the output port address present in the destination. If two or more data send the request at the same time from the crossbar input, the round robin arbiter allows only one request at the time. This may cause the data losses, to avoid the data loss by using FIFO buffer and SRAM memory. The stored data in the memory transfer into the next clock cycle [13]. This process is called as contention free crossbar. Figure 2 shows that the block diagrams of Bi-directional NoC router.

Static RAM and Dynamic RAM are the two type of memory element used in the routing logic. DRAM consists of transistor and capacitor, and it needs periodical revive to carry on the leak power of capacitor. SRAM contain more transistors, so it consumes more area, but it reduces the leakage power by increasing the number of the transistor to increase the reading capability. It provides high speed of operation when compared to the DRAM. The proposed bidirectional router is designed using the SRAM memory to speed up the router and avoid the unwanted leakage power. Virtual channel allocator and Source allocator is used to controlling the channels.Virtual channel allocator is used to virtually change the corresponding channel direction. Switch allocator is used to removing the path failures. Three methods are used to transfer the data in the bidirectional NoC router these are, all input and output channel act as master or slave. The

second one is data from the input channel routes the data through same output channel; it eliminates the path failure. Third, all input data transfers through all the output port. It will remove the live lock and dead lock problems. The proposed bidirectional NoC router provides less area and high frequency than the conventional unidirectional router. The area and delay are reduced by introducing the efficient routing logic in the proposed bidirectional router.

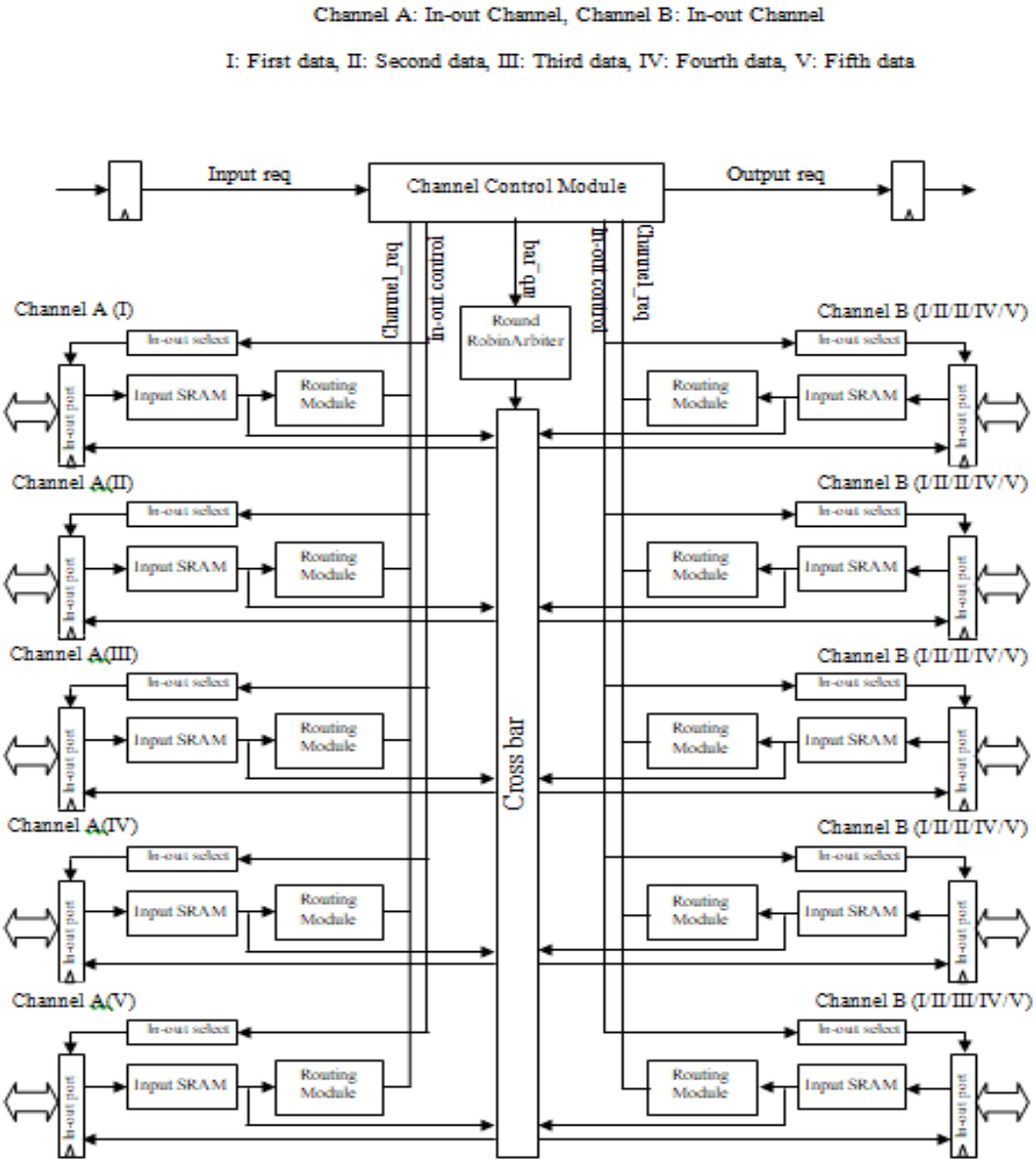

Figure 2. Architecture of Bi-directional NoC Router

5. RESULTS AND DISCUSSION

The design of bidirectional NoC router with and without contention is a main goal of this research work. The proposed router is designed using Verilog HDL. Performance investigation is processed between unidirectional and bidirectional NoC router. Simulation process is done by ModelSim6.3c. Synthesis process is checked by Xilinx10.1. Contention free bidirectional NoC router is designed using Static Random Access Memory (SRAM) to store the data upto next clock cycles. So high speed and low leakage power are used in Static RAM. Crossbar switches with Round Robin Arbitration scheme is used to eliminate the path failures occur. Simulation result of conventional unidirectional NoC router is shown in Figure 3.

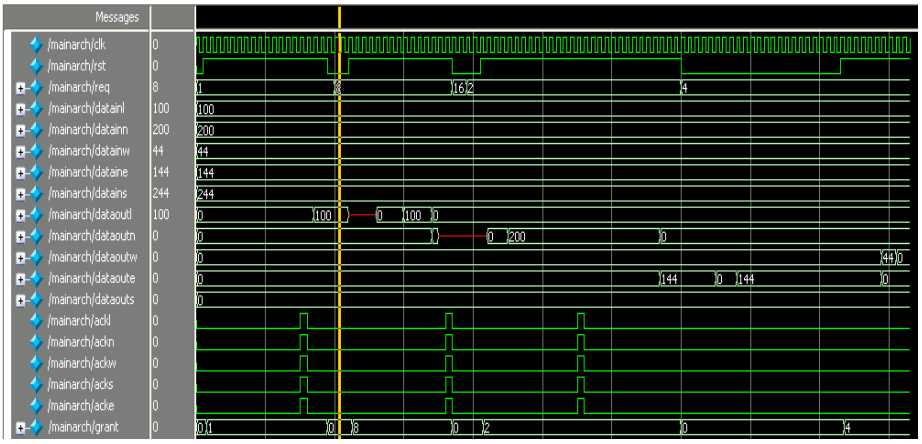

Figure 3. Simulation result of unidirectional NoC router

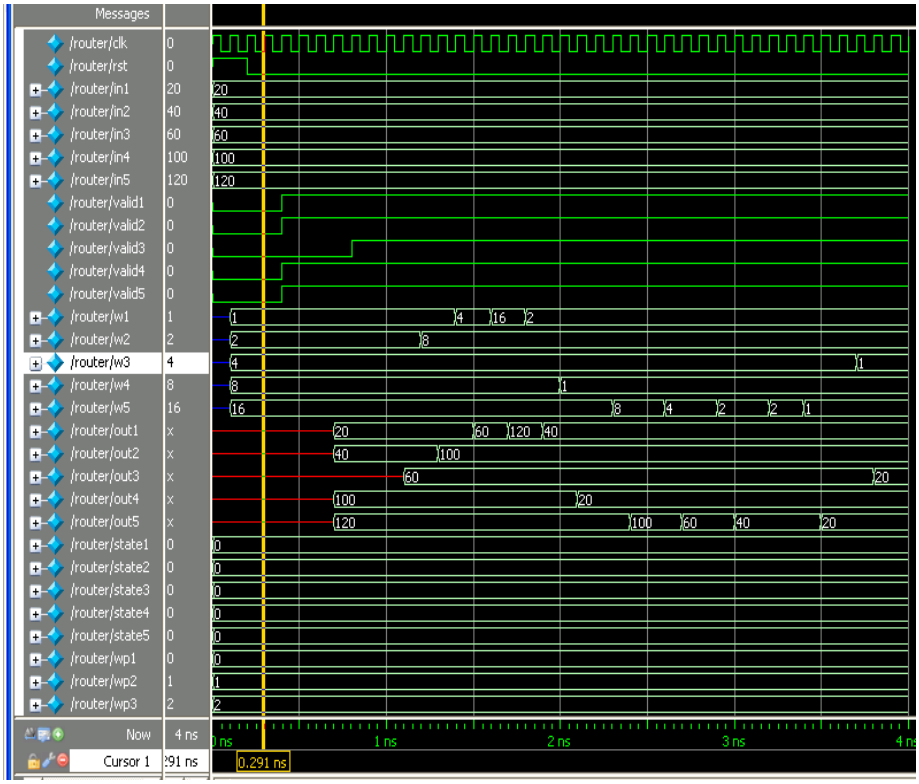

Figure 4. Simulation result of proposed bidirectional NoC router

The proposed bidirectional NoC router is designed and verified through simulation process. Simulation result of bidirectional NoC router is shown in Figure 4. Active high reset is used in the router i.e. whenever the reset is high, all the output were zeros. All the outputs are generated, when the reset is low. The information or data in the input channel1 is 20, input channel2 is 40, input channel3 id 60, input channel4 is 100 and input channel5 is 120. The valid data signal goes high, when the valid information comes from input channel. From the table 1 the analysis results of conventional and bidirectional routing are clearly shown. Delay of the bidirectional routing is reduced when compared to the conventional unidirectional routing. Also device utilization of the bidirectional routing is getting reduced. Figure 5 shows that the Comparison graph of Conventional and Bidirectional Routing Technique.

Table 1. Comparison Between Conventional and Bidirectional Routing

Parameters Noticed	Conventional Routing	Bidirectional Routing	% reduction
Number of Slices Flip-flop	1579	1269	19%
Number of 4-input LUTs	1050	868	17%
Number of Occupied Slices	1204	981	18%
Minimum Time period (ns)	13.684ns	8.501ns	37%
Maximum frequency (MHz)	73.076MHz	117.636MHz	~

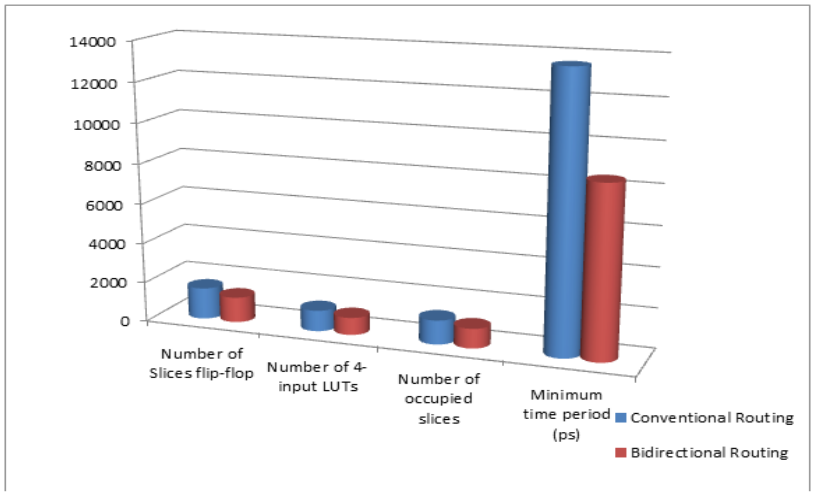

Figure 5. Comparison graph of Conventional and Bidirectional Routing Technique

5. CONCLUSION

In this work, an area efficient and high speed bidirectional NoC router with and without contention is proposed. This proposed bidirectional NoC router is compared with the conventional unidirectional router. The simulation result shows that the proposed bidirectional NoC router occupies smaller chip size and utilizes lesser delay than the conventional unidirectional NoC router. The designed router is suitable for coarse grained architecture. Delay of the coarse grained architecture can be reduced by bi-directional routing method. It effectively reduced the delay occurring in the architecture. It offers 37% of delay reduced when compared to the conventional routing method. Also it provides 17% reduction in LUT counts and 18% reduction in slices used in the architecture. In future, the proposed NoC router is used in System on Chip applications for efficient on chip routing process.

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