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Design of "32" Point Split Radix based Multipath Delay Commutator FFT Architecture for Low Power Applications

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ABSTRACT

FFT is used in Modern high speed signal processing application. In aforementioned technologies that tends to operate in various operational modes. To implement FFT obviously it not only needs to meet high throughput demand and also it needed to scalable cater selectable N point FFT. Our contribution to this paper is two-fold of our existing method, as proposes for the split radix using Multipath Delay Commutator (MDC) algorithm has the least complex design and less multiplications comparing to radix-2 algorithm. So that it can able to reduce power consumption and area than our existing work. The implementation of power efficient hardware of split radix FFT (SRFFT) is built up by pruning excessive computation. Leveraging this potential, a new architecture of a configurable SRFFT processor is first developed so that unnecessary computations, which yield zeros at the output, are pruned. Simulations show that maximum power saving of around 20% is achieved. The proposed algorithm consists of mixed radix butterflies, whose structure is more regular. It has the conjugate-pair version, which requires less memory.

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1. INTRODUCTION

FFT with split radix method was initially described by Duhamel and Hollman in the year of 1948.The SRFFT algorithm is also called as FFT algorithm. It uses two radix in single butterfly operations, even terms for radix-2 and odd terms for radix-4 structure, which computes in the butterfly structure with the shape of "L" .Radix-8 Cooley–Turkey (CT) algorithm's efficiency, can be obtained by this algorithm. It can be designed by the combination of radix-2 and radix-4 [1]. This can be achieved by Radix-4 CT FFT's complexity and the Radix-2 CT FFT's flexibility. By combining radix-2 algorithm the cost for computing is minimized in the split radix FFT architecture.

In pipelined architecture, the both SDF architecture and MDC architecture furnishes the same throughput with the low memory and less complex multipliers and adders. Although, multipath Commutator architecture can yield N times throughput of single feedback architecture only at the high Memories, high number of complex multipliers and adders. The FFT with split radix structure has the advantages of which a multiplier /accumulator is the basic processor, but has the disadvantage of SRFFT butterfly computational unit as the basic processor. Pipelined hardware is much hard to realize for the SR algorithm than CT algorithm because the computational load varies between the various stages. The SRFFT algorithm using MDC of VLSI implementation is proposed for the radix 4-FFT and radix 2-FFT because it has less computations in pipelined architecture with multiple path delay commutators. It has good throughput

obtained from its raised parallelism and also has the elasticity of providing the SRFFT of sequence that have the power of two, also by using four, for the R4-FFT.The cost that needs to implement SRFFT has increase due to the high parallelism but it balances the computational power and flexibility also added for the proposed FFT architecture [2].The FFT algorithm with split radix and radix-2 FFT algorithm are almost same with the exception of its location and twiddle factors values. The computational complexity of the FFT can be reduced by using pipelined 32-point split-radix multi-path delay commutator (SRMDC) FFT architecture. It reduces the slices and LUT counts for reducing the area occupying of the FFT processor. The proposed architecture is mainly to improve an efficiency of the FFT processor

2. BACKGROUND

In explained an extensive FFT algorithm with split radix structure. The extended FFT algorithm and the traditional FFT algorithm with split radix structure has the same asymptotic arithmetic difficulty. FFTs are operated on that the need registers to compute a split-radix FFT algorithm; FFTs will use few loads and stores on the radix-4 FFT algorithm. The no of load, store, arithmetic operations used for R2, R4, and R8 and extended split-radix using 4- multiply 2–add schemes.

In described that the implementation of split radix FFT. They are compared with the SRFFT algorithm for power of two (i.e.,) x^2 transform to the Cooley-Turkey (CT) FFT algorithm. The SR FFT requires few complex multiplications than the CT algorithms of radix two, four and eight. It requires about 20-50% more butterfly operations than the radix four CT FFT [3]. Subsequently, the utilities of SRFFT algorithm for depend on multiply or accumulate the rate of throughput. The techniques that are used to construct SRFFT pipelined implementation are simple.

In explained parallel MDCFFT processor with efficient scheduling. The proposed work FFT processor can attain by using parallel data-path design with high throughput MDC structure. This scheme reduces the no of complex multipliers from eight to six with no rising of delay buffers. It can also offer a lower hardware computational complexity with 100 percent utilization of hardware [4]. The FFT processor can be utiilized in OFDM essential with the lower complexity and higher complexity.

In proceeded that the flexible MDC-based FFT architecture and are used for higher performance generator applications [5]. The proposed work was done easy and flexible that is to satisfy throughput rate. In proposed work, automatically generate the particular HDL code by hardware generator and hardware generator is also developed so that the time and cost can be extremely reduced. MDC-based architectures first divide the input sequence into two parallel data streams by properly-controlled switches/FIFOs and direct them to the correct butterfly units MDC-based architecture demands a little bit resources and with high throughput but larger throughput [6].

3. MIXED R2SDF-R4SDC

There are four types of pipelined FFT architecture are single delay feedback (SDF), singlepath delay commutator (SDC), Multipath delay feedback(MDF), Multipath delay commutator(MDC). It can be classified as Multipath or single path by their no. of input data stream paths [7]. Mixed R2SDF-R4SDC pipelined FFT architecture gives the $\log_2$ (N-1) SDC stage with one SDF stage. The R2SDF-R4SDC work done for the 100% efficient utilization of hardware resources in multiplexed time approach by sharing the same resource of arithmetic operations that considers of adders and also multipliers. It reduces the requirement of complex multipliers while comparing with other radix FFT architectures [8]. It also requires complex adders and complex delay. Figure represents the DIF Dataflow graph the combined SDC-SDF FFT Pipelined structure which has the output in sequential flow[9]. It reduces complex multiplier of 50% while comparing with the other radix FFT architecture.

4. PROPOSED SPLIT RADIX USING MDC ARCHITECTURE

Fast computation of the discrete Fourier transform (DFT) is called as fast Fourier transform. Algorithm of Multipath delay split radix FFT (SRFFT) algorithm for sequential data that having a power integer length of 2($N = 2^m$) is based on radix-2 application for coefficients computation of even terms of the transform and radix-4 applications for computing the odd terms coefficient of the transform. SR-DIF FFT algorithm is obtained by applying equally in R-2 and R-4 FFT algorithm to clear the problem [10].

By changing the exponents of twiddle factor, it can be obtained by converting straight forwardly into radix 4 FFT algorithm. The SR algorithm is based on the following decomposition:

$$Y_k = \sum_{n=0}^{N-1} y_n W^{nk}$$

$$Y_k = \sum_{n=0}^{\frac{N}{2}-1} (y_n + y_n + \frac{N}{2}) W_N^{2nk}\, k = 0,1, \ldots . \frac{N}{2} - 1$$

$$Y_{4k+1} = \sum_{n=0}^{\frac{N}{4}-1} [(y_n - y_n + \frac{N}{2}) - j(y_n + \frac{N}{4} - y_n + 3\frac{N}{4})] W_N^n W_N^{4nk}$$

$$Y_{4k+3} = \sum_{n=0}^{\frac{N}{4}-1} [\left(y_n - y_n + \frac{N}{2}\right) + j(\, y_n + \frac{N}{4} - y_n + 3\frac{N}{4})] W_N^{3n} W_N^{4nk}\, k = 0,1, \ldots . , N/4 - 1$$

To calculate FFT using the method of Split radix using radix-2 and radix-4, it can be computed that even no points and the odd no points and that can be resulted independently. This reduces the complexity of arithmetic computational processing complexity in the opportunity of using various computational schemes for various parts of the algorithm [11]. Splitting by combining two radix that is the radix-2 and radix-4 and why are proceeding for the split radix is because radix-2 is best mean for simplicity and radix-4 is for less computational complexity, resulting in less arithmetic calculation stages [12]. Split radix FFT algorithm represents the DIF length N, length N/2 represents one small DFT and length N/4 represents two small DFTs. In Figure 1 shows the split radix algorithm FFT flow graph and the butterfly structure of 32-point split radix FFT using MDC shown in Figure 2.

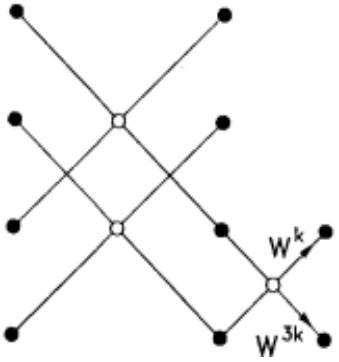

Figure 1. Structure of Split Radix algorithm

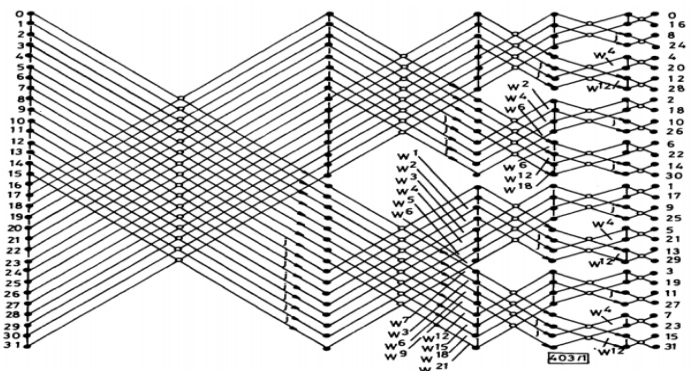

Figure 2. 32-point Split Radix FFT Butterfly Structure

5. PROPOSED MULTIPATH DELAY COMMUTATOR (MDC) WITH SPLIT RADIX FFT

In this paper, the proposed work gives the architecture of 32 point split radix multipath delay Commutator is established to decrease the area utilization and power utilization of the processors. In the conventional method, mixed architecture of radix-2, radix-4 and radix-8 is design is used to decrease the power and area consumption. In the proposed split radix FFT architecture using MDC was designed. The designed architecture is compared with the conventional architecture; the proposed FFT structure has great increase in the speed and throughput of the processor and also drastically decreases the power, occupied slices, and LUT counts.

Compared with the existing method, proposed work gives the better performance. Split radix FFT is evaluated completely in MDC. Figure 3 represents the 32-point split-radix Multipath delay commutator pipelined architecture. Figure 3 show the proposed method contains processing elements, commutators, twiddle factors, multiplexers, delay buffers. Converting from one signal form to another signal form is the main process of commutator. By using processing elements, that is used for the complex value addition and

subtraction. Among four input data samples one sample is selected at each clock cycles, Multiplexers are used [13]. Twiddle factors are to be implemented efficiently using signed digit approach. In this architecture, FFT processor performance can be improved by using multiple numbers of delays. Split radix based FFT algorithm needs only both smaller number of multiplies and joint multiplies and adds than radix-4 and radix-2 algorithm. An arithmetic operation in the split radix based MDC architecture is reduced. High throughput can be achieved by using pipelined method and MDC structure. Reduced complexity radix-4 FFT is used in 32-point split radix FFT with multiple path delay.

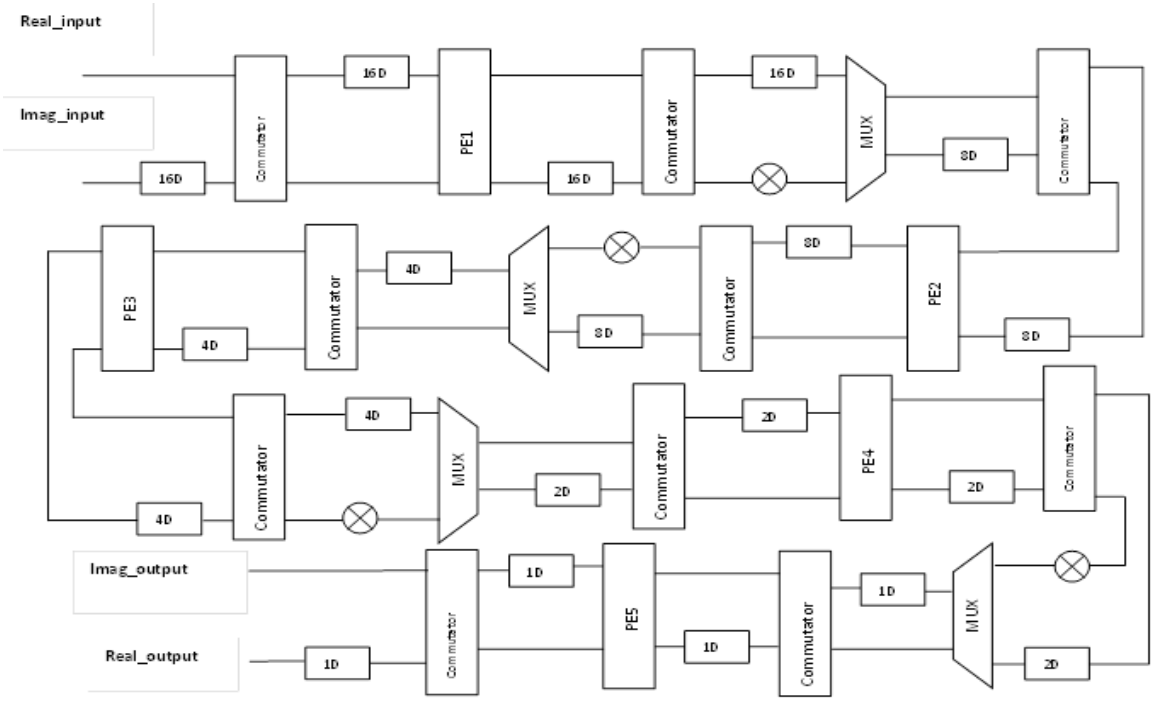

Figure 3. 32-point split-radix multi-path delay commutator (SRMDC) pipelined FFT architecture

6. RESULTS AND DISCUSSION

The proposed split radix FFT using the multipath delay commutator by using Verilog HDL. The proposed architecture has the advantage of having only few arithmetic operations compared to the existing method. Split-radix also have some advantages that is it has a clear cut structure, except the output signals it has no reordering of input signals, etc. The simulation results have been processed by using ModelSim XE simulator and those results are evaluated using Xilinx ISE 10.1 processing tool. Power, Area has been reduced and performance of proposed one has been utilized efficiently. Figure 4 shows the simulation result of the proposed FFT structure. Table.1 shows the Existing and proposed method performance.

Table 1. Comparison between Existing and Proposed Method

Parameters Noticed	Existing FFT Architecture	Proposed FFT Architecture	% reduced
Number of LUTs	13602	10143	25.1%
Number of flip flops	1761	931	47.13%
Number of slice Registers	2476	1711	30.89%
Power(mW)	5.248	2.958	43.63%
Delay (ns)	19.470ns	25.188ns	~

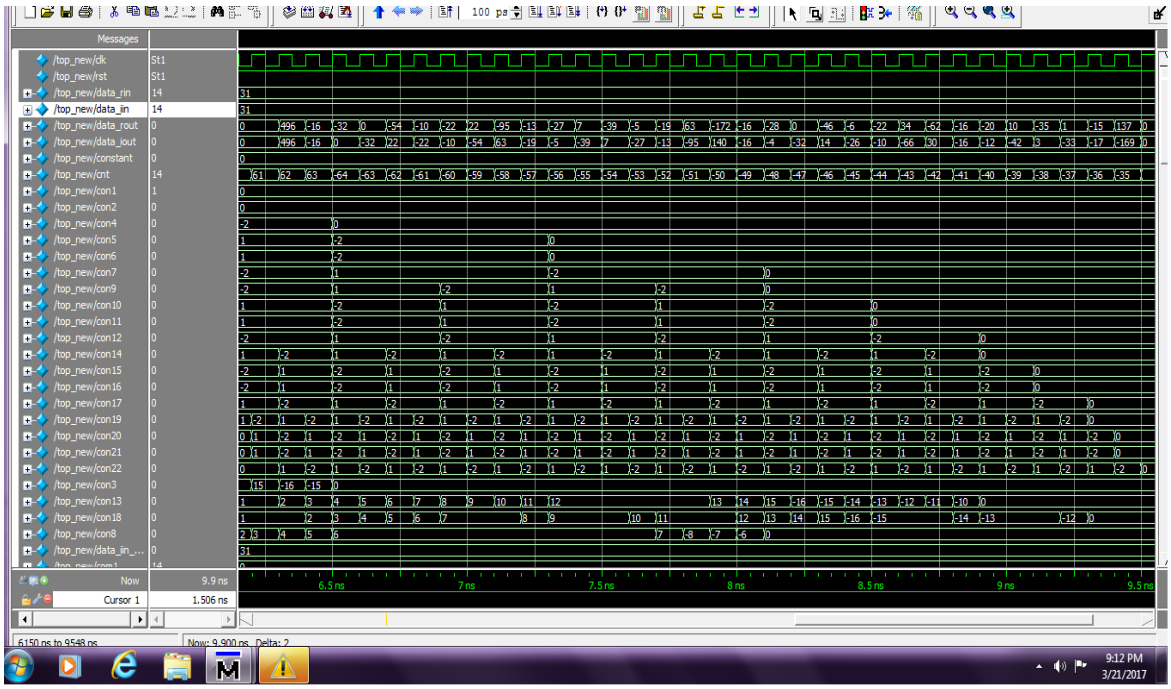

Figure 4. Result based on 32-point split-radix MDC FFT

The proposed FFT architectural design offers 17.72% reduction of area and gives the power reduction of 43.63% reduction. The proposed work offers the better performance and utilizes it efficiently compared to the existing 32-point mixed R2, R4, R8 FFT. Performance comparison graph between the existing method and proposed method for different parameters are shown in the Figure 5.

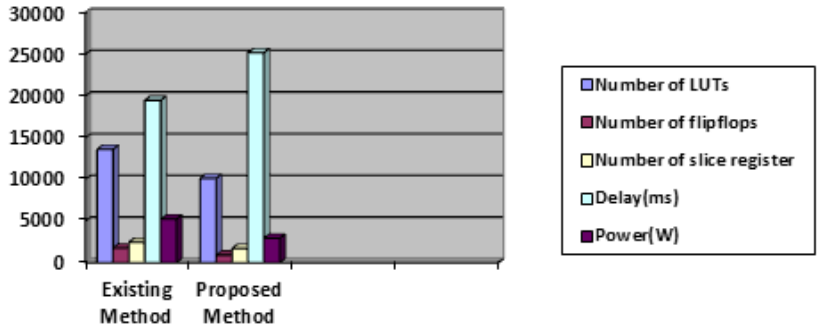

Figure 5. Performance comparison between the existing and proposed method

7. CONCLUSION

The split radix based FFT architecture was designed in VLSI using verilogHDL language. The Multipath delay commutator (MDC) architecture using split radix technique is used for reducing the slices counts occupied by the chip, LUTs counts and higher consumption of power. The proposed structure offers 25.1% reduction in LUTs count, 47.13% reduction in flip-flops usage and 30.89% reduction in slices utilization and 43.63% power reduction. The proposed split radix based MDC structure will be extended to 64-point, 128-point, and 256-point split radix based MDC architecture. For 128-point split radix FFT can be computed by using radix-8 and radix-16 for future development of FFT.

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