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Modeling and Simulation of Nine-Level Cascaded H-Bridge Multilevel Inverter

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ABSTRACT

This paper analyzed a single phase nine level cascaded h-bridge multilevel inverter (CHMLI) topology in which requires lesser number of components and easier to control if compared to other methods. The inverter of different voltage levels (up to 9-Levels) are designed and simulated using MATLAB Simulink. A Level Shifted Multi-Carrier PWM control scheme is used to control the operation of the power switches for CHMLI topology. The results are compared in terms of THD. The value of THD is found to be reduced as the number of voltage level of CHMLI is increased.

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1. INTRODUCTION

Conventional inverter has been used since the past decades in the field of industrial applications and power systems of lower power usage. Problems appeared when it comes to high power and medium voltages usage. Conventional inverters are found that it is no longer fulfill the requirement of voltage usage due to the incapable of reducing harmonic contents. It has high switching losses, lower efficiency and the lifespan of the systems due to long term constraining. This lead to the growth of Multilevel Inverter (MLI), the creation of multiple DC levels that combined into sinusoidal wave which reduces harmonic distortion. MLI topologies are introduced to be functioning under high frequency with lesser switching losses and higher efficiency [1]. Therefore, a 9-level multilevel inverter is designed and simulated to produces a lower THD content.

2. METHODOLOGY

The Cascaded H-Bridge topology is employed in this simulation. Cascaded H-Bridge is constructed with 5 switches (MOSFETs). Each of the H-Bridge represents an increment of 2 levels of the inverter. Therefore, Table I shows the number of H-Bridges in an inverter of different numbers of voltage levels.

Table 1. No. of H-Bridges for Different Levels of MLI

Voltage Level(s)	No. of H-Bridges
3	1
5	2
7	3
9	4

Figure 1 illustrates the connection of 9-level MLI in which 4 sets of H-Bridge are cascaded in series with the load.

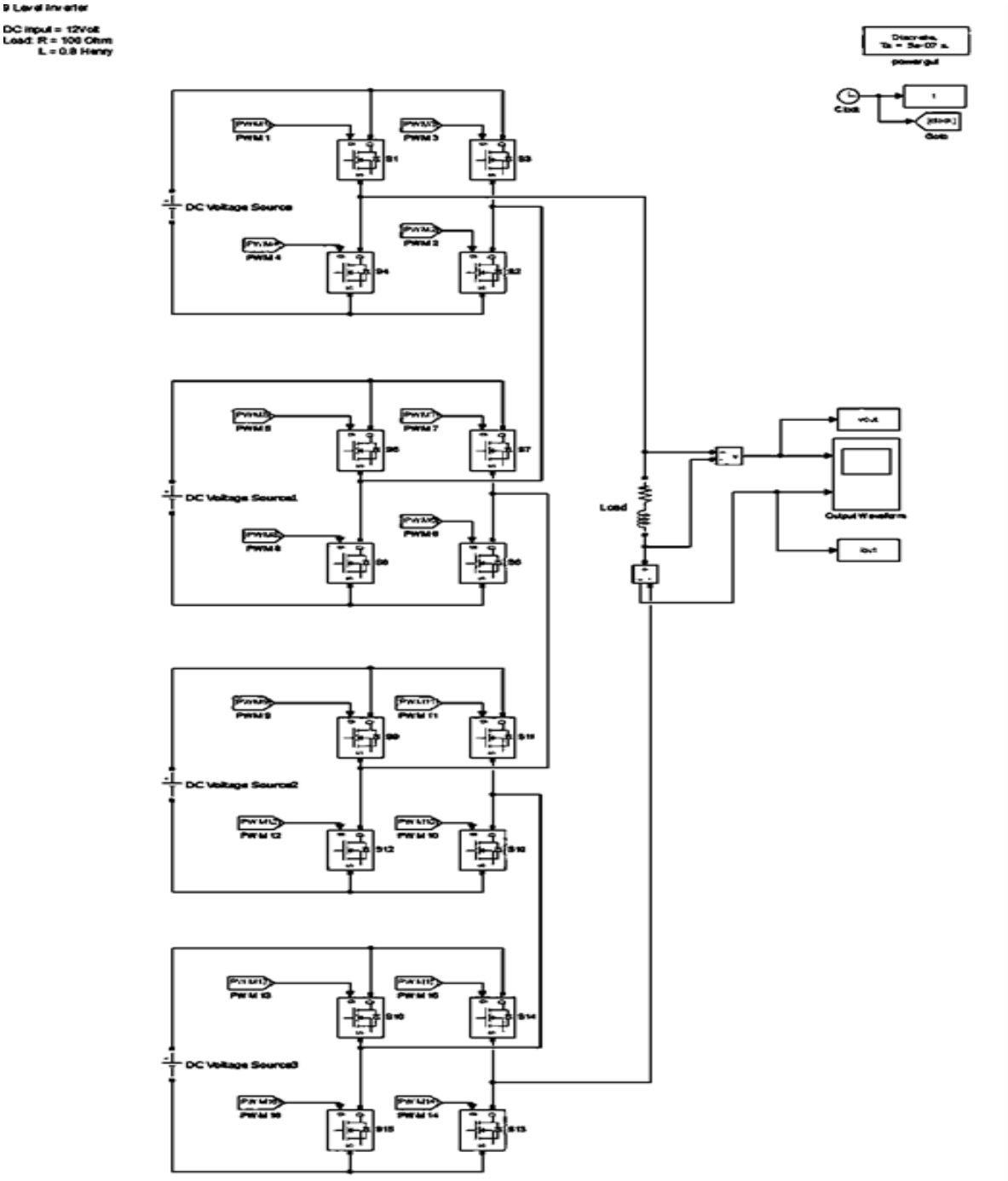

Figure 1. 9-Level CHMLI Circuit

2.1. Switching States

For a 9-Levels Inverter, the voltage levels included are 4VDC, 3VDC, 2VDC, 1VDC, 0, -VDC, -2VDC, -3VDC, -4VDC. The switching states of MOSFETs for 9-Level MLI are shown in Table 2.

Table 2. The switching states of MOSFETS FOR 9-LEVEL MLI

Voltage Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	Output Voltage
4	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	$4V_{DC}$
3	1	1	0	0	1	1	0	0	1	1	0	0	0	1	0	1	$3V_{DC}$
2	1	1	0	0	1	1	0	0	0	1	0	1	0	1	0	1	$2V_{DC}$
1	1	1	0	0	0	1	0	1	0	1	0	1	0	1	0	1	$1V_{DC}$
0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
-1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	$-1V_{DC}$
-2	0	0	1	1	0	0	1	1	0	1	0	1	0	1	0	1	$-2V_{DC}$
-3	0	0	1	1	0	0	1	1	0	0	1	1	0	1	0	1	$-3V_{DC}$
-4	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	$-4V_{DC}$

As exhibited in Table 2, each of the switch has its own unique pulses. At every of the switch, there must be another switch which its' pulses are inverted from itself. For example, the inverted pulses of S1 will be the same as the S4's pulses. With all the information written in Table 2, the modulation of a signal is ready to take place.

2.2. Modulation Technique

The switching technique can be defined as the controlling method of switches in the inverter's circuit. Pulses are needed to drive the switches (MOSFETs). Therefore, a Multi-Carrier Pulse Width Modulation is used to trigger the switches [2, 3, 4].

Modulation of pulses are the process that is comparing the Modulating Frequency (F_m) with the Carrier Frequency (F_c). The modulating frequency is a reference frequency (sinusoidal) while the carrier frequency is most-likely to inform the carrying frequency. However, the numbers of the carrier are the same as the number of H-Bridges in a MLI [5].

By employing the aforementioned technique, the modulation is the comparison of modulating frequency and the carrier frequencies. Therefore, the amplitude of carrier(s) will be reduced as the voltage level increases as the carriers will share the minimum and maximum amplitude of the modulating frequency. The minimum and the maximum amplitude of carriers of a 9-Level Inverter are tabulated as in Table 3. The circuit that is designed to generate the pulses using Multi-Carrier PWM is depicted as in the Figure 2.

Table 3. Amplitude for Carrier Waves of 9-Level MLI

Carrier No.	Voltage Level(s)	No. of H-Bridges
1	+0.5	+1.0
2	0	+0.5
3	-0.5	0
4	-1	-0.5

2.3. Simulation

The design of the Multi-Level Inverter is simulated with different condition at the DC input. Firstly, the circuit is simulated with the same and equal values of DC input. The DC input assigned in this report is 12Volt. The relationship is analyzed from the results.

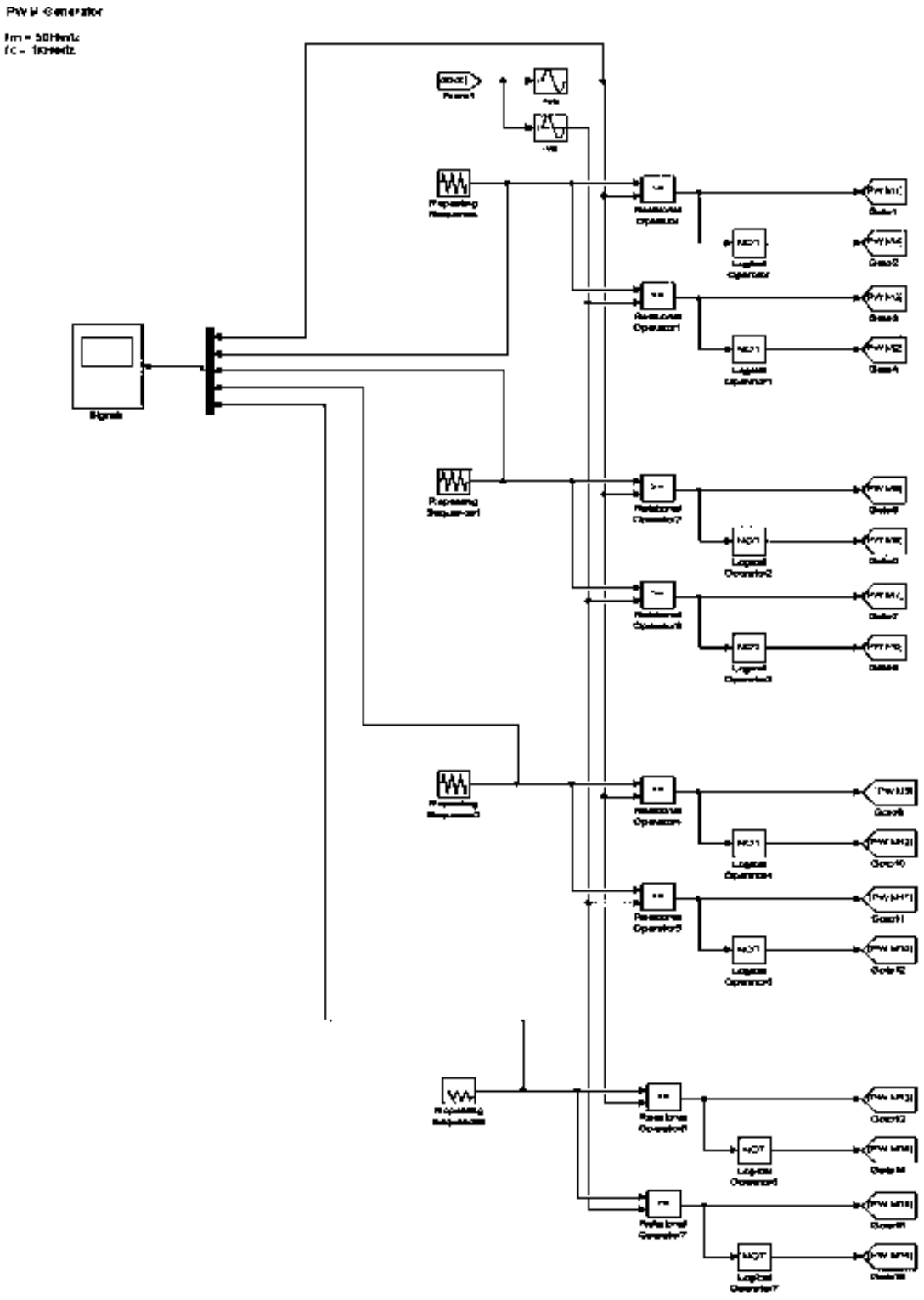

Figure 2. Modulation Circuit

3. RESULTS

The simulations for this paper include the 3-levels, 5-levels, 7-levels and 9-levels inverter and also a separated DC source. The Level Shifted Multi-Carrier PWM is used due to the numbers of carrier(s) is depending on the H-Bridges and construction of the PWM generator [6]. Hence, the number of carriers for each of the level is tabulated as in Table 4.

Table 4. No. of Carriers of MLI

Level of Inverter	Number of Carrier(s)
3	1
5	2
7	3
9	4

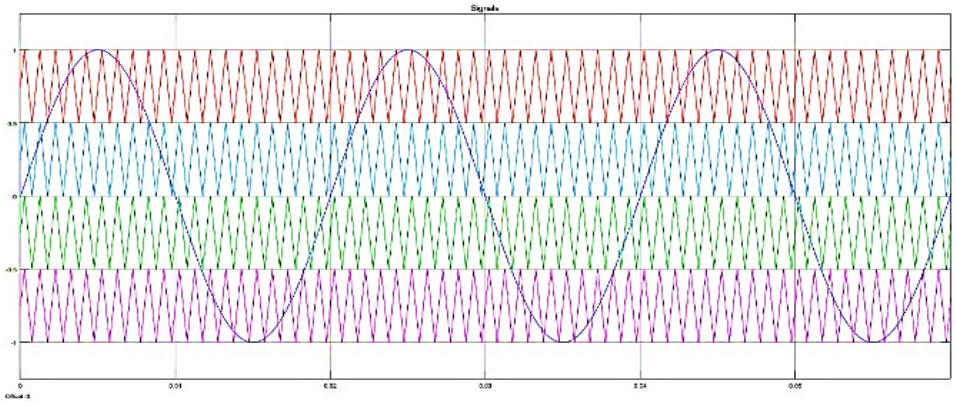

Figure 3. Modulation Waveform for 9-Level MLI

Figure 3 shows the comparison of both the modulating and carrier waves of a 9-level inverter. The generation of pulses is taking place when the both the sinusoidal and carriers are compared [7]. Therefore, pulses generated are inserted into the correct switches as stated in the table of switching state of each switches in H-Bridge. The DC input for each of the H-Bridge is set constantly as the value of 12 Volt.

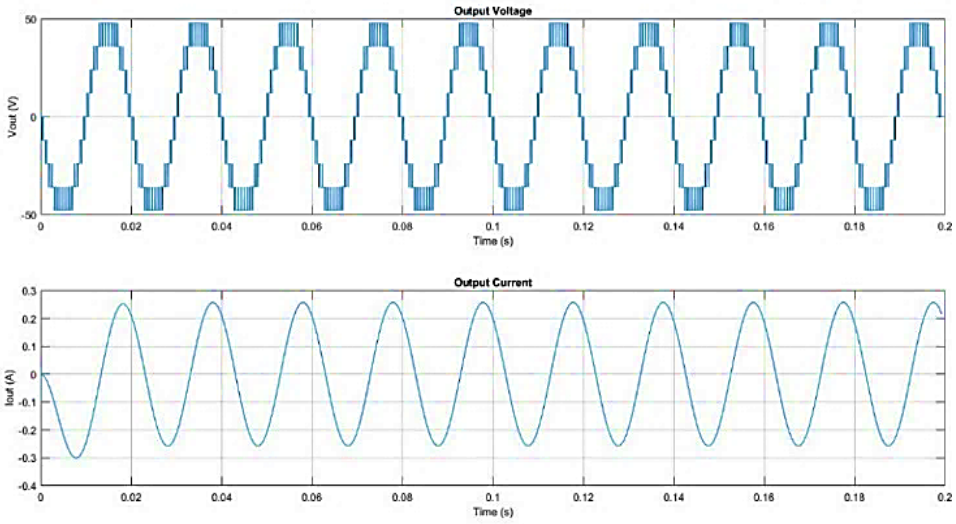

Figure 4. The Output Waveform (Voltage & Current) of 9-Level MLI

Figure 4 exhibits the output waveform of a 9-level inverter. The waveform of output voltage becomes more likely to be sinusoidal as the voltage level getting higher. Hence, the graph become smoother as the voltage level increased. The amplitude of voltage is increased as the level of MLI increases. The percentage of THD content of different levels are simulated by using FFT analysis.

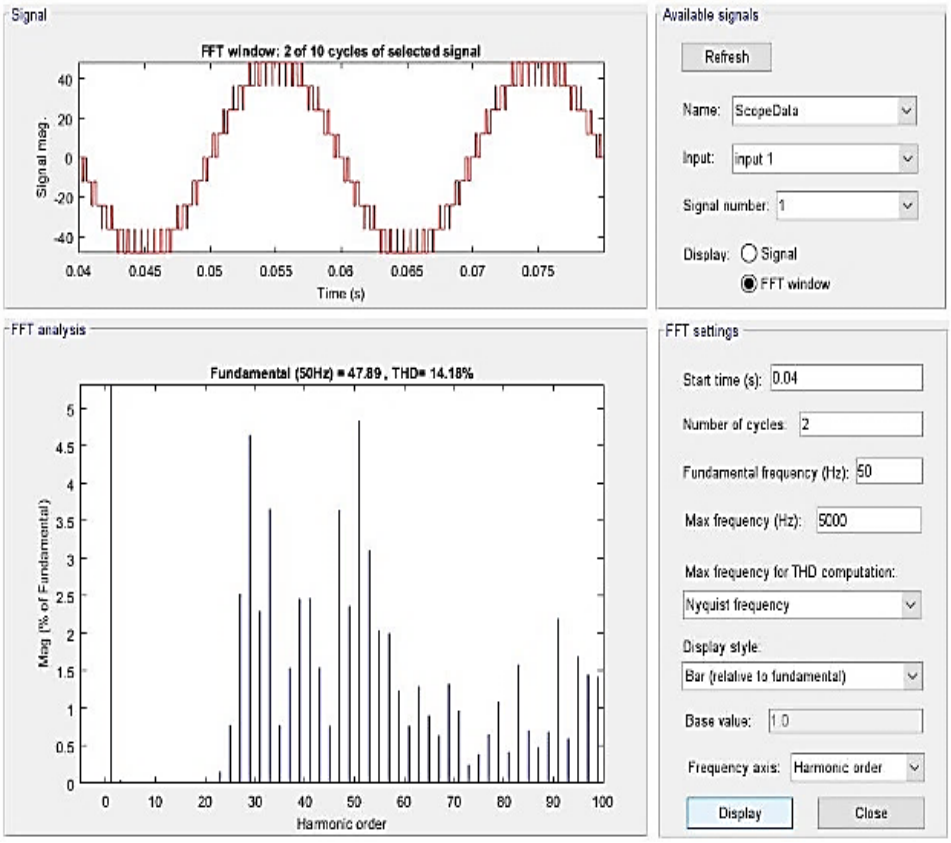

Figure 5. FFT Analysis

The %THD content for inverters of different voltage level are then compared and analyzed. The results show that the %THD decreased when the level of MLI increases. This indicates the increase of the output efficiency [8].

4. ANALYSIS

The number of carrier is increased as the number of level increases. Hence, the amplitude for each of the carrier is divided evenly across the maximum and minimum amplitude of ±1. These carrier frequencie are then compared with the modulating frequency (sinusoidal signal) to produce the pulses to trigger the switches (MOSFETs).

The number of voltage source(s) is/are increased as the number of level increases. This is due to the increase of the number of H-Bridge in the inverter. The increase of the number voltage source(s) has affected the output of voltage and current amplitude. The outputs of the inverters are tabulated in Table 5.

Table 5. Amplitude for Carrier Waves of 9-Level MLI

Level	Voltage Source(s), V_i (V)	Output Voltage, V_O (V)	Output Current, I_O (A)
3	1	12.0	0.0644
5	2	24.0	0.1262
7	3	36.0	0.1941
9	4	48.0	0.2560

Figure 6 exhibits the correlation between the numbers of levels and percentages of total harmonic distortions. The higher the number of the level of an inverter, the lesser the total harmonic distortion (THD) content of the output voltage. The THD content for the Multi-Level Inverter is tabulated in Table 6.

Table 6. % THD & Fundamental Voltage of MLI

Level	Percentage of THD Content (%)	Fundamental Voltage, V_F (V)
3	51.96	11.99
5	27.20	23.97
7	18.24	35.94
9	14.18	47.89

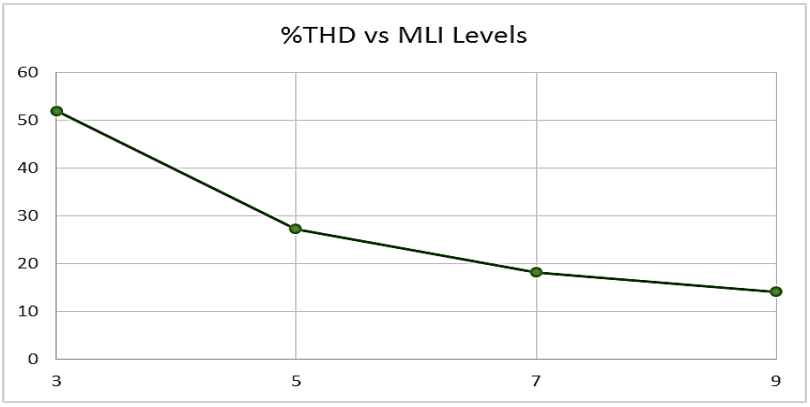

Figure 6. The Correlation between number of levels and percentage of total harmonic distortion

The voltage measurements at the output contains of the fundamental voltage and the harmonics. Therefore, The THD measurement is important to assure the quality of the output. Due to the increased of the voltage levels, THD content are found to be decreased. This would mean the difference of Fundamental Voltage and the Exact Voltage are decreased. Hence, the quality is improved as the voltage level is increased.

5. CONCLUSION

In conclusion, the %THD for 3-levels, 5-levels, 7-levels and 9-levels are found to be 51.96%, 27.20%, 18.24% and 14.18%. It shows that the percentage of THD decreased abruptly when the number of level increased. This meant that the harmonic distortion is decreased as the voltage level of a Cascaded H-Bridge MLI is increased. As a result, the performance of the Cascaded H-Bridge MLI is depending on the voltage levels in terms of THD content.

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