Indonesian Journal of Electrical Engineering and Computer Science
Vol. 11, No. 1, July 2018, pp. 144~151
ISSN: 2502-4752, DOI: 10.11591/ijeecs.v11.i1.pp144-151

Symmetrical and Asymmetrical Multilevel Inverter Structures with Reduced Number of Switching Devices

M. H. Yatim, A. Ponniran, M. A. Zaini, M. S. Shaili, N. A. S. Ngamidun, A. N. Kasiran, A. A. Bakar, J. N. Jumadril
Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia, Malaysia

Article Info

Article history:

Received Jan 25, 2018
Revised Mar 30, 2018
Accepted Apr 19, 2018

Keywords:

Asymmetrical
Multilevel inverter
Structure
Symmetrical

ABSTRACT

The purpose of this study is to analyze the operation and design of symmetrical and asymmetrical multilevel inverter structures with reduced number of switching devices. In this study, the term of conventional inverter is defined as a single cascaded inverter. Specifically, the inverter operates in three complete loops and only produces 2-level and 3-level of output voltages. Usually, cascaded structure suffers from the high total harmonic distortion. Thus, by considering multilevel structure of inverter, low total harmonic distortion reduction and voltage stress reduction on switching devices can be archived. Sinusoidal pulse width modulation and modified square pulse width modulation are used as modulation techniques in switching schemes of the designed multilevel inverters. The findings indicate that, the designed multilevel structure cause low total harmonics distortion at the output voltage. Furthermore, the asymmetrical structure is producing the same output voltage levels with reduced number of switching devices compared to the symmetrical structure is experimentally confirmed. The findings show that the total harmonic distortion for 7-level (symmetrical) and 9-level (asymmetrical) are 16.45% and 15.22%, respectively.

Corresponding Author:

A. Ponniran,
Faculty of Electrical and Electronic Engineering,
Universiti Tun Hussein Onn Malaysia, Malaysia.
Email: asmar@uthm.edu.my

1. INTRODUCTION

The developments in power electronics and semiconductor technology have triggered the improvements in power electronic systems. The multilevel inverter has many advantages compared to the typical voltage source and current source inverters and the converter is widely used in photovoltaic systems and electric vehicle applications [1],[2]. For a typical inverter structure, large passive components such as capacitor and inductor are required and consequently, the cost is increased [3],[4]. Three general types of multilevel inverters are usually referred, i.e., flying capacitor, diode clamped and H-bridge [5]. Flying capacitor type is not widely used because of the presence of high number of capacitors, meanwhile, diode clamped type is high cost of implementation compared to flying capacitor and cascaded H-bridge types [6]. Cascaded H-bridge multilevel inverter is simpler than diode clamped and flying capacitor types due to several advantages such as automatic voltage sharing, low switching stresses, low switching redundancy and requirement of least number of components, lower voltage of capacitors and diodes [7]. In Cascaded H-bridge multilevel inverter, only three output voltage levels can be produced. More bridges are required in order to produce higher voltage level, consequently the number of switching devices are increased as well [8],[9]. This may cause high semiconductor devices losses due to high number of semiconductor devices used. This drawback can be overcome by using multilevel inverters structure with reduced number of switching devices [10]. Generally, there are two topologies must be considered in order to achieve the

reduction of switching devices number with maintaining the output voltage level as the conventional structures, i.e., symmetrical and asymmetrical multilevel inverter structures [11]. With these structures, semiconductor devices losses and total harmonic distortion (THD) can be reduced [12]. Two different modulation techniques are considered in this study, i.e., modified square pulse width modulation (MPWM) and sinusoidal pulse width modulation (SPWM). The selection of modulation techniques will affect the THD of the output voltage [13],[14].

2. DESIGN OF SYMMETRICAL MULTILEVEL INVERTER STRUCTURE WITH REDUCED NUMBER SWITCHING DEVICES

Figure 1 shows the symmetrical multilevel inverter structure circuit with reduced number of switching devices. With this structure, the switching devices are reduced without affecting the output voltage levels as compared to the conventional structure. It is demonstrated that this structure comprises of two essential parts, i.e., DC sources, H-bridge structure for creating positive and the negative output voltages. The output voltage levels can be increase as conventional structure as well.

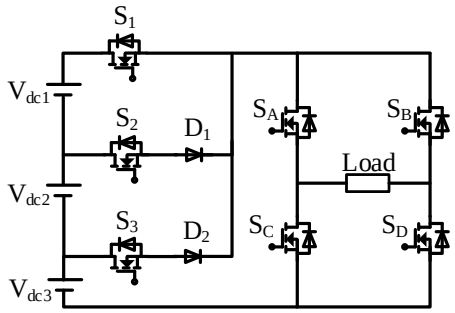


Figure 1. The Symmetrical Structure of Multilevel Inverter

The level number of output voltage is determined by referring Equation (1). Meanwhile, the switching devices number used in the structure is determined by referring Equation (2). Besides, the maximum and minimum values of the generated output voltage are estimated by referring Equation (3) and Equation (4).

$$N_{level} = 2k + 1 \quad (1)$$

$$S_{number} = k + 4 \quad (2)$$

$$V_{L\_max} = kV_{dc} \quad (3)$$

$$V_{L\_min} = -kV_{dc} \quad (4)$$

where k is the number of source.

3. DESIGN OF ASYMMETRICAL MULTILEVEL INVERTER STRUCTURE BASED

Figure 2 shows two cascaded structures of the multilevel inverter. It consists of eight numbers of switching devices and the output voltage level can be 7-level and to 9-level for asymmetrical based structure. The number of switching devices used in the structure can be estimated by referring Equation (5). Meanwhile, the maximum and minimum of output voltages generated can be estimated by referring Equation (6) and Equation (7), respectively.

$$S_{number} = 4k \quad (5)$$

$$V_{L\_max} = kV_{dc} + V_{dc1} \quad (6)$$

$$V_{L\_min} = -kV_{dc} - V_{dc1} \quad (7)$$

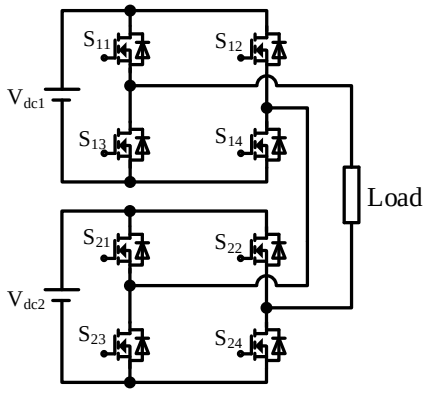


Figure 2. The Asymmetrical Structure of Multilevel Inverter

4. EXPERIMENTAL RESULTS

This section analyzes the results from simulation and experiment. The simulation and experimental results are analyzed to confirm the designed parameters and structures of the symmetrical and asymmetrical structures of multilevel inverter.

4.1. Conventional Inverter

The structure used four switches and the output voltage level for this structure is 3-level. Two different modulation techniques are used in the experiment, i.e., modified square pulse width modulation (MPWM) and sinusoidal pulse width modulation (SPWM). Figure 3 shows the switching pattern by using MPWM. For switching pattern, switches S1and S4 used same switching pattern and another switches S2 and S3 with 180° of phase-shifted and equivalent to time-delayed of 10 ms. The switching frequency is 50 Hz. Figures 4(a) and 4(b) show a good agreement between simulation and experimental results. From these results, the design principle is confirmed for the conventional inverter structure with MPWM.

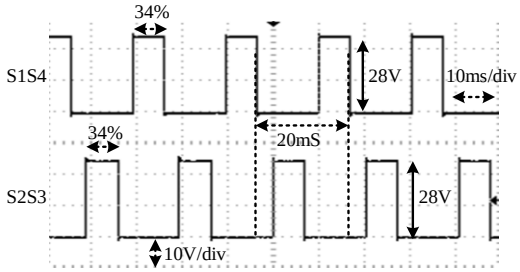
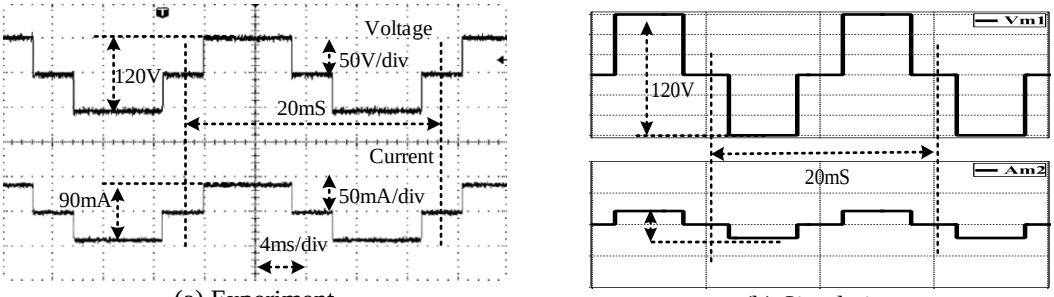


Figure 3. Switching Pattern for Cascaded Inverter Structure by Using MPWM



(a) Experiment (b) Simulation

Figure 4. Output Waveform from Cascaded Structure by Using MPWM

Meanwhile, Figure 5 shows switching pattern of SPWM. The reference frequency is 50 Hz and the carrier frequency is 30 kHz. The SPWM technique used is phase opposition disposition (POD). Figures 6(a) and 6(b) show the output voltage waveforms of the experimental and simulation results, respectively. Both results show a good agreement between experimental and simulation results.

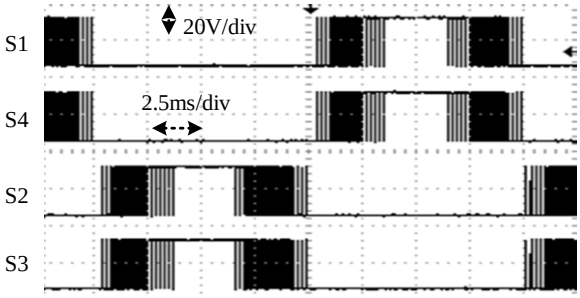
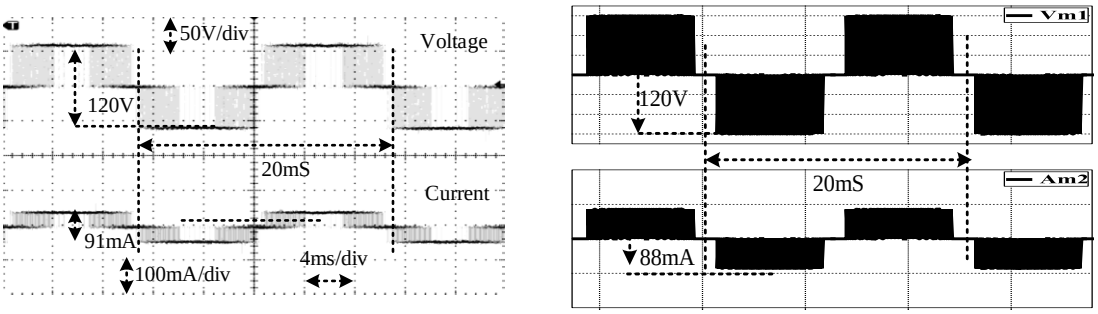


Figure 5. Switching Pattern for Cascaded Inverter Structure by Using SPWM



(a) Experiment (b) Simulation

Figure 6. Output Waveform from Cascaded Structure by Using SPWM

4.2. Symmetrical 7-level Multilevel Inverter

The selected structure, Figure 1, is considered in the symmetrical 7-level multilevel inverter structure. The inverter structure is considered for two modulation techniques, i.e., MPWM and SPWM. The structure only used seven switches in order to produce 7-Level of the output voltage. Figure 7 shows the switching pattern in MPWM. Switching signals for S1, S2 and S3 use switching frequency of 100 Hz. The duty cycle for S1 is 0.3. Meanwhile, the duty cycles for S2 and S3 is 0.15, respectively. For the switching signals SA, SB SC and SD, the switching frequency is 50 Hz with the duty cycle of 0.5. Figures 8(a) and 8(b) shows the output voltage waveforms of the experimental and simulation results, respectively. Both results show a good agreement. Thus, the designed parameters of the inverter are confirmed.

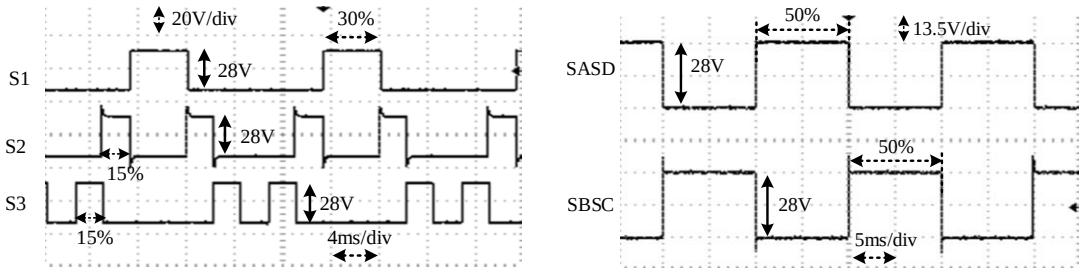
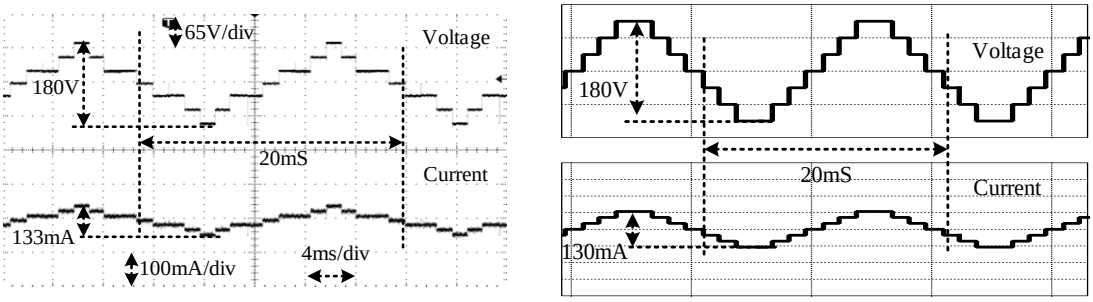


Figure 7. Switching Pattern by Using MPWM for Symmetric Multilevel Inverter



(a) Experiment (b) Simulation

Figure 8. Output Waveform From Symmetrical Structure Using MPWM

Another modulation technique used is SPWM with phase opposition disposition. Figure 9 shows the switching pattern of the SPWM. The reference frequency is 50 Hz and the carrier frequency is 30 kHz. The experimental and simulation results show a good agreement as depicted in Figure 10 for the symmetrical 7-level multilevel inverter. The peak-peak voltage is 180 V with 50 Hz of frequency.

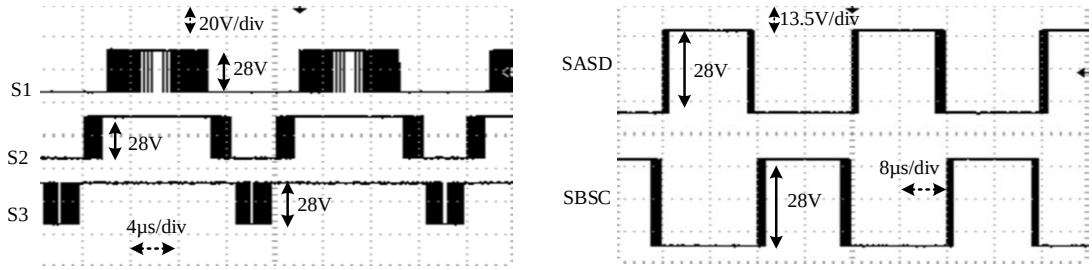
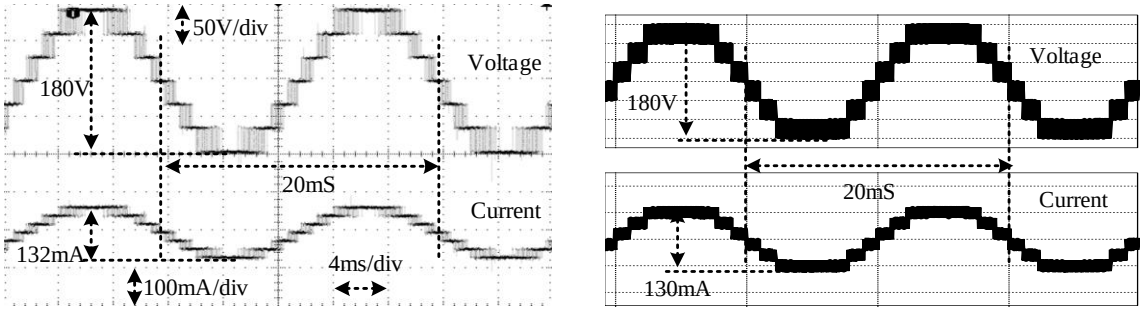


Figure 9. Switching Pattern Using SPWM for Symmetric Multilevel Inverter

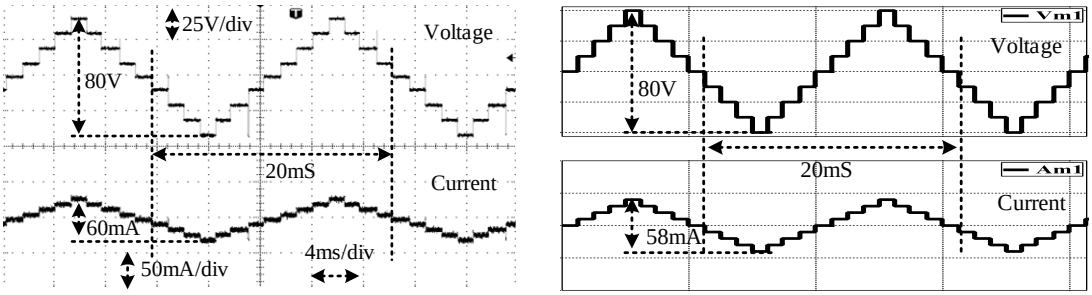


(a) Experiment (b) Simulation

Figure 10. 7-level Symmetrical Structure Output Voltage Waveform Using SPWM

4.3. Asymmetrical 9-level Multilevel Inverter

The asymmetrical 9-level multilevel inverter structure, Figure 2, is selected for the asymmetrical based structure. The selected structure uses two cascaded circuit with eight number of switches, Figure 2. The output voltage level can be produced with this structure is nine. All switching frequencies used is 50 Hz. For the switches S1 and S2, the duty cycle is 0.06 and 0.18, respectively. Meanwhile, for the switches S3 and S4, the duty cycle used is 0.06. For the switches S5 and S6, the duty cycle is 0.5 and for S7 and S8, the duty cycle used is 0.312. Figures 11(a) and 11(b) show the output waveforms from the simulation and experimental results. Both results show a good agreement for the parameters designed confirmation. The peak-peak voltage is 80 V and the output frequency is 50 Hz.

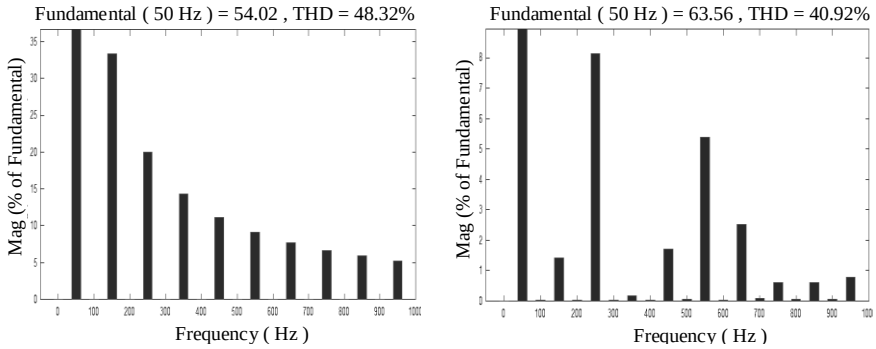


(a) Experiment (b) Simulation

Figure 11. Output Waveform from Asymmetrical Structure Using MPWM

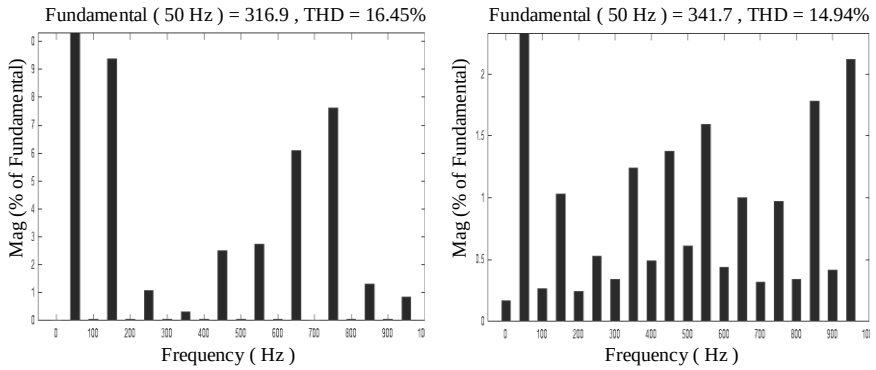
4.4. Total Harmonics Distortion

The total harmonics distortion (THD) is measured before filter the output voltage. Figure 12 shows the frequency spectrum of the conventional 3-level inverter using two modulation techniques, MPWM and SPWM. By using SPWM technique (40.92%), the THD is lower than MPWM technique (48.32%). Meanwhile, Figure 13 shows the frequency spectrum and THD of the symmetric 7-Level multilevel inverter using SPWM technique (14.94%) is lower than using MPWM technique (16.45%).



(a) MPWM (b) SPWM

Figure 12. Frequency Spectrum for Conventional 3-level inverter



(a) MPWM (b) SPWM

Figure 13. Frequency Spectrum for Symmetrical 7-level Multilevel Inverter

Figure 14 shows the THD of the output voltage waveform of the asymmetric 9-Level multilevel inverter using MPWM technique. The THD is 15.22% which is much lower than 3-Level conventional inverter using MPWM with THD of 48.32%. Table 1 shows the percentage of THD with number of output voltage level.

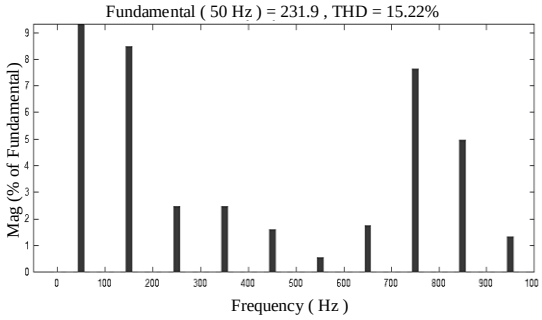


Figure 14. Frequency Spectrum for Asymmetrical Structure 9-level

Table 1. Comparison between Numbers of Output Voltage Level with Total Harmonics Distortion

Number of output voltage levels	Output voltages	%THD of output voltages
3-level MPWM	60 V	48.32
3-level SPWM	60 V	40.92
7-level MPWM	90 V	16.45
7-level SPWM	90 V	14.94
9-level MPWM	40 V	15.22

Figure 15 shows the relationship between the number of switches and output voltage level. 3-Level conventional inverter structure, it requires four switches. For the 7-level multilevel inverter structure, it requires of switches less from the conventional structure and similar goes to the 9-level multilevel inverter structure compared to the conventional structure. This trend shows that when higher output voltage level is considered, the required of switches is increased as well. Reduced switches structures offer fewer number of switches compared to the conventional structure by considering both structure have same output voltage level.

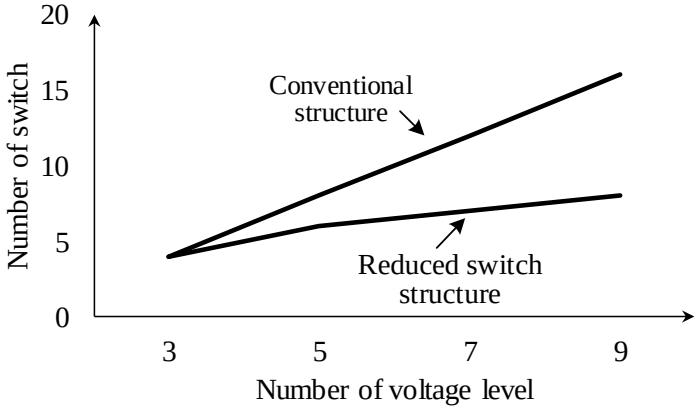


Figure 15. Relationship between Number of Switch and Number of Voltage Level

Figure 16 shows the relationship between voltage stress and number of output voltage level. Reduced switch structure of inverter has lower voltage stress on switches compared to the conventional structure. For the conventional structure, the voltage stress is always same when the output voltage level is increased. Meanwhile, for the reduced switch structure, voltage stress is reducing as increasing of the voltage level.

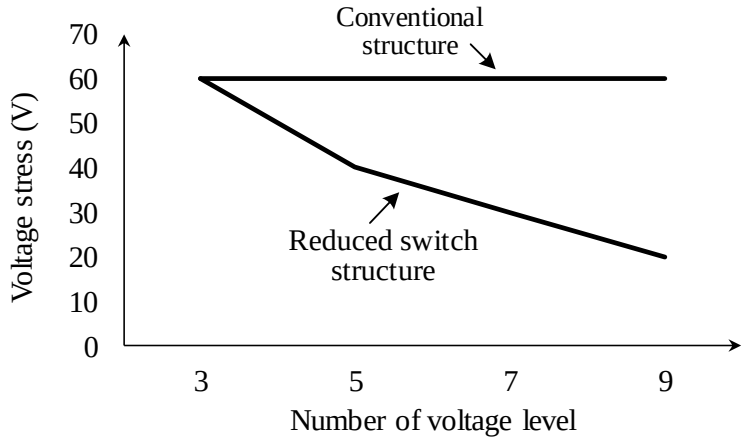


Figure 16. Relationship between Voltage Stress and Number of Voltage Level

5. CONCLUSION

Based on the simulation and experimental results, the implementation of multilevel inverter with reduced number of switches and improved cascaded multilevel inverter for symmetrical and asymmetrical inverter structures, respectively. From the study, it proves that by considering the reduction of switches number, semiconductor losses and THD is reduced and furthermore, the output voltage level is not affected. Meanwhile, by reducing switching devices, the output voltage level can be maintained and it realizes by implementing the asymmetric and symmetric topologies of the inverter structure.

REFERENCES

[1] A. B. Ponniran, *et al.*, "Minimum Flying Capacitor for N-Level Capacitor DC/DC Boost Converter," *IEEE Trans. Ind. Appl.*, vol/issue: 52(4), pp. 3255-3266, 2016.
[2] J. Rodriguez, *et al.*, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron*., vol/issue: 49(4), pp. 724-738, 2002.
[3] A. B. Ponniran and M. A. N. B. Kasiran, "Parameters design evaluation in 3-level flying capacitor boost converter," in *2017 IEEE Symposium on Computer Applications & Industrial Electronics (ISCAIE)*, pp. 195-199, 2017.
[4] A. B. Ponniran, *et al.*, "Minimization of Passive Components in Multi-level Flying Capacitor DC-DC Converter," *IEEJ J. Ind. Appl*., vol/issue: 5(1), pp. 10-11, 2016.
[5] J. S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IAS '95. Conf. Rec. 1995 IEEE Ind. Appl. Conf. Thirtieth IAS Annu. Meet*., vol/issue: 3(3), pp. 2348-2356, 1996.
[6] S. Ghosh and S. Mahanty, "Single Phase Multilevel Inverters with Simple Control Strategy Using MATLAB," *Int. Res. J. Eng. Technol*., vol/issue: 2(7).
[7] A. Prayag and S. Bodkhe, "Novel Basic Block of Multilevel Inverter Using Reduced Number of On-State Switches and Cascaded Circuit Topology," vol. 2017, 2017.
[8] M. Marchesoni, *et al.*, "A non conventional power converter for plasma stabilization," in *Power Electronics Specialists Conference, 1988. PESC '88 Record, 19th Annual IEEE*, vol. 1, pp. 122-129, 1988.
[9] S. N. Rao, *et al.*, "Implementation of Cascaded based Reversing Voltage Multilevel Inverter using Multi Carrier Modulation Strategies," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol/issue: 9(1), pp. 220-230, 2018.
[10] S. Malathy, "A New Single Phase Multilevel Inverter Topology with Reduced Number of Switches," *Int. Conf. Electr. Energy Syst*., vol. 3, pp. 1-6, 2016.
[11] S. N. Rao, *et al.*, "Integration of Reversing Voltage Multilevel Inverter Topology with High Voltage Gain Boost Converter for Distributed Generation," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol/issue: 9(1), pp. 210-219, 2018.
[12] O. L. Jimenez, *et al.*, "THD in cascade multilevel inverter symmetric and asymmetric," *Proc. - 2011 IEEE Electron. Robot. Automot. Mech. Conf. CERMA 2011*, pp. 289-295, 2011.
[13] G. J. Rushiraj and P. N. Kapil, "Analysis of different modulation techniques for multilevel inverters," in *2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*, pp. 3017-3024, 2016.
[14] S. Usha, *et al.*, "Performance Analysis of H-bridge and T-Bridge Multilevel Inverters for Harmonics Reduction," *International Journal of Power Electronics and Drive System (IJPEDS)*, vol/issue: 9(1), pp. 231-239, 2018.