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A Low Quiescent Current Fast Settling Capacitor-less Low Drop Out Regulator Employing Multiple Loops

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ABSTRACT

This paper presents a fast transient and low noise capacitor-less LDO using multiple loops. The proposed LDO exploits adaptive biasing, bulk modulation and a fast reacting control loop for achieving high performance striking reasonable tradeoffs among quiescent current, transient response and stability. The proposed LDO offers a load regulation of 0.095µV/mA while consuming quiescent current of 16 µA. It exhibits a load transient of 134.23mV with a settling time of 240.8ns against 0 to 100mA load variation with 40pF output capacitor. It exhibits an integrated noise of 31.027 pV2 /Hz at 10 Hz for a maximum load current of 100mA. The proposed LDO is designed using 0.18-µm 1P6 CMOS process.

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1. INTRODUCTION

The portable devices such as mobile phones, laptops, and wireless sensors play crucial role in every walk of life. These devices comprise several high performance analog and digital subsystems. Most of these portable gadgets being driven by battery require a dedicated power management unit consisting of dc-dc converters or linear regulators that caters to the heterogeneous needs of individual subsystems. Linear regulators offer good regulation, less output noise in a small foot print area as compared to its switching counterpart though the later enjoys better efficiency [1]. These high performance portable systems on advanced process nodes demand precise regulated output voltage against fast load transitions of the order of ns [2]. It also requires minimizing the power supply noise over the band of interest. The large capacitor connected at the output of regulation unit helps to filter the noise at high frequencies but makes the regulator sluggish and occupies significant silicon space making it unfeasible for SOC applications [3]-[4].

These externally compensated LDOs are unstable during abrupt load transients due to the proximity of output pole to the internal poles. Its stability is achieved through a zero generated due to ESR of the capacitor. The limited range of possible values of ESR and lack of control on stability for wide load current transients limits its usage [5]. A pole zero cancellation schemes, where a zero is tracking the output pole variation is introduced in [6] to ensure stability but it requires a compensation capacitor of large value that limits the bandwidth and thus influences the transient response.

The portable SoC applications discourage the usage of external capacitor for LDO regulator which led to development of on chip LDO regulator. Miller compensation splitting poles apart yields a right hand plane zero that affects the frequency response, power supply rejection (PSR) characteristics and stability [7]. The cascode compensation technique overcomes the limitation imposed by miller compensation technique and is suitable for high speed IC applications [8]. Optimum power management requires the portable devices to remain in standby mode consuming low quiescent current during quiet periods while drawing sufficiently

large currents as per the load requirements. Conventional on chip LDOs use a single large pass transistor to support entire range of loads under consideration. This limits the performance of the on chip LDO at lighter loads.

The performance of the LDO can be improved by segmenting the pass transistor into smaller units and adapting the same to match the load variations. However this topology reported in [8] suffers from poor stability at lighter loads. The SD cards of microcontroller requirea a constant voltage provided by L7850 supplying a voltage of 5v but it is targeted for PCB board [15]. A high-accuracy and robust Low Drop-Out Regulator for LED Control and Driver SOC applicable for outdoor applications [16].

This paper attempts to improve the performance by improving stability and optimizing quiescent current. LDO with segmented pass transistor is discussed in section 2. Section 3 presents the prposed regulator topology using multiple loops. Results are presented in section 4 followed by conclusions in Section 5.

2. SEGMENTED PASS TRANSISROR TOPOLOGY

In this section, the reported capacitor-less LDO in [8] is reviewed for its benefits and limitations. This develops a foundation for the proposed topology. Figure 1 shows the quasi digital segmented pass transistor based capacitor-less LDO reported in [8].

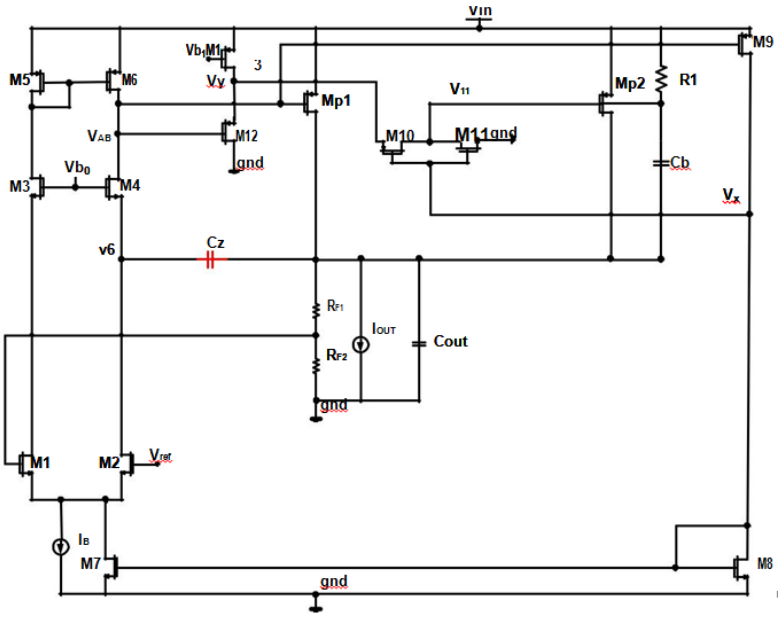

Figure 1. Segmented pass transistor based capacitorless LDO reported in [8]

The main negative feedback loop consists of transistors in the path M2–M4–M6–M7–M1 regulating the output for lower load currents where the MP1 serves as pass transistor. The second pass transistor Mp2 that supports heavy load currents is coupled between error amplifier and the regulated output through a buffer unit and an adaptively biased control unit. The adaptive bias loop for the error amplifier comprises the loop transistors in the path M2–M4–M6–M7–M1, while the adaptive bias for the control unit constitutes the path M2–M4–M6–M7–M1. The various regulation parameters influenced by the incremental change of the load current is discussed in the following.

The control units is biased with low quiescent current so as to remain it in the off state while the pass transistor Mp1 is regulating the output for lower load currents. This selection of lower bias current impacts the slew rate drive at the gate of pass transistor Mp2 during large load current transients. The latencies involved in the adaptive bias loop delays the charging and discharging of the gate capacitance of pass transistor thus a prolonged overshoot and undershoot with large overshoot and undershoots is observed. The action of relinquishing the transfer of pass transistor MP1 hold to MP2 for higher load current transients also results in oscillations over the regulated output. The pass transistor Mp2 become ineffective during lower load current when it is expected that the control unit transistor pull the gate voltage to ground to

increase the drive strength of Mp2.However,the ineffectiveness of Mp2 results in a large undershoot and overshoot with large settling time.

3. DEVELOPMENT OF THE PROPOSED REGULATOR TOPOLOGY

The architecture of the proposed adaptively biased capacitor less LDO is shown in Figure 2.The topology comprises of a telescopic based cascode error amplifier transistors M1-M6, buffer transistors M12, M13 along with a small size pass transistor Mp2 to support lower load currents. The feedback of output voltage to the error amplifier differential input is through Rf1, Rf2 resistors. The response to higher load currents is handled by a large pass transistor Mp2 coupled to the error amplifier through buffer transistors M12, M13. The control unit comprises of M10, M11 transistors switches the control form one pass transistor to the other to regulate the output once the load current increases to a larger value. The decision to switch the pass transistors operation is taken while the threshold limit set by the sense transistors constituting M9, M8 is crossed. The multiple stage topologies are compensated by a cascode compensation stage formed by capacitor Cz, along with a current buffer transistor M4. The output capacitor Cout is selected to be of 40pF.The adaptive biasing stage employed for the error amplifier and control unit develops a operating current through the stages proportional to load current thus conserving power during low load currents. It also improves the slew rate drive at the gate of pass transistor and thus supporting the transient response.

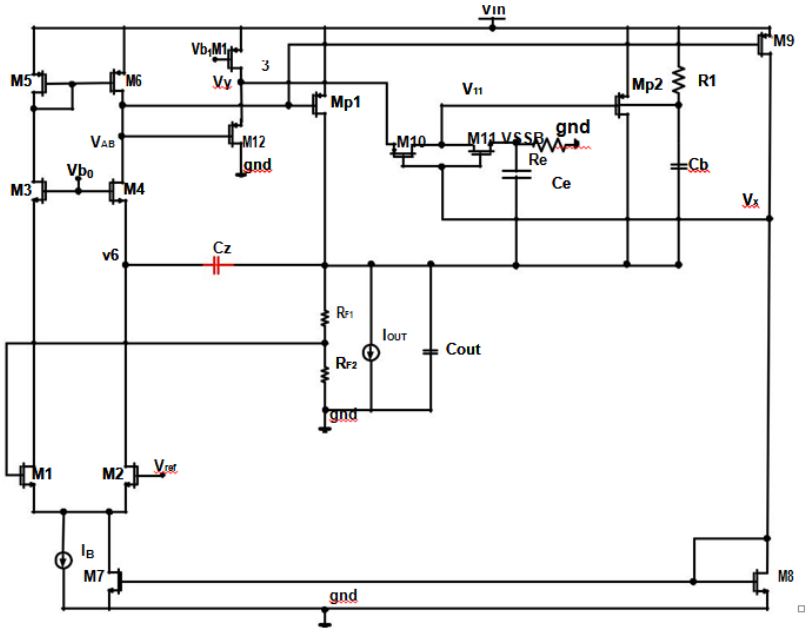

Figure 2. The proposed capacitor-less low drop out regulator employing various techniques

A fast reacting path (Re,Ce) connected between the output and the control transistor unit charges and discharges the pass transistor faster and thus assists in the fast settling of output voltage. The inefficiency of pass transistor Mp2 to regulate the output while the gate voltage falls below threshold value is augmented by R1,Cb that modulates the bulk voltage in addition to gate voltage drive leading to better drive of the pass transistor MP2 to source current and regulates the output voltage. The detail operation of different blocks of the topology is explained below.

3.1. Error Amplifier Configuration

The low quiescent current consumption (power efficiency) and better accuracy (load and line regulation) are the vital parameters of error amplifier. It should survive low supply voltage conditions which occur across the pass transistor and reject the supply variations to the output.

The proposed LDO uses telescopic based configuration with NMOS input pair transistors (M1-M2). The NMOS input pair transistors with its large Trans conductance contributes to a higher bandwidth required for LDO. The load of this input differential pair (M1.M2) is a current mirror load (M5, M6). The cascode

compensation configuration of transistor M4 along with Cz supports good rejection of supply variations on the output and also facilitates the use of low capacitance for compensation. This compensation technique also reduces the Cc value as the cascode structure contributes an increased trans conductance and thus exhibiting a multiplying effect on the original capacitance value. The differential feedback loop operation constitutes differential pair transistors of error amplifier and its load transistors (M1-M6) driving pass transistor Mp1 and feedback resistors providing sampled voltage to the non-inverting input of error amplifier. The other feedback loop path constitute error amplifier transistors M1-M6,buffer transistors(M12,M13),control unit transistors (M10,M11),pass transistor Mp2, and through feedback transistor fed back to differential pair input. The adaptive bias loop meets the demand of increased current efficiency, load regulation and high slew rate requirement of the error amplifier through adaptive biasing stage constituting transistors(M1-M6) of error amplifier, buffer transistors (M12,M13),pass transistor Mp2 sensing transistors M9,M8 and M7 modulating the tail current.

This adaptive biasing configuration senses the changes in the load current and alters the operating current of the error amplifier and thus reserves the current consumption only when required i.e. during large load currents while maintaining low operating current for steady state operation. This method which increases operating currents high during load transients improves the transient response of the regulator by increasing the slew rate drive at the output of error amplifier.

3.2. Buffer Circuit Configuration

A Buffer circuit in conventional LDR couples the error amplifier and large pass transistor to imply a low capacitance and high input resistance at error amplifier output thus supporting error amplifier good loop gain and bandwidth.

In the proposed topology, the pass transistor MP1 that supports lower load currents from 0 to 1mA is of a dimension 5.16µmX0.18µm impinges a low value of node capacitance at the output of error amplifier. However, the other pass transistorMp2 is of large dimensioning 32.14µm X0.18µm to support for the higher range of load current from 1mA to 100mA. Therefore, the pass transistor Mp1is driven directly from the output of error amplifier while the other pass transistor with its huge size is isolated from the same error amplifier by a source follower unit i.e. a buffer. The requirement of switching operations between the two pass transistors according to the requirement of load transients is met by employment of a control unit comprising transistors (M10, M11, and MP2). An added advantage would be is to have a dynamically adaptability of it in respect of load transients so that a smooth relinquish operation between them is done using a threshold limit imposed by the current comparator unit comprising transistors (M8,M9).

Although this configuration assists in a good response but the latencies involved in the loop makes it sluggish resulting in a great voltage shoots at the output. To circumvent this localized regenerative circuit comprising RC network shown in Figure 2.

It is discerned from the Figure 2. that the (Vsb) node of control section is not connected to ground as usual but is conveniently AC coupled to the output voltage (Vout) through a coupling capacitor Ce and dc biased to ground through Re. The load variations at the output couples their changes to the Vgs of M11 resulting in a fast sourcing and sinking operations on gate capacitance of Mp2 well ahead of the feedback loop action to regulate the output thus allowing MP2 to source large currents to the output. The simulation waveforms at different nodes of control unit are shown in Figure 3. The transient waveforms in sequence shows the response voltage V11 at the gate of pass transistor MP2, VSSB node voltage and the control element current IM11 with and without fast path. It reveals that there is sudden increase in the slope representing fast charging and discharging of the large value of gate capacitance of pass transistor Mp2 leading to improved transient response with reduced voltage variations at the output.

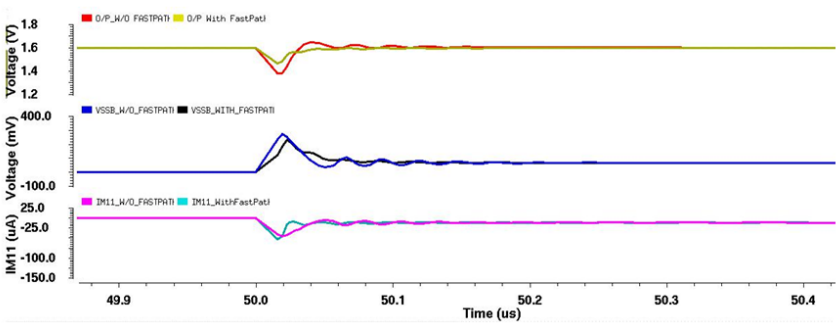

Figure 3.The transient response of the control section at different nodes

So the regenerative action of fast reacting path can dynamically adapt and boost the slew rate drive of the control element overcoming the bandwidth limitations of above discussed adaptive control loop. A concern of worth noting in the positive feedback (regenerative) loop is its prone to oscillations and difficult to revert back of latched events.so it is ensured that the loop gain of the loop is negative and its poles do not interfere with the main feedback loop and thus conserves the stability. The frequency response for the inner loop shown in Figure 4 is less than 0dB and claims the LDO stability.

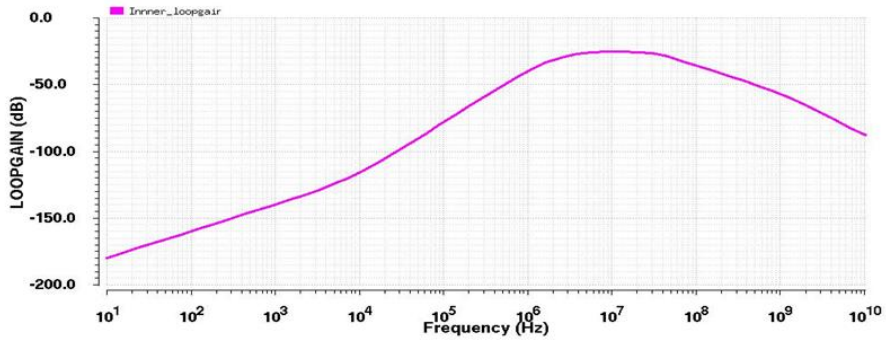

Figure 4.Frequency response of inner loop comprising control unit and pass transistor Mp

3.3. Pass Transistor Configuration

Conventionally a large pass transistor is used in support of voltage regulation for a wide range of load currents transients. The large pass transistor with its huge capacitance at the gate of pass transistor affects the LDO stability while operated at lower load currents. However, the stability can be sustained provided a huge miller compensation capacitor is utilized that reduces the bandwidth and avoids the existence of dominant pole near other parasitic poles. This occupies a large foot print area on silicon. A favorable solution is segmentation of pass transistors. The pass transistors configuration comprises a light load supporting pass transistor MP1 and heavy load supporting pass transistor MP2 both connected in parallel between input and output of voltage regulator.Mp1 is dimensioned small (5.16µmX0.18µm) to support low load currents while MP2 dimensioned big (32.14µm X0.18µm) for support of large load currents. The R1,Cb connected at the bulk terminal of pass transistor Mp2 transfer the voltage variations at the output terminal to its bulk leading to variation of its threshold which allowing pass transistor to source more current than normal and regulating the output.

4. RESULTS

Adaptively controlled multi loop capacitor-less low drop out regulator is designed using UMC 180nm CMOS technology with a dropout voltage of 200mV at maximum 100mA load. It is designed to deliver an output voltage of 1.6V for an input voltage range of 1.4-1.8V while consuming a total quiescent current of 16uA using 2pF compensation capacitor and a relatively smaller output capacitor of 40pF for stability.

The transient response of the proposed regulator is depicted in Figure.3 and Figure.4. The effect of the inclusion of the bulk modulation and fast reacting path are shown explicitly. It is clearly seen that the impact of bulk modulation and fast reacting path minimizes the overshoot (95.56mV) and undershoot (134.23mV) voltage with corresponding settling time of 4.35µs and 240.81ns.The limited swing available at the gate of MP2 to source large currents in response to output voltage variations is supplemented by bulk modulation. Further improvement is attributed to the fast reacting path. It is also discerned that the regulated output voltage is free of any oscillations as compared to the adaptively bias low dropout regulator.

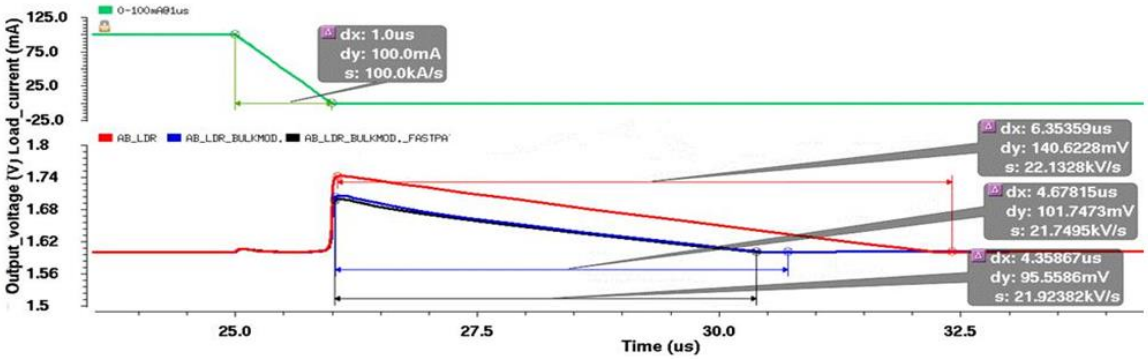

Figure 5. An overshoot response for a load current varying from 100 to 0 mA

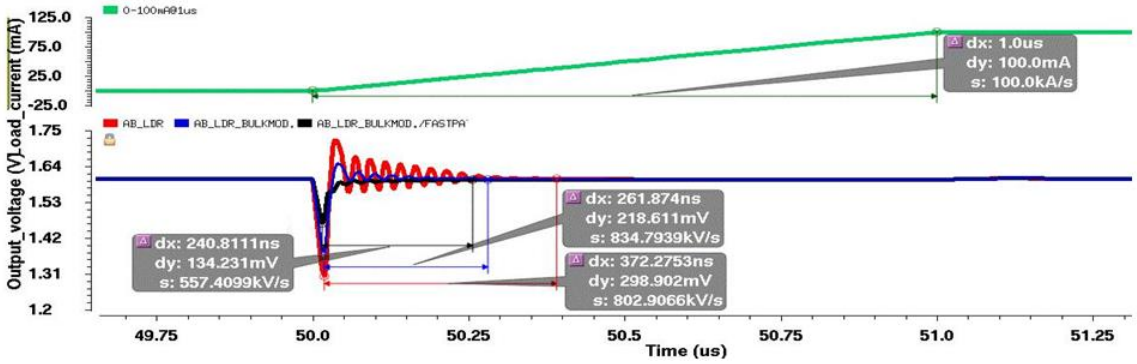

Figure 6. An undershoot response for the load current varying from 0 to 100 mA

The dc performance metrics load/line regulation determines the ability of a regulator to maintain a constant output voltage despite the changes in the supply or load current changes. A good load regulation/line regulation protects the integrity of regulator. Figure 5 represents the line regulation at load currents of 100uA and 100mA.

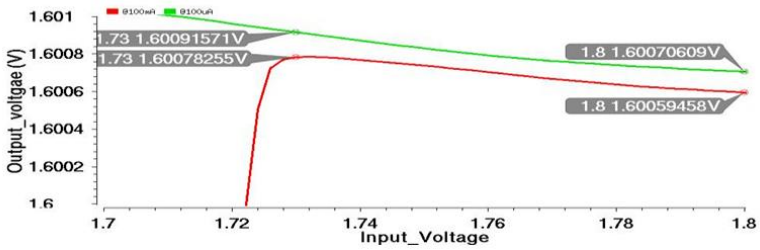

Figure 7. Line regulation for load current 100µA and 100mA

Ideally, the curves overlay with each other all along the change in the input voltage range from 1.7-1.8V truly signifying zero load regulation. However, the gap between them portrays a load regulation. The load regulation of the proposed regulator for a load current of 100uA is 2.1mV/V while the slope is 1.9mV for a heavy load condition of 100mA. The load regulation for the proposed LDO for a load current swept between 0 to 100mA is shown in Figure 8.

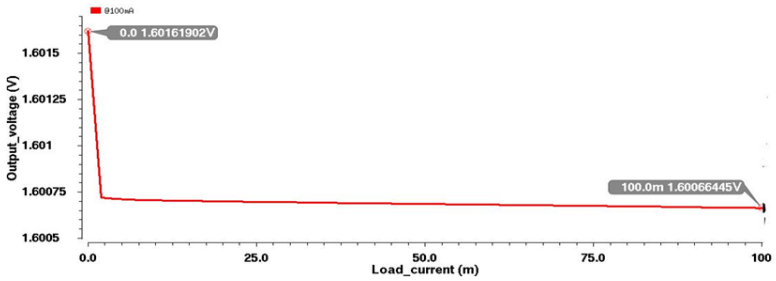

Figure 8. Load regulation for load current varying from 0 to 100mA

The output voltage changes nearly 0.95mV across the load current change form 0 to 100mA.This translates to a load regulation of 0.095µV/mA. The load regulation and transient response voltage variation in the process corners is shown Figure 9 and Figure 10 respectively.

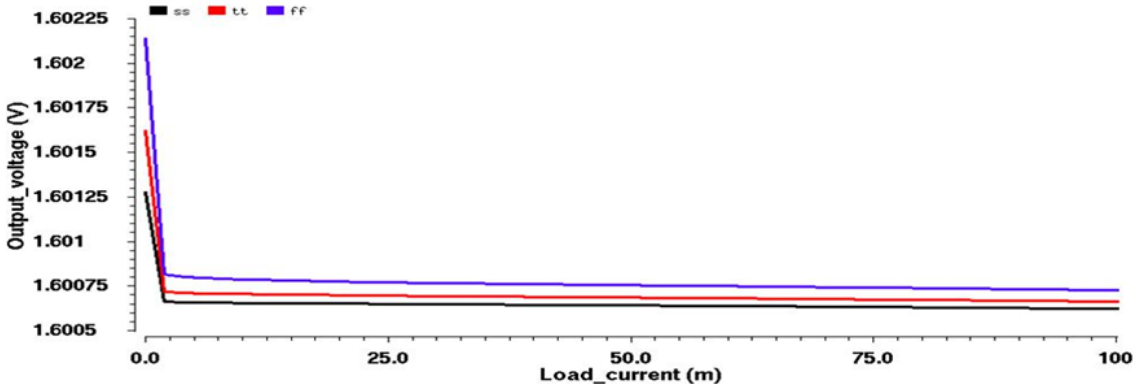

Figure 9 Load regulation for different corners

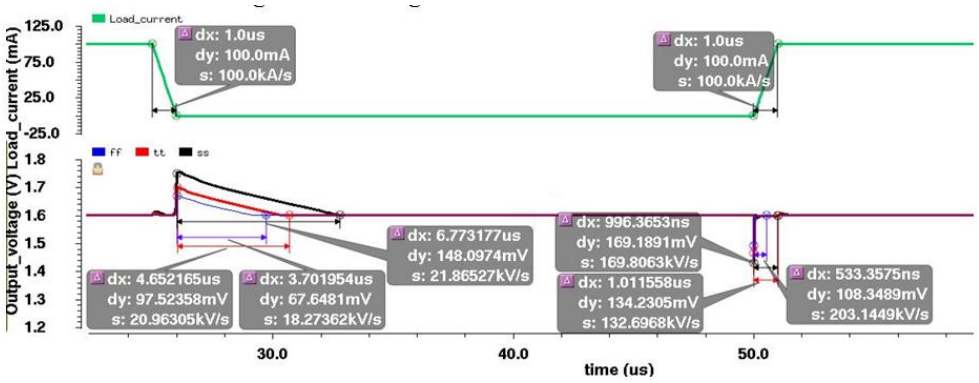

Figure 10. Transient response of the regulator @100mA for different corners (ss-slowslow,ff-fastfast,tt-typicaltypical)

The proposed topology while subjected to temperature variations between -40 oC to 70oC results in output voltage variation as shown in Figure 11. The variation in the output is observed to be 1.2mV at 0mA load current.

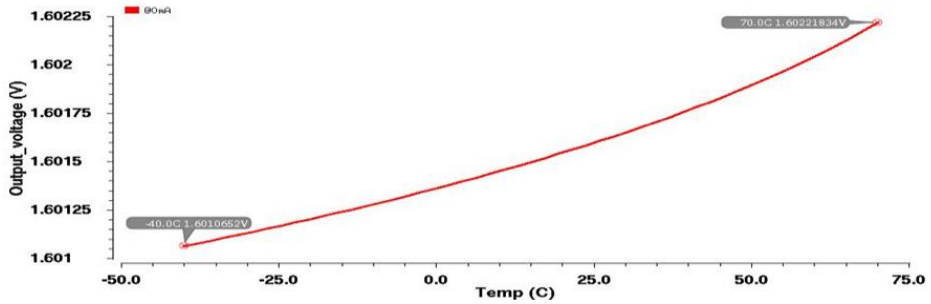

Figure 11.Output voltage variation w.r.t temperature for a load current of 0mA

The stability of the proposed regulator is ensured by the adequate phase margin and unity gain frequency at different load currents and its variation with load current is shown in Figure12. Figure10 depicts the unity gain frequency and phase margin at different values of load current. The fixed tail current applied to the error amplifier dominates over adaptive biasing current in the range of load current from 0 to 25mA causing the error amplifier pole remain static while the output pole moves towards it. It results in variation of phase margin between 82.3oand 90o and unity gain frequency varying between 0.5MHz and 1MHz. As the load current increases above 25mA the effect of adaptive biasing increases the unity gain frequency and brings error amplifier pole in proximity with output pole effectively decreasing the phase margin to 780 at maximum load current. The quiescent current required to keep these poles separated is relatively less and thus conserves power.

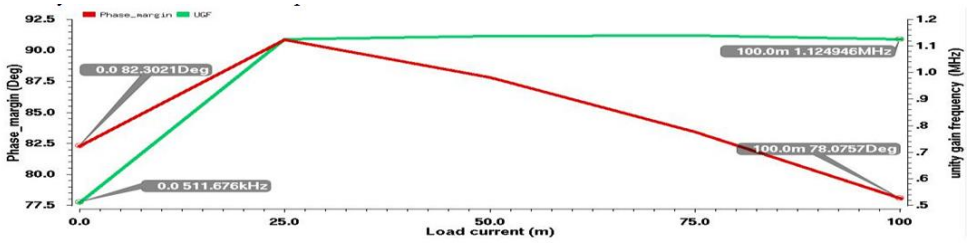

Figure 12. Phasemargin and unitygain frequency as a function of load current

The output noise power spectral density of the proposed LDO versus frequency is demonstrated in Figure 13. The spot noise at DC frequency is 30.208pV2 /Hz and 31.027 pV2 /Hz at no-load and full-load conditions.

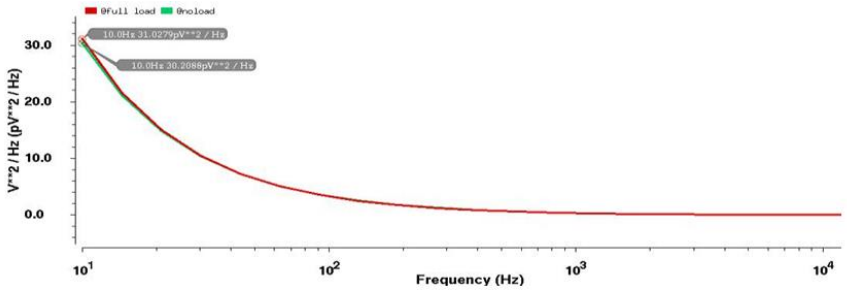

Figure13. Power Spectral Noise density of the proposed LDO

Table 1. The Performance Parameters Comparison of the Proposed Topology with the State of Art LDOs

Parameter	[8]	[9]	[10]	[11]	[12]	[13]	This work
Tech	0.18	0.18	0.18	0.18	0.13	0.35	0.18
V_{in}(V)	1.8	1.4	1.5	1.2	1.2	2.0	1.8
V_{out}(V)	1.6	1.2	1.2	1.0	1.0	1.8	1.6
Undershoot(mV)	170	110	125	342	140	89	138.89
Overshoot(mV)	200	85	65	192	90	129	90
V_{out}(pp)	370	195	190	534	230	218	228.89
Iq(min)	4.8	0.61	2.4	14	27	50	1.5
Iq(max)	6	141	242	14	27	50	16
I load(mA)	100	99.99	99.9	99.95	100	99	100
Cout(pF)	40	100	100	100	80	100	40
Sett.time(µs)	2	10	4	4	2.5	1.5	0.26
*FOM(sett.time)	0.12	14.1	9.68969	0.56028	0.675	0.75758	0.0225

*Figure of merit(FOM) $=\frac{T_R * I_Q min}{ILOAD}$

The performance parameters comparison of the proposed topology with the state of art LDOs is tabulated in Table 1. The proposed regulator consumes the lowest quiescent current of 1.5 µA along with a small output capacitor of 40pF similar to [8]. However, [8] exhibits a large overshoot and undershoot of approximately +200 mV and 170 mV respectively with large settling times. The dependency of overshoot and undershoot on the value of quiescent current, output capacitor, and step change in load current is characterized through a figure of merit FOM = Cout*Vout(pp)/Iload . A lower FOM is desirable for portable applications. The proposed regulator with lowest FOM of 0.488 definitely improves the battery life time of portable applications.

5. CONCLUSION

The adaptive biasing technique used for error amplifier and control section provides additional current to their stages for the duration of load transients while using minimal current at steady state operation. This minimal current conserves energy and extends battery life time used in mobile applications. Additionally, it also supports better slew drive at the gate of pass transistors thus influencing transient response. The selection of segmented pass transistors based on the load current demand paves the way for simpler compensation (reduced compensation capacitance) and fast charging and discharging operation of gate of pass transistors facilitating fast transient response. The control section transistors output swing limitations in regulating the output is overpowered by the bulk modulation strategy applied for pass transistors without consuming any extra power. The inability of low value of output capacitor to support response to sudden load current transients is further assisted by a regenerative action of control section.

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