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The Analysis of Soft Error in C-elements

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ABSTRACT

Soft errors are a serious concern in state holders as it can cause temporarily malfunction of the circuit. C-element is one of the state holders that is used widely in the asynchronous circuit. In this paper, the investigation will focus on the vulnerability of two types of C-element towards soft errors. A framework has been proposed for the rate of error due to neutron spectrum energy that can cause failure in the state holder. Effective analysis has been conducted on two different C-elements at different nodes by using UMC90 nm technology and 180nm technology. Based on the vulnerability data, a method for assessing vulnerability on a different implementation of C-elements has been developed. From the obtained data, it can be concluded that SIL is more resistant towards soft errors.

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1. INTRODUCTION

Asynchronous circuits operate without a clock and there are numerous advantages of using asynchronous circuits such as no clock skew problem and no global timing issues. Asynchronous circuits are also less affected by the technology and process [1]. There is also power issue in synchronous design since it utilizes clocks to make any transition at the logic. On the other hand, the power in asynchronous design will be less compared with synchronous design. However, one of the disadvantages of asynchronous circuit is the circuit failure due to deadlock: A state where the system will be disabled indefinitely until the system has been reset or the error is filtered or corrected from the system. That means the circuit will be in the waiting state unless there is a feedback or some kind of acknowledgement signal since it is depended on the data itself rather than clock to function. Single event upset (SEU) has been identified as a possible reason that caused data corruption. The term soft error refers to the temporarily error that is due to the particle strike provided the sufficient current and with certain width of current pulse is needed to cause the state change.

The PMOS or NMOS will be the most sensitive towards SEU when it is in the OFF mode, in particular at the drain region. Figure 1 shows the single event transient (SET) produced after an energetic ionizing particle has been brought to the silicon near sensitive device [2]. The density of electron-hole pairs is produced by particle as shown in Figure 1(a). The carriers are collected by electric field and will cause the charge collection to expand due to drift current (Figure 1(b)) and result in the sudden current pulse. Then, the diffusion current will dominate until all the excess carrier have been collected, recombined or diffused away from junction area (Figure 1(c)). The size of funnel as shown in Figure 1(b) and collection time is very much inversely proportion with the substrate doping. The collection time is usually complete within picoseconds and the diffusions current begin to dominate until all the excess carriers have been collected [3].

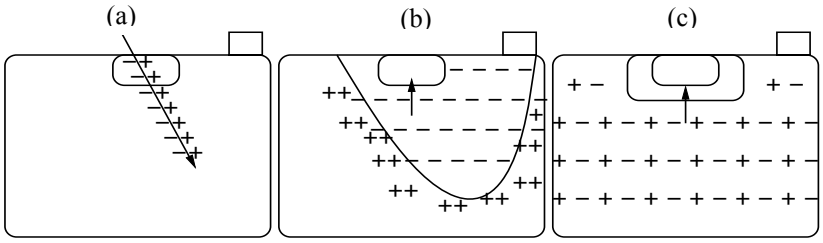

Figure 1. SET produced [2]

2. COMPARING SEU WITH DIFFERENT TECHNOLOGY

In order to compare C-element with different technology against SEU, the circuits chosen are Single Rail with Inverter Latch (SIL) as shown in Figure 3(a) and the corresponding layout in Figure 3(b). The circuit is modelled to have the same width of the main transistors and the feedback transistors. For this purpose, two different types of Cadence Technology are used in the simulation: UMC90nm and 180 nm.

A current pulse can be represented as having fast rising time and slow falling time. The amplitude, rising time and falling time of the current pulse depend on factors such as the type of particle, the energy of the particle and the angle of the strike. These factors can add complexities in modelling current pulse. The model shown in Figure 2 is used as a current injection to compare the critical charges between the nodes and C-elements. The model in [4] stated the rising and falling times of current pulse to be 50 ps and 164 ps respectively.

The current pulses are injected at the main transistors and the output of the circuit as shown in Figure 3. The rising and falling times of the current pulse are fixed. However, in order to change the area under the curve, the amplitude is varied until the output is flipped. The simulation is done using circuit analyser (spectre). The amplitude of the current pulse is increased until the output is flipped at nodes (i) (ii) and nodes (iii) of Figure 3(a). The critical charges which corresponds to the amplitude of the current pulse that causes the state to change are obtained and the experiments are repeated with different technology and with different temperature.

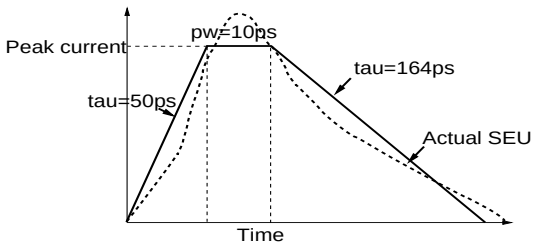

Figure 2. Model of current pulse [4] condition

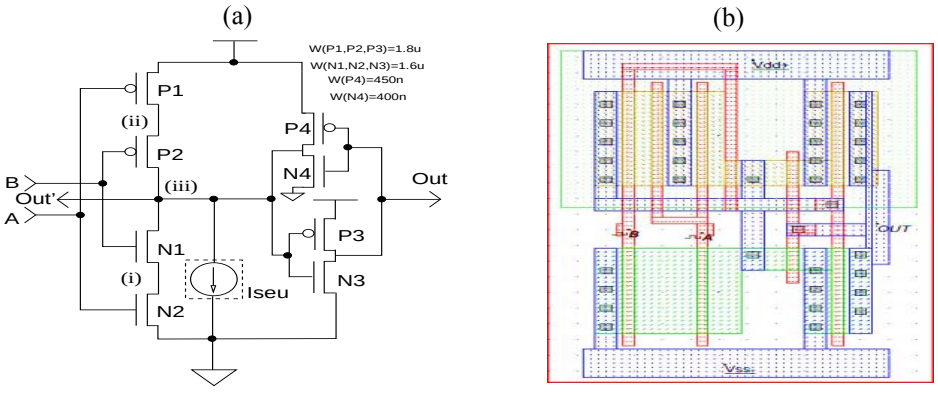

Figure 3. (a) Schematic SIL; (b) Layout of SIL

The work initially investigated the effect of soft errors on two different C-elements by varying the width of the injected current pulse into various locations on the circuit. Authors in [5] have defined valid output such that Out(t) ≤ 0.2. The responses of the state holders are characterized into three possible categories as shown in Figure 4 (a, b), and explained in the following:

a) No change to the state holder – There is no significant output pulse that has been generated and will not cause any state change. It is assumed that if the generated pulse is less than 0.2 of the input pulse such pulse will be further attenuated in the following gates and caused no further damage as seen from circles "a" in Figure 4 (a, b).
b) Pulse output- Over a small range of input pulse width, the pulse output is generated. It is assumed that if the generated pulse is 0.2 or more of the input pulse, such pulse will be very likely to cause the problem as seen from circles "b" in Figure 4 (a, b).
c) State change – At certain width with fixed magnitude of current pulse, the state holder may change its state as as seen from circles "c" in Figure 4 (a, b).

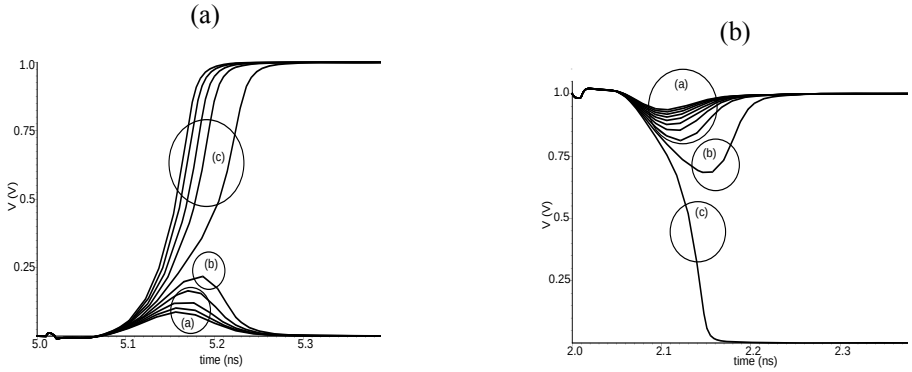

Figure 4. (a) State holder change from low to high (0-1); (b) State holder change from high to low (1-0)

Generally, as the technology is scaled down the transistors are very vulnerable to soft error. Figures 5 (a, b) and 6 show the critical charge of the injected soft error with different technology and temperature at different nodes. As temperature increases, it degrades the threshold voltage, carrier mobility and saturation velocity [6, 7]. Therefore, the carrier mobility degrades and the drain current becomes lower result in the sensitivity of the node towards SEU is increased. Hence, the critical charge needed to flip the output is decreased. To observe the change in temperature variations, the process corner is set to TT with the width of the transistors are identical.

Figure 5(a) shows the critical charge with respect to temperature variation when the soft error is injected at node (i). The critical charges reduce by 38% for (1- 0) change and by 51% for (0-1) change as the technology change from 180 nm to 90 nm. The critical charge also decreases by 29.2% for 1-0 change and 8.2% for 0-1 change as the temperature increases from $-40^0\ C$ to $100^0 C$ for 180nm technology. Similarly, for 90nm technology the critical charges decrease by 21.5% for 1-0 change and 9.2% for 0-1 change on the same temperature increment. The experiments are repeated at node (ii) and (iii).

Figure 5(b) shows the critical charge with respect to temperature variation when the the soft error is injected at node (ii) The critical charges reduces by 39% for (1-0) change and by 49% for (0-1) change as the technology change from 180 nm to 90 nm. The critical charge also decreases by 27.3% for 1-0 change and 10.1% for 0-1 change as the temperature increases from $-40^0\ C$ to $100^0 C$ for 180nm technology. Similarly, for 90nm technology the critical charges decrease by 24.5% for 1-0 change and 12.9% for 0-1 change on the same temperature increment.

Figure 6 shows the soft error is injected at node (iii). The critical charges reduce by 39% for (1-0) change and by 51% for (0-1) change as the technology change from 180 nm to 90 nm. The critical charge also decreases by 27.4% for 1-0 change and 8.2% for 0-1 change as the temperature increases from $-40^0\ C$ to $100^0 C$ for 180nm technology. Similarly, for 90nm technology the critical charges decrease by 23.7% for 1-0 change and 10.3% for 0-1 change on the same temperature increment. It is concluded that as the technology is scaled down the transistors are very vulnerable to soft error by 38% for (1-0) change and by 51% for (0-1).

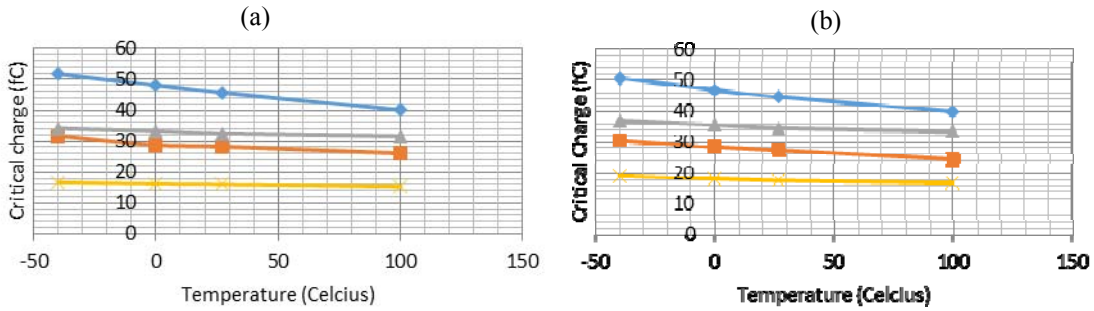

Figure 5. (a) Temperature variation for SIL configuration at node (i) with different technology; (b) temperature variation for SIL configuration at node (ii) with different technology

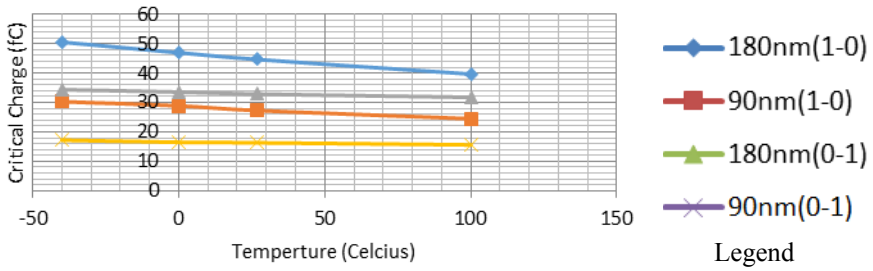

Figure 6. Temperature variation for SIL configuration at node (iii) with different technology

3. COMPARING SEU WITH DIFFERENT C-ELEMENTS

In part 3, the experiments in part 2 are repeated for single rail with conventional (SC) pull up and pull down as shown by Figure 7(a) and the layout in Figure 7(b). For input A=1 B=0, only node (ii) and (iii) are vulnerable to soft error as other nodes are connected with supply voltage and hence not affected with soft error for both SIL and SC. The critical charges are obtained for both nodes with the temperatures are varied from $-40^0\ C$ to $100^0 C$.

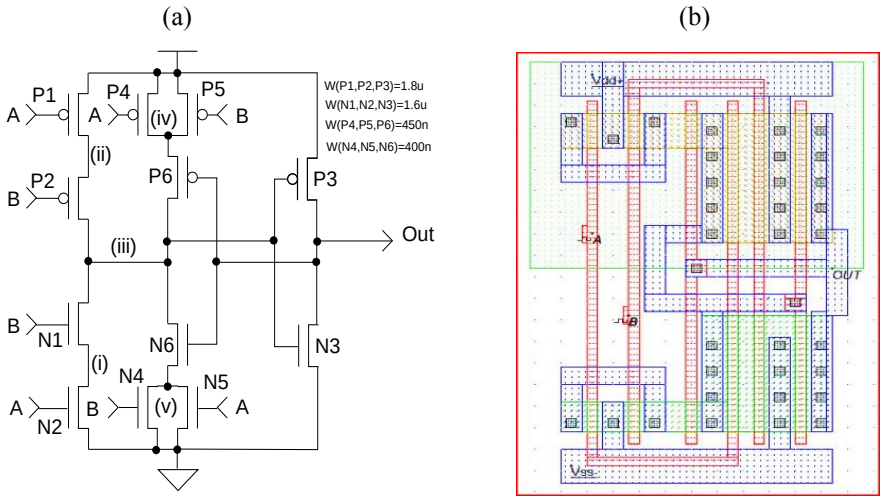

Figure 7. (a) Single Rail with conventional pull up and pull down; (b) Layout of single rail with conventional pull up and pull down

In order to calculate the soft error a method is proposed as below. For simplicity, an injected current that resemble SEU is assumed to have trapezoidal shape with width (t_w), fast rising time (t_r), slow falling time (t_f) and an amplitude Amp_i. Let Amp_1 be an amplitude of injected pulse in such a way that produce Out(t) ≥ 0.2 and Amp_2 is the amplitude of injected pulse that cause the output to corrupt or change the state to change. Since the generated pulse directly proportion with the ratio of the injected charge that produced Out(t) ≥ 0.2, ($Q_{injected}$), with the injected charge that cause the state to change $Q_{state\text{-}change}$, the mathematical expressions are derived to describe the response of the state holders as illustrated above, and to show whether the state is corrupted or not depended on the polarity of the current source. The positive polarity of current on n-type drain can cause the state to change from 1-0-1. The negative polarity on n-type drain can only reinforce logic state 1 [8]. Therefore, by taking into consideration the polarity of current, a constant 1/2 is added to the response equation to indicate that there are 50% chances of current to cause SEU. The response of the state holder equations is given by (1) – (3).

$$R_i(Amp_i) = \begin{bmatrix} 0 & Amp_i < Amp_1 \\ \frac{1}{2}\frac{Q_{injected}}{Q_{state-change}} & Amp_1 \le Amp_i \le Amp_2 \\ 0.5 & Amp_i > Amp_2 \end{bmatrix} \quad (1)$$

$$R_i(Amp_i) = \begin{bmatrix} 0 & Amp_i < Amp_1 \\ \frac{1}{2}\frac{0.5*(t_r+t_f)*Amp_i+Amp_i*t_w}{0.5*(t_r+t_f)*Amp_2+Amp_2*t_w} & Amp_1 \le Amp_i \le Amp_2 \\ 0.5 & Amp_i > Amp_2 \end{bmatrix} \quad (2)$$

$$R_i(Amp_i) = \begin{bmatrix} 0 & Amp_i < Amp_1 \\ \frac{1}{2}\frac{Amp_i}{Amp_2} & Amp_1 \le Amp_i \le Amp_2 \\ 0.5 & Amp_i > Amp_2 \end{bmatrix} \quad (3)$$

We defined the following terms to illustrate the sensitive area of n/p-type drain of different C-elements implementations:

(a) $A_{n,SIL}^{(i)}$ The area of sensitive n-type drain area of SIL at node (i)
(b) $A_{p,SIL}^{(ii)}$ The area of sensitive p-type drain area of SIL at node (ii)
(c) $A_{p,SIL}^{(iii)}$ The area of sensitive p-type drain area of SIL at node (iii)
(d) $A_{n,SIL}^{(iii)}$ The area of sensitive n-type drain area of SIL at node (iii)
(e) $A_{n,SC}^{(i)}$ The area of sensitive n-type drain area of SC at node (i)
(f) $A_{p,SC}^{(ii)}$ The area of sensitive p-type drain area of SC at node (ii)
(g) $A_{p,SC}^{(iii)}$ The area of sensitive p-type drain area of SC at node (iii)
(h) $A_{n,SC}^{(iii)}$ The area of sensitive n-type drain area of SC at node (iii)

The total areas of vulnerable $A_{vulnerable}$ nodes of different configurations of C-elements are the sum of the drain of p-type and n-type, which are given by (4) and (5).

$$A_{vulnerable(SIL)} = A_{n,SIL}^{(i)} + A_{p,SIL}^{(ii)} + A_{p,SIL}^{(iii)} + A_{n,SIL}^{(iii)} \quad (4)$$

$$A_{vulnerable(SC)} = A_{n,SC}^{(i)} + A_{p,SC}^{(ii)} + A_{P2,SC}^{(iii)} + A_{P6,SC}^{(iii)} A_{N1,SC}^{(iii)} + A_{N6,SC}^{(iii)} \quad (5)$$

Therefore, the probability of current that can hit the drain for any given nodes is given by Equation (6).

$$P_{n,p-node} = R_i(Amp_i) \times \frac{A_{n,p}^{(node)}}{A_{circuit}} \begin{cases} \text{node} = \text{node number (i) to (iii)} \\ \text{n, p} = \text{drain of NMOS or PMOS} \\ \text{circuit} = \text{SIL, SC} \end{cases} \quad (6)$$

Therefore, we can extend the above probability to find the probability of current that can hit for different implementation of C-elements is given by Equation (7) and (8).

$$P_{SIL} = \frac{1}{A_{SIL}}(A_{n,SIL}^{(i)} + A_{n,SIL}^{(ii)} + A_{p,SIL}^{(iii)} + A_{n,SIL}^{(iii)}) \quad (7)$$

$$P_{SC} = \frac{1}{A_{SC}}(A_{n,SC}^{(i)} + A_{n,SC}^{(ii)} + A_{p,SC}^{(iii)} + A_{n,SC}^{(iv)} + A_{p,SC}^{(v)} + A_{n,SC}^{(v)}) \quad (8)$$

where, A_{SIL}, A_{SC} are the total area of SIL, SC respectively. The number of events is reduced in quadratic with neutron energy. On a log-log plot of the number of event per energy, $\frac{dN}{dE}$ versus Energy (MeV), as shown in Figure 8 [9] can be approximated by a straight line for the interval of "1 – 100" MeV. The line can be used to predict the error rate of the state holders by neutron energy. Two parameters C_1 and C_2 can be extracted from the graph as follows:

1) Constant C_1 equals to the y-intersect of the straight line segment of the plot.
2) Constant C_2 is the slope of the straight line segment of the plot.

The straight line of spectrum density of neutron that is larger or equal to 1 MeV, $SD_{neutron>1MeV}$, can be modelled as in (9),

$$SD_{neutron>1MeV} = C_1 * E^{-C_2} \ \text{MeV}/cm^2/hr \quad (9)$$

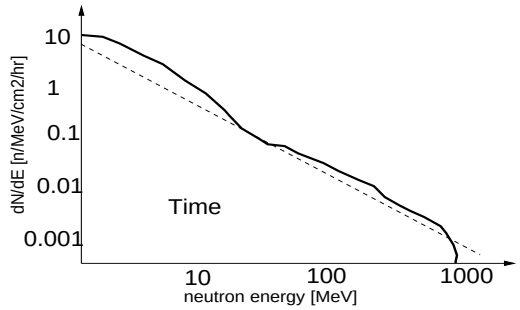

Figure 8. Neutron energy spectrum [9]

For spectrum density of neutron that is equal or smaller to 1 MeV, $SD_{neutron<1MeV}$, the equation can be approximated from Figure 9(a) by [10]. The simulations on four different configurations of C-elements show that the critical energy needed to cause 0.2 of input pulse or causing the state to change is lies between 0.15 MeV to 0.9 MeV. In other words, energy that is less than 1 MeV is sufficient to cause the output of C-element to change. This range is as shown by the red circle in Figure 9(a). The constant 3600 refers to the conversion of second to hour. The approximate equation of the line is given as,

1) Constant C_3 equals to the slope of the straight line segment.
2) Constant C_4 equals the y-intersect of the straight line segment.

$$SD_{neutron<1MeV} = 3600 * 10^{C_3E - C_4} \ \text{MeV}/cm^2/\text{hr} \quad (10)$$

The ratio of normalized atmospheric neutron cross section with the drain area of PMOS and NMOS with $0.1\ \mu m$ technologies for neutron energy is shown in Figure 9 (b) [11]. As the 90 nm-technology is used in the simulation, the ratio can be approximated by neutron cross section and drain cross section with $0.1\ \mu m$ technology. It is very obvious from the graph that NMOS transistor is more vulnerable towards SEU compared with PMOS transistor. Authors in [12] suggested that for the same transistor width, NMOS transistor is 2.2 times more sensitive compared with PMOS transistor. This is due to the collected charge for drain NMOS is higher for drain PMOS. The equations for normalized cross section of PMOS and NMOS straight-line for $0.1\ \mu m$ technology are given by (11) and (12).

$$nmos_{normalised} = 10^{(d_1Q + d_2)} \quad (11)$$

$$pmos_{normalised} = 10^{(e_1Q + e_2)} \quad (12)$$

where, $d_1, d_2, e_1$and e_2 are constants. Four parameters d_1, d_2,$e_1$and e_2 can be extracted from the graph of Figure 9(b) as follows:
1) Constant d_1 and e_1 equal to the slope of the straight line segment of nmos and pmos graph respectively.
2) Constant d_2 and e_2 equal the y-intersect of the straight line segment of nmos and pmos graph respectively.

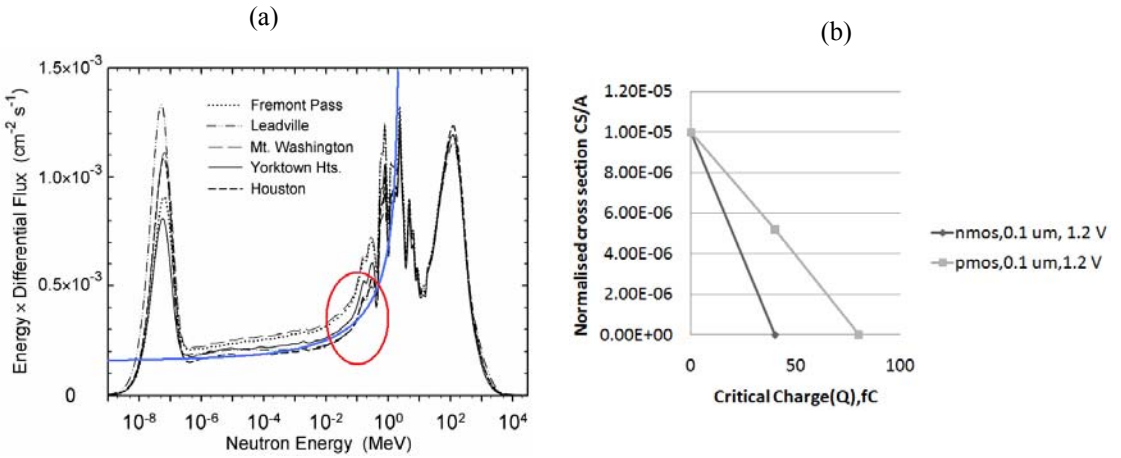

Figure 9. (a) Neutron spectrum below 1 MeV including thermal-energy [10]; (b) Normalized atmospheric neutron cross section [11]

The error rate of neutron spectrum energy that causes failure for any node of NMOS transistor for spectrum of energy more than 1 MeV in state holder is given by (13) and (14).

$$R_{n,node>1MeV} = P_{n-node} * (nmos_{normalised}) SD_{neutron>1MeV} * A_{vulnerable} \quad (13)$$

$$R_{n,node>1MeV} = R_i * (Amp_i) \frac{A_n^{(node)}}{A_{circuit}} * 10^{(d_1 Q + d_2)} * C_1 E^{-C_2} * A_{vulnerable} \quad (14)$$

Similarly, the error rate of neutron spectrum energy that cause failure for any node of NMOS transistor for spectrum of energy less than 1 MeV in state holder is given by equations (15) and (16).

$$R_{n,node<1\,MeV} = P_{n-node} * (nmos_{normalised}) * SD_{neutron<1MeV} * A_{vulnerable} \quad (15)$$

$$R_{n,node<1MeV} = R_i (Amp_i) * \frac{A_n^{(node)}}{A_{circuit}} * 10^{(d_1 Q + d_2)} * 3600 * 10^{C_3 E - C_4} * A_{vulnerable} \quad (16)$$

Equations (14) and (16) are added to calculate the total error rate of neutron spectrum energy that cause failure for any node of NMOS transistor is given by (17) and (18).

$$R_{Totaln} = R_{n,node<1MeV} + R_{n,node>1MeV} \quad (17)$$

$$R_{Totaln} = R_i (Amp_i) * \frac{A_n^{(node)}}{A_{circuit}} * 10^{(d_1 Q + d_2)} * C_1 E^{-C_2} * A_{vulnerable} + R_i (Amp_i) * \quad (18)$$
$$* \frac{A_n^{(node)}}{A_{circuit}} * 10^{(d_1 Q + d_2)} * 3600 * 10^{C_3 E - C_4} * A_{vulnerable}$$

The error rate of neutron spectrum energy that causes failure for any node of PMOS transistor for spectrum of energy more than 1 MeV in state holder is given by Equation (19).

$$R_{p,node>1MeV} = P_{p-node} * (pmos_{normalised}) * SD_{neutron>1MeV} * A_{vulnerable} \quad (19)$$

Equation (19) can be written as shown by (20). However, since energy that is less than 1 MeV only affect NMOS transistor [13], the total error rate of neutron spectrum energy that cause failure for any node of PMOS transistor is equal to Equation (21).

$$R_{p,node>1MeV} = R_i(Amp_i) * \frac{A_p^{(node)}}{A_{circuit}} * 10^{(e_1Q+e_2)} * C_1E^{-C_2} * A_{vulnerable} \quad (20)$$
$$R_{p,node<1MeV} = 0$$

$$R_{Totalp} = R_i(Amp_i) * \frac{A_p^{(node)}}{A_{circuit}} * 10^{(e_1Q+e_2)} * C_1E^{-C_2} * A_{vulnerable} \quad (21)$$

The probability can be extended in order to find the total probability due to the drain of NMOS or PMOS transistor of any given C-element circuit as shown by (22) – (25).

$$P_{n,SIL} = \frac{1}{A_{SIL}}\left(A_{n,SIL}^{(i)} + A_{n,SIL}^{(iii)}\right) \quad (22)$$

$$P_{p,SIL} = \frac{1}{A_{SIL}}\left(A_{p,SIL}^{(ii)} + A_{p,SIL}^{(iii)}\right) \quad (23)$$

$$P_{n,SC} = \frac{1}{A_{SC}}\left(A_{n,SC}^{(i)} + A_{n,SC}^{(iii)}\right) \quad (24)$$

$$P_{p,SC} = \frac{1}{A_{SC}}\left(A_{p,SC}^{(ii)} + A_{p,SC}^{(iii)}\right) \quad (25)$$

where, A_{SIL}, A_{SC} are the total area of SIL, SC respectively. The total probability of current pulse that can hit for NMOS and PMOS transistor in circuit are given by (26) and (27).

$$P_{n,total} = R_i(Amp_i) * (P_{p,circuit}) \quad (26)$$

$$P_{p,total} = R_i(Amp_i) * (P_{p,circuit}) \quad (27)$$

The total errors rate due to SEU of any configurations of C-elements are given by,

$$R_{Total} = Total\ error\ rate\ due\ to\ NMOS\ +\ Total\ error\ rate\ due\ to\ PMOS \quad (28, a)$$

$$R_{Total} = P_{n,total} * 10^{(d_1Q+d_2)} * C_1E^{-C_2} * A_{circuit} + P_{n,total} * 10^{(d_1Q+d_2)} * 3600 * 10^{C_3E-C_4} * A_{circuit} * P_{p,total} * 10^{(e_1Q+e_2)} * C_1E^{-C_2} * A_{circuit} \quad (28, b)$$

$$R_{Totalp} = R_i(Amp_i) * \frac{A_p^{(node)}}{A_{circuit}} * 10^{(e_1Q+e_2)} * C_1E^{-C_2} * A_{vulnerable} \quad (29)$$

In order to verify the proposed technique, we have generated a random width of current injected into different types of C-element. A Monte-Carlo analysis was used to generate random sample with the number of samples were fixed at 1000. The error rate for both SIL and SC are calculated by using the method shown above.

As shown in Figure 10, the error rates for SIL increase with the increase of temperature due to the degradation of the mobility carrier. Therefore, these nodes are more vulnerable to SEU at high temperature. The error rates of 0-1 change increase by 29.1% and the error rates of 1-0 change increase by 132% by increasing the temperature from -40^oC to 100^oC. From the increment of critical charge, it is concluded that the PMOS transistors had greater effect on temperature variation compared with NMOS. Similarly for SC, the error rates of 0-1 change increase by 14.2% and the error rates of 1-0 change increase by 73.9% when increasing the temperature from -40^oC to 100^oC as seen in Figure 11.

To identify which implementations are more resistant towards soft error at different transition, the error rates from Figures 10 and 11 are added for the same C-element. Figure 12 (a, b) shows the total error rate of neutron spectrum energy for 1-0 and 0-1 on different C-elements respectively. We could conclude that SIL implementations are more resistant toward soft error compared with SC.

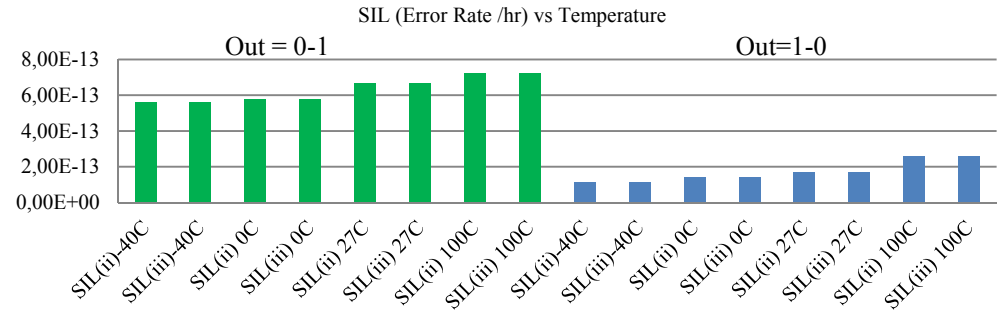

Figure 10. Error rate due to neutron energy spectrum with respect to temperature SIL

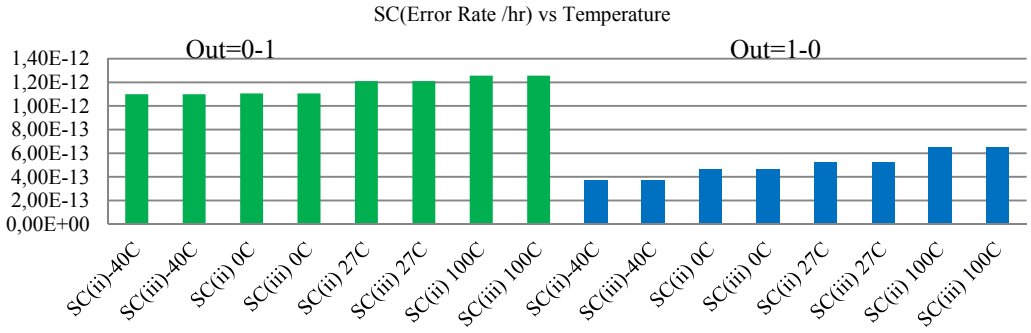

Figure 11. Error rate due to neutron energy spectrum with respect to temperature SC

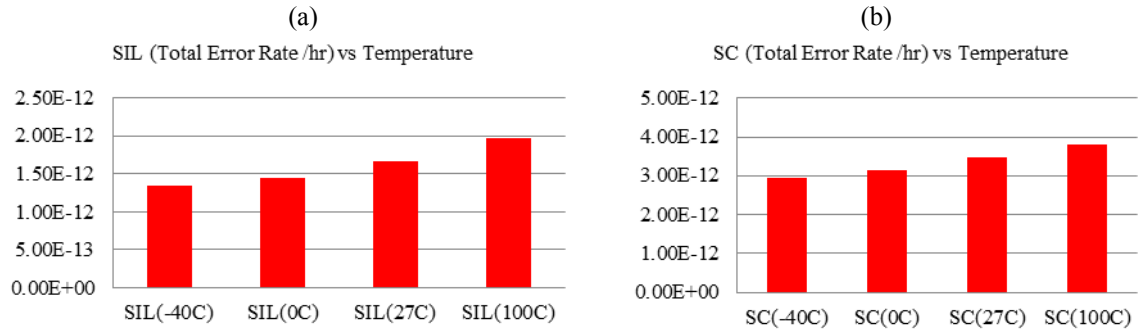

Figure 12. (a) Total error rate due to neutron energy spectrum with respect to temperature SIL; (b) Total trror rate due to neutron energy spectrum with respect to temperature SC

4. CONCLUSION

In this paper, we have injected error on SIL configuration of C-Elements. As the technology is scaled down, the transistors are very vulnerable to soft error and this has been affirmed from the experiments that we had performed on SIL. We developed a method to calculate the error rate due to neutron energy spectrum. This method can be used to assess the vulnerability of soft error towards different memory circuit configurations. The presented calculation indicates that SIL implementations are more resistant toward soft error compared with SC. Future work will be focusing on the incorporation of sensor technology within electronic circuits by considering different aspects as in [14-16].

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