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Analysis the Effect of Control Factors Optimization on the Threshold Voltage of 18 nm PMOS Using L27 Taguchi Method

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ABSTRACT

This research paper is about the investigation of Halo Implantation, Halo Implantation Energy, Halo Tilt, Compensation Implantation and Source/Drain Implantation. They are types of control factors that used in achievement of the threshold voltage value. To support the successfully of the threshold voltage (VTH) producing, Taguchi method by using L27 orthogonal array was used to optimize the control factors variation. This analysis has involved with 2 main factors which are break down into five control factors and two noise factors. The five control factors were varied with three levels of each and the two noise factors were varied with two levels of each in 27 experiments. In Taguchi method, the statistics data of 18 nm PMOS transistor are from the signal noise ratio (SNR) with nominal-the best (NTB) and the analysis of variance (ANOVA) are executed to minimize the variance of threshold voltage. This experiment implanted by using Virtual Wafer Fabrication SILVACO software which is to design and fabricate the transistor device. Experimental results revealed that the optimization method is achieved to perform the threshold voltage value with least variance and the percent, which is only 2.16%. The threshold voltage value from the experiment shows -0.308517 volts while the target value that is -0.302 volts from value of International Technology Roadmap of semiconductor, ITRS 2012. The threshold voltage value for 18 nm PMOS transistor is well within the range of -0.302 ± 12.7% volts that is recommendation by the International Roadmap for Semiconductor prediction 2012.

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1. INTRODUCTION

From time to time, the semiconductor industries throughout the world with collaboration with researches do many works to upgrade the quality and performance of MOSFET. This achievement is provided the better performance electronics to users. Advancement in technology allows the size of MOSFETs design become smaller and increase the switching speed. Capacitance indicates switching speed of the MOSFET. Due to our necessary to compact the Integrated Circuit as possible as we can for getting small electronics devices [1]. Scaling down the size of transistor is not an easy job as it requires higher transistor drive current, higher integration density and faster switching speeds [2]. The main aim behind scaling down MOSFETs geometry is to create a faster switching speed at a lower production cost.

The scaling down the transistors will bring great effects on the reliability of integrated circuit and manufacturing cost. However, the problems will arise to the short channel effects such as leakage current where the leakage current is the main issues for static power dissipation in standby mode as the size of transistor been scale. Therefore, the subthreshold leakage current rises due to threshold voltage scaling and gate leakage current increases due to scale down of oxide thickness [3]. The subthreshold swing is increasing due to tunneling current and that the performance of nano scaled MOSFETs is degraded. It is shown that the degradation of subthreshold swing increases with both reduction of channel length and increase of channel thickness [4]. While the size of MOSFETs is reducing, the atoms count inside the silicon which affects the production of transistors properties is reducing as well. This will result inconsistent placements and number of controlled dopant [5]. Semiconductor process is uncontrolled causing the process variables to have statistical variation. In order to reduce the influence of variations, the manufacturer is using the bigger scaled physical gate length for memory applications purposes. The downscaling on length gate is something that cannot be avoided and it will be expected to continue in the coming years. This is due to the inability of control factors to track scaling of minimum feature sizes.

In advance process control, random variations is expected to increase due to minimization of systematic shifts in the critical dimension. This will lead to variation in impact of the overall power dissipation and performances [6]. Statistical design is now becoming more important because of the random variations. The statistical design which includes process variation parameters has become the great effect in circuit design as it causing huge effect in the MOS transistor. All of these transistors need to undergo optimization process to guarantee a quality outcome which to improve the performance of CMOS. The optimization process is always being continued throughout these decade to ensure user satisfaction in using electronic devices. The technique of optimization explained in this paper is focus on the control factor which will give effect in the threshold voltage. In this era, the Taguchi method has becoming one of the powerful tools used to improve productivity during the research and development process. Thus, it is possible to produce a higher quality of products at a lower cost and in the shorter time [7]. While designing the devices by using a deep sub-micron technology and analyze the variability, it had grown to become a very important tool. This will allow prediction of the response in the very early stage; just from the control factor itself.

The Taguchi method involving analysis of control factor in which of the factors should be manipulated and finely adjusted to produce an improvement of results. The optimization for the control factor is the heart of Taguchi method as the quality can be improved while maintaining its development cost. The reason is the processes are insensitive to variation of environmental conditions and other noise factor. This method solves the problem with the specially designed orthogonal arrays that are used to analyze every control factor in small experiment number. By using an orthogonal array, these could help designers to find out multiple manipulated factors on each characteristic and faster variation in a more economical way [8].

2. RESEARCH METHOD

2.1. Simulation of the Fabrication

Athena module from VWF was used to fabricate the 18nm PMOS nanostructured. The first step in fabrication is a creating the initial substrate from a Silicon p type (boron doped) with a doping 7 x 10^{14} atoms/cm^3 and orientation <100>. Next process is to generate retrograde N-well by growing a dry oxygen 200 Å on the top of the substrate for 20 minutes with 970ºC and doped with Phosphorous. The dose is 3.75 x 10^{12} atoms /cm^3 and energy implantation is 100KeV. The next step is to form the Shallow Trench Isolation (STI) of 130-Å thickness in annealing process with dry Oxygen in 25 minutes at 900ºC. In this procedure, the Low Pressure Chemical Vapor Deposition process (LPCVD) and Reactive Ion Etching (RIE) process were applied and involved to achieve the making of the desired depth STI. Then, Phosphor Silicate Glass (PSG) was developed on top of substrate after wafer is undergoing the annealing process at 850ºC for 15 minutes. After complete the process of growing and annealed 1.1 nm Gate Oxide Thickness (TOX), the Boron Di-fluoride (BF2) with 1.6757777 x 10^7 atoms /cm^3 Boron and the energy 5KeV with a tilt angle of 7º was implanted at the N-well active. Followed by deposition process of insulator that is Hafnium dioxide (dielectric permittivity HfO2, εopt = 22) on top of bulk Silicon. In this research the length of HfO2 material was 18nm. Then, on the top of the insulator was the deposition process of gate material, Titanium Silicide (TiSi2). The PMOS device, Phosphorous with dose 5.581 x10^{13} atoms /cm^3 at 30° angle and energy, 290KeV was used in Halo Implantation process. The chemical vapor deposition (CVD) process was used to develop side wall spacer with a 0.047µm Silicon Nitride layer. Again, Boron with density of 5.556666 x 10^{13} atoms/cm^3 and tilted at 7° with 11KeV implantation energy was used in Source/Drain Implantation process. Next process is to develop a 0.3µm layer of Boron Phosphor Silicate Glass (BPSG) and followed by the annealing process of structure at 850ºC. The last implantation process is Compensation Implantation with Phosphorous dose of 2.5 x 10^{13} atoms /cm^3 at 60KeV energy and angle tilted at 7°. Last but not least, the

process of deposition the Aluminum material on top of the structure and etching accordingly to form metal contacts for Source and Drain [9], [10]. The complete diagram of 18nm structure as shown in Figure 1.

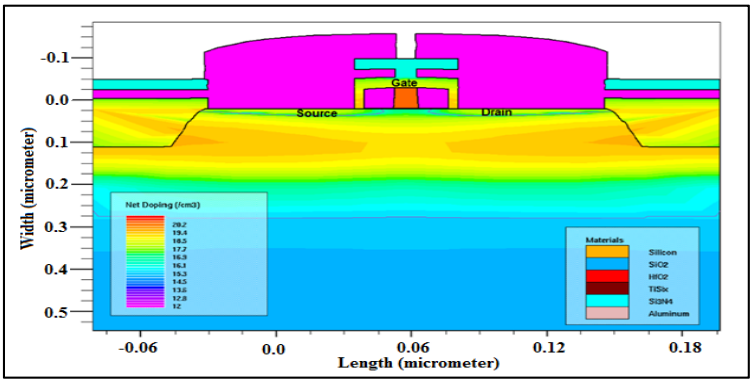

Figure 1. A doping profile of the 18 nm gate length of PMOS transistor

2.2. Taguchi L27 Orthogonal Array Method

The designing of 18nm PMOS device is completed by using SILVACO simulation. Next, the statistical of analysis process for parameters device by using Taguchi method. In this section, Taguchi method is used to study the control factor effects at the threshold voltage (VTH). The orthogonal array L27 in Taguchi method is used to optimize the control factors intended to consider the impact of the interaction. The important of the interaction study is to identify which control factor has interaction with the key factor during the optimization process is carried out. The key factor (factor E) is selected from optimization process using orthogonal array L9 Taguchi method [11]. This is because the experimental study of Taguchi method with orthogonal array L9 only shows the dominant factor and adjustment factors without showing the impact of the interaction. The key factor is the dominant factor from array L9 Taguchi.

In this research, the optimization process by using orthogonal array L27 Taguchi method needs only five important control factors to be considered in the design of experiments with interaction. In the previous experiment, which studies the process by using an orthogonal array L9 it can be conclude that the Source/Drain Implantation is selected as dominant factor [11]. So this study proves that the Source/Drain implantation dose is as factor E. So in the orthogonal arrays L27 study, it aimed to investigate the relationship of interaction factor E with other control factors. Many experiments were done to select the suitable five control factors and noise factors. The study of interactions involving dose of Source/Drain Implantation (factor E) are considered interacting with dose of Halo Implantation (factor A), dose of Halo Energy Implantation (factor B), Halo Tilt (Factor C) and dose of Compensation Implantation (Factor D) as shown in Table 1. While the noise factors are Phosphor Silicate Glass (BPS) temperature and Boron Phosphor Silicate Glass (BPSG) temperature at different levels aimed to give more sensitivity to changes in factors also listed in Table 2.

Table 1. Control Factors and their ranges

Symbol	Control Factor	Unit	Level 1	Level 2	Level 3
A	Halo Implantation	atom/cm^3	5.595000e13 [A1]	5.600000e13 [A2]	5.605000e13 [A3]
B	Halo Energy Implantation	KeV	294 [B1]	295 [B2]	296 [B3]
C	Halo Tilt	°C	30 [C1]	32 [C2]	34 [C3]
D	Compensation Implantation	atom/cm^3	14.871000e13 [D1]	14.875000e13 [D2]	14.879000e13 [D3]
E	Source-Drain Implantation	atom/cm^3	5.394000e13 [E1]	5.400000e13 [E2]	5.406000e13 [E3]

Table 2. Noise Factor and its ranges

Symbol	Noise factor	unit	Level 1	Level 2
X	PSG Temperature	°C	850 [X1]	851 [X2]
Y	BPSG Temperature	°C	850 [Y1]	851 [Y2]

3. RESULTS AND ANALYSIS

3.1. Analysis of 18nm PMOS Device

Taguchi L27 orthogonal array estimates twenty seven experiments with one hundred and eight simulations run between the combination five control factors and two noise factors. The design value of 18nm PMOS threshold voltage is -0.302 ± 12.7% Volts. This value is referred to International Roadmap of Semiconductor (ITRS) 2012 [12]. That mean the threshold voltage (VTH) is in Nominal-the-Better (NTB) quality Taguchi's categories. Based on the control parameters listed in Table 1 with a combination of noise factors in Table 2, the design optimization process is carried out referring to the PMOS transistor arrays combination L27 Taguchi method and the results of the analysis VTH listed in Table 3. The reading for VTH is between -0.89278 to -0.127719 Volts. It takes 8 hours and 64minutes to complete the simulation.

Table 3. 18nm PMOS Statistical Result-Taguchi L27 Orthogonal Array

Exp.No	Threshold voltage X_1Y_1	Threshold voltage X_1Y_1	Threshold voltage X_1Y_1	Threshold voltage X_1Y_1	Mean	Variance	SNR (Nominal-the Better),η dB
1	-0.29829	-0.27788	-0.28759	-0.27591	-0.285	1.06E-04	28.86
2	-0.24944	-0.23777	-0.24747	-0.23581	-0.243	4.66E-05	31.01
3	-0.23932	-0.22767	-0.23735	-0.22569	-0.233	4.66E-05	30.64
4	-0.33395	-0.32700	-0.33280	-0.32560	-0.330	1.72E-05	38.00
5	-0.32859	-0.31718	-0.32696	-0.31513	-0.322	4.61E-05	33.52
6	-0.31853	-0.30690	-0.31647	-0.30489	-0.312	4.63E-05	33.22
7	-0.75252	-0.89278	-0.47339	-0.82500	-0.736	3.39E02	12.03
8	-0.89144	-0.69478	-0.82431	-0.67680	-0.772	1.07E-02	17.47
9	-0.69536	-0.61845	-0.67749	-0.60683	-0.650	1.89E-03	23.49
10	-0.29134	-0.28005	-0.28936	-0.27809	-0.285	4.37E-05	32.68
11	-0.28134	-0.27015	-0.27938	-0.26821	-0.275	4.30E-05	32.45
12	-0.27143	-0.26031	-0.26949	-0.25838	-0.265	4.24E-05	32.19
13	-0.43722	-0.41947	-0.43357	-0.41629	-0.427	1.06E-04	32.34
14	-0.42103	-0.40225	-0.41785	-0.40058	-0.410	1.10E-04	31.83
15	-0.40694	-0.39309	-0.40414	-0.39066	-0.399	6.45E-05	33.91
16	-0.36410	-0.35455	-0.36284	-0.35235	-0.358	3.45E-05	35.71
17	-0.35631	-0.34344	-0.35411	-0.34129	-0.349	5.66E-05	33.32
18	-0.34518	-0.33257	-0.34303	-0.33048	-0.338	5.43E-05	33.23
19	-0.12772	-0.13232	-0.12919	-0.13377	-0.131	7.74E-06	33.44
20	-0.13158	-0.13609	-0.13330	-0.13748	-0.135	7.12E-06	34.06
21	-0.13530	-0.14855	-0.13998	-0.15360	-0.144	6.81E-05	24.86
22	-0.29751	-0.28559	-0.29549	-0.28360	-0.291	4.86E-05	32.40
23	-0.28721	-0.27538	-0.28521	-0.27340	-0.280	4.79E-05	32.15
24	-0.27699	-0.26218	-0.27500	-0.26324	-0.269	5.97E-05	30.85
25	-0.35178	-0.34402	-0.35048	-0.34278	-0.347	2.05E-05	37.70
26	-0.34568	-0.32382	-0.34444	-0.32037	-0.334	1.78E-04	27.96
27	-0.33987	-0.33270	-0.33777	-0.33022	-0.335	1.98E-05	37.53

From the threshold voltage values, the data of mean (μ), variance (σ^2) and Signal-to-Noise (SNR) Nominal-the-Better (η_{NTB}) can be calculated by using the formulas below [13]:

$$\text{SNR (NTB)}, \eta_{NTB} = 10 \text{ Log}_{10} \left[\frac{\mu^2}{\sigma^2} \right] \quad (1)$$

Where:

$$\text{Mean, } \mu = \frac{Y_i + \ldots\ldots + Y_n}{n} \quad (2)$$

$$\text{Variance, } \sigma^2 = \frac{\sum_{i=1}^{n}(Y_i - \mu)^2}{n-1} \quad (3)$$

Based on the equations, n is the number of tests, Y is the experimental value of the VTH. The equation (2) and equation (3) are the formulas to calculate mean values and variance values respectively. By applying the both formulas in equation (3), the SNR (NTB), η_{NTB} for the PMOS device was calculated and the results were also listed in Table 3.

Based on the results obtained in Table 3, next part is to determine the control parameters that affect to the changing of the characteristics of the device with display the highest SNR value of each level. SNR (NTB) for each level of control parameters is shown in Table 4.

Table 4. Result of SNR (NTB), η Control Factors

Factor	Control Factor	SNR (NTB),dB Level 1 [A1, B1, C1, D1,E1]	Level 2 [A2, B2, C2, D2,E2]	Level 3 [A3, B3, C3, D3,E3]	Overall SNR (NTB), dB
A	Halo Implantation	27.58	33.07	32.33	
B	Halo Energy Implantation	31.13	33.14	28.72	
C	Halo Tilt	32.02	33.92	27.05	31.00
D	Compensation Implantation	32.42	33.26	27.30	
E	Source/Drain Implantation	31.46	30.42	31.10	

Through this information, the dominating factor can be determined in the factor A, factor B, factor C, factor D and factor E during the process variability is carried out and it can be selected for the verification process to the end. Refer to Table 4, the highest value of each control factor in the text indicates that the level of this parameter is the highest of SNR (NTB), this means the better quality of threshold voltage, VTH [14]. So it can be observed in factor A, showed that the level A2 of Halo implantation dose with a value of 33.07 dB SNR can be considered as dominating as the highest level of noise generated compared with level A1 and level A3. Factor B2 of Halo Energy implantation dose and factor C2 of Halo Tilt which respectively show the highest values of SNR with 33.14 dB and 33.92 dB. While Factor D shows the level 2 is the highest value of 33.26 dB and lastly factor E indicates the level 3 is the highest value of 31.10 dB. The average values of SNR (NTB) data is 31.00 dB and the evaluation result without interactions process is A2 B2 C2 D2 E1.

3.1. Analysis of ANOVA Result with Interaction

This research was studying the effects of interactions (EXA), (EXB), (EXC) and (EXD) in determination of the optimal combination of control factors. The aim is to calculate the average value of the interaction of Factor E that is Source/ Drain Implantation (E1, E2, E3) with other factors such as Halo Implantation (A1, A2, A3), Halo Energy Implantation (B1, B2, B3), Halo Tilt (C1, C2, C3), and Compensation Implantation (D1, D2, D3). Then, all the data were transfer to the graphs and study the interaction. The graphs of the relationship between control factors to SNR (NTB) can be plotted and shown in Figure 6, Figure 7, Figure 8 and Figure 9. The presence of interaction through graphs can be observed by the existence of lines that intersect and inconsistency among the factors involved. Figure 6, Figure 7, Figure 8 and Figure 9 respectively show the relationship between interaction E (EXA), (EXB), (EXC) and (EXD).

Figure 6 shows the SNR (NTB) values for graph interaction between Halo Implantation (factor A) and Source/Drain Implantation (factor E). There are 3 lines show on the graph, which are A1, A2 and A3, which are intersect with E level, E1, E2 and E3. From that, it can be seen as crossing the 2 lines plot in between A2 and A3 only. But A1 level crossing does not exist. So determined the highest SNR (NTB) level on lines that intersect with E1 parameter is A3 (34.51 dB).

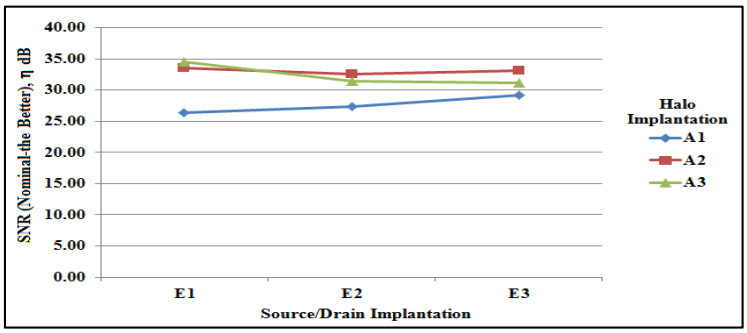

Figure 6. The interaction between Source/Drain Implantation and Halo Implantation

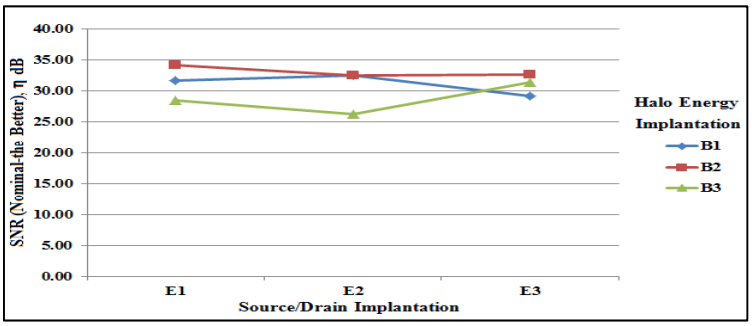

Figure 7. The interaction between Source/Drain Implantation and Halo Energy Implantation

Figure 7 is the interaction graph for SNR (NTB) between Halo Implantation (factor B) with Source/Drain Implantation (factor E). There are 3 lines which are B1, B2 and B3 are plotting on the graph, where they are intersect with level E1, E2 and E3. From that, 2 lines are crossing to each other. Line B1 is crossed with line B2 at E2 level and line B1 is crossed with line B3 at E3 level. Refer to the graph, the highest SNR (NTB) level that intersection with E2 parameter is B2 (34.25 dB).

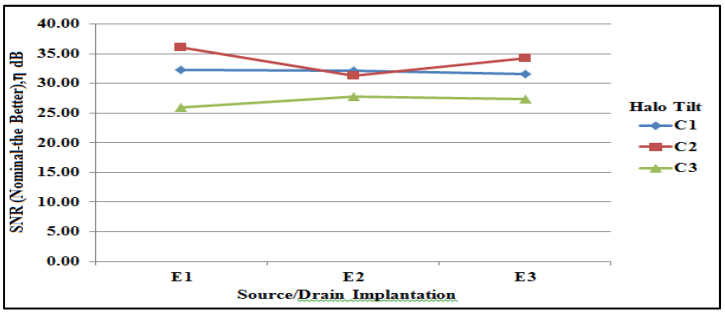

Figure 8. The interaction between Source/ Drain Implantation and Halo Tilt

Figure 8 shows the interaction result between Halo Tilt (factor C) and Source/Drain Implantation (factor E). Graph from Figure 8 is same with graph from Figure 6, only 2 lines that is C1 line is crossed with C2 line. While C3 line is crossing does not exist. Result shows the higher value of SNR (NTB) of Halo Tilt is interaction with Source /Drain implantation is C2 with 36.13 dB.

Figure 9 shows the SNR (NTB) interaction between Compensation Implantation (factor D) and Source/Drain Implantation (factor E). The graph displays the 2 lines are crossing to each other. The highest value of SNR (NTB) for Compensation Implantation is D2 with 35.72 dB.

Based on information analysis performed, the optimum combination for PMOS devices VTH analysis that takes into account the effect of interaction is A3, B2, C2, D2, E1.

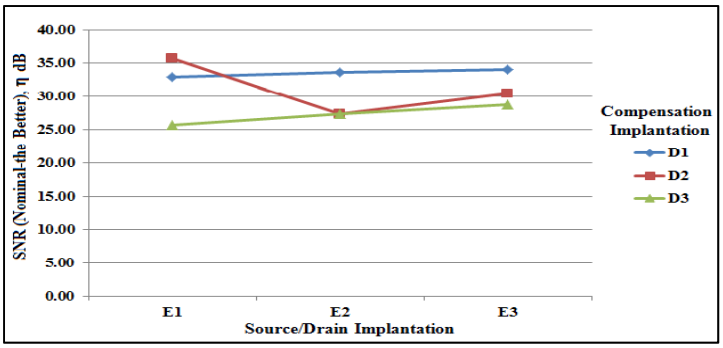

Figure 9. The interaction between Source/Drain Implantation and Compensation Implantation

3.2. Confirmation Test

The end of the simulation with the noise factor of the final test verification should be carried out to verify the accuracy of the forecast Taguchi method. The combination of optimum control factors (A3, B2, C2, D2, E1) listed in Table 5.

Table 5. Combination of optimum L27 analysis for 18nm PMOS

Symbol	Control factor	Unit	Level	Best Value
A	Halo Implantation	atom/cm³	3	5.605000e13
B	Halo Implantation Energy	keV	2	295
C	Halo Tilt	°C	2	32
D	Compensation Implantation	atom/cm³	2	14.875000e13
E	Source-Drain Implantation	atom/cm³	1	5.394000e13

While the final verification decision with noise factor and combination of optimum control factors for the analysis of arrays L27 Taguchi methods for threshold voltage, VTH with value -0.308517 volts.

Table 6 shows the lists of the percentage difference between the results of the combination without the interaction and combination with interaction during device optimization process is carried out, which it refers to the nominal value projected by ITRS 2012. The final decision analysis methods in designing model L27 Taguchi 18 nm PMOS device shows that the two experiments in which the interaction or without interaction take effect of VTH value within the range of the nominal value (-0.302 ± 12.7% volts).

However, the percentage of the experiment that takes into account the effect of the interaction is better than nominal values without taking interaction with 2.16%. Analysis shows that the key factor or factor E in this study, Source/Drain Implantation dosage factor had interaction with other control factors.

Table 6. Analysis of Percentage Threshold Voltage, VTH 18nm PMOS

	Before Interaction	After Interaction	ITRS value
Noise Factor (°C)	X2,Y2	X2,Y2	-0.302 ± 12.7% volts
Combination of optimum factors	A2, B2, C2, D2, E1	A3, B2, C2, D2, E1	
Threshold voltage, VTH	-0.317885 volts	-0.308517 volts	
Percentage from nominal value	5.26%	2.16%	

4. CONCLUSION

In the present study proves that, the control factors effects the threshold voltage, VTH of 18 nm PMOS transistor was successful found together with the optimal factors level predicted by Taguchi method. Source/Drain Implantation dosage factor has been identified as key factor had interaction with other control factors such as Halo Implantation, Halo Implantation Energy, Halo Tilt and Compensation Implantation. Therefore, it has been proven that 18nm transistor can be achieved produced the VTH value is well within the ITRS 2012 requirements of -0.302 ± 12.7% volts.

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