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A Comprehensive Review of Applications of Don't Care Bit Filling Techniques for Test Power Reduction in Digital VLSI Systems

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ABSTRACT

Massive power consumption during VLSI testing is a serious threat to reliability concerns of ubiquitous silicon industry. Many low-power methodologies are found in the technical literature to address this issue of test mode high power consumption and don't care bit(X) filling approaches are one of them in this fraternity. These don't care(X) bit filling techniques have drawn the significant attention of industry and academia for its higher compatibility with existing design flow as neither modification of the CUT is required nor they need to rerun the time-consuming ATPG process. This paper presents a comprehensive review of the applications of don't care bit filling techniques for mitigating prime two concerns of dynamic power dissipation namely shift power and capture power, occurred during full scan testing.

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1. INTRODUCTION

The testing phenomenon in silicon industry is known for its overrated power consumption and this remains unaltered in case of scan testing. This test mode high power consumption is potent enough for damaging the chip or even may become a reason for power-induced test yield loss. As a result, significant research attention was focused towards finding suitable low-power testing strategies. The two prime variants of test power during scan test are shift power (i.e., the power consumed during the scan shifting operations) and capture power (i.e., the power consumed during the response capture cycle).

Increase in switching activity occurred during the shifting of test data into the scan chain is viewed as a major shortcoming of scan-based test scheme. Reduction in the number of scan cell's signal transitions is a familiar approach to reduce the power dissipation during scan-based testing and may be classified into three categories:

a) Difference between the adjacent scan cells' values, while the test stimulus is loaded into the scan-chain, is termed as the scan-in transitions.
b) Difference amid the test stimuli and its response of the same scan cells is termed as capture transitions
c) While unloading the responses in scan-out mode, the difference between the adjacent scan cells' values are known as scan-out transitions

Scan-shift-power is related to first and third category and needs to be minimized in order to apply higher shift frequency for reducing the testing time and cost. The capture-power relates to the second category. The test mode capture-power should be kept smaller than peak-power threshold of CUT to avoid the cropping up of ICs damaging excessive heat. Moreover, higher switching activity originates from

simultaneous testing of multiple cores and test compaction. Adversely, hot spots may be developed increased from excessive switching activity during scan shift that may damage the silicon, the bonding wires, and even the package

1.1. Background

Power-aware strategy for filling of don't care(X) bits of the test cube during scan testing are generally made to be exploited for either shift power reduction or capture power reduction or even both of them. During scan testing, don't care(X) bits can be effectively replaced in order to lower down the toggling activity up to the desired level. Efficient filling of don't care bits may lead to significant reduction in test power consumption. Well known X-filling techniques such as 0-fill, 1-fill, minimum transition-fill and adjacent-fill have shown a notable reduction in average/peak power during scan shifting or during launch to capture. The fundamental merit of low-power don't care bit filling technique is that it can neither results in area overhead nor degrades performance.

1.2. Problem

The issue of excessive test power has turned out to be more terrible with the boundless utilization of at-speed scan testing, which is currently obligatory for performance verification. Regardless of the testing strategy utilized, the issue of excessive power amid testing can be part into two sub problems i) Excessive power during shift cycle ii) Excessive power during Launch-To- Capture (LTC) cycle. This is well reported that switching tasks of a circuit dependably prompt heat dissemination. On the off chance that the circuit temperature is too high notwithstanding amid a brief term of on-line test session it might have the accompanying circuit related issues such as chip damage, lower reliability, low test throughput and yield loss.

1.3. Analytical contribution

This paper introduces a comprehensive survey on the uses of don't care bit filling methods for moderating prime two concerns of dynamic power dissipation to be specific shift power and capture power, happened amid full scan testing. In this paper, we have identified and analyzed the merits and shortcomings of various test power reduction techniques based on don't care bit filling and the variants of test power covered in our analysis include shift power and capture power. Besides these two variants of test power, there are some test power reduction techniques which reduce both shift and capture power and we have identified their merits and shortcomings also. The most significant aspect of this analytical work lies in the fact that we have drawn a relative performance comparison among these don't care bit filling techniques and this comparison is based on the % of test power reduction on the given benchmark circuit corresponding to a particular filling technique.

2. TEST POWER AT A GLANCE

2.1. Variants of Test Power

At-speed tests are widely recognized by the industry as it aids to uncover timing-speed-related and even un-modelled defects of the CUTs. At-speed tests typically entail longer low-frequency shift phase and a short capture phase. Test data are usually loaded into scan chains at a lower frequency in order to maintain CUT's power constraint and also to reduce shift power. Although, high test cost might have to be incurred for this type of strategy. Best possible reduction in the CUT's shift-power dissipation facilitates higher shift frequency to provide test parallelism yielding reduced testing time. Invalidation of test results may arise due to IR-drop and/or ground bounce effects triggered by excessive at-speed transitions during the capture phase. Hence, containment of capture-power dissipation under the CUT's peak power constraint becomes inevitable.

2.2. Metrics of Power Estimation

The major fraction of power is dissipated in a CMOS circuit when switching elements switch from logic 0 to 1 or vice versa. Switching elements will make transitions only in the event of either the primary inputs alter value or the scan cells change values. Sankaralingam et al. (2000) [1] showed that the total power consumption in scan-based testing is not only based on the number of transitions in test set but also on the relative position of where the transition occurs. One common metric weighted transitions metric (WTM) is used to estimate the test power. The metric is strongly associated with the switching activity in the internal nodes of CUT during scan-shift operation. It was experimentally shown by Sankaralingam et al. (2000) [1] that higher value of WTM corresponding to scan vectors results in more power dissipation in CUT. The WTM for the scan-in test stimuli can be computed by:

$$WTM_j = \sum_{i=1}^{l-1} (l-i)(t_{j,i} \oplus t_{j,i+1}) \quad (1)$$

Where the scan-chain length is denoted by and a scan vector with scanned in before and so on. Scan in average shift power, and peak power for a test set can be estimated as follows

$$P_{ave} = \frac{\sum_{j=1}^{m} \sum_{i=1}^{l-1} (l-i)(t_{j,i} \oplus t_{j,i+1})}{n} \quad (2)$$

$$p_{peak} = \max_{j \in (1,2,3,\ldots,n)} \sum_{i=1}^{l-1} (l-i)(t_{j,i} \oplus t_{j,i+1}) \quad (3)$$

Equations 2 and 3 show that reducing the test vectors' transition and the weight (l-i) are the key factors for reducing the average and peak power. The same equations can be used to estimate also the average and peak-powers in scan-out mode.

We consider the number of transitions in scan cells for each scan-chain to compute the capture-power. This is because of the linear relationship exists between capture transitions on the scan-chain and peak-power of the circuit. So, it is attempted to minimize the Hamming distance between test stimuli and its response on each scan cell. This will reduce the peak-power of the circuit in test mode. Filling the entire or larger number of unspecified bits in the test set to reduce the peak-power may affect the compression efficiency and may increase the total power, i.e. scan-in and scan-out transitions. It is required to maintain the capture-power within the circuit's peak-power limit for proper operation. Filling one unspecified bit in the test stimuli may affect many unspecified bits in the test response which may cause capture-power violations. So, it is necessary to estimate the impact of filling of each unspecified bit in the test set. The logic values are assigned to the unspecified bit(s) based on its impact on capture-power. The impact of filling of one unspecified bit with the logic value v (i.e. 0 or 1) for the nth scan cell of mth test vector can be computed as

$$C_{impact}(m,n,v) = \sum_{for\,all\,n} R(m,n) \oplus S(m,n) - \sum_{for\,all\,n} R(m,n) \Theta S(m,n)$$

Where and are logic values of the test stimulus and response of same scan cells respectively.

3. SHIFT POWER REDUCTION THROUGH DON'T CARE BIT FILLING

In[2] the idea is to use a during which non-random filling is used to assign values to don't care bits (Xs) of each test pattern of a deterministic test set sequence Experiments performed on ISCAS'89 and ITC'99 benchmark circuits have been done to estimate the reduction in peak power obtained during TC.

In [3] the test patterns are extracted from the ATPG considering a post-ATPG X-filling. SR-aware X-filling is carried out on ATPG extracted test patterns performed based on pre-computed transition probability (TP). Scan chains stitching was done by using minimum WHD (Weighted Hamming Distance) searching. Scan cell value similarity in both scan in and scan out direction is improved with the aid of pattern simulation and the TP estimation. The reason is as it attempts to X-bits assignment to same bits and alike responses are gathered for the referred scan stitching method.

In [4] substantial reduction in shift power during scan testing is achieved through ensuring that the capture switching limit is within the pre-defined threshold. Defect coverage is also increased as compared to other X filling heuristics while keeping test pattern count persistent. Hence the approach can be treated as the balanced way to deal with power efficiency and defect coverage simultaneously. Fill adjacent (FA) technique has got the negative impact on the peak capture power limitation and to resolve this issue Preferred Fill (PF) technique for specifying as many Xs as necessary in order to limit the peak capture under the power budget. This is done in a stepwise [5, 6] fashion and concurrently with the application of MFA/MFA+P technique in order to minimize the number of Xs specified according to PF. As P increases, the defect coverage of the test vectors increases but they consume more shift power. In order to evaluate the scan-in switching activity of every test cube T generated using each of these fillings, they used the normalized weighted switching activity (N-WSA) [7]. This metric counts the number of transitions in successive scan cells, taking also into account their relative positions, and normalizes this value by dividing it by the upper bound of the volume of switching flip-flops.

In [8] the peak shift power minimization problem is formulated as a modified form of interval colouring problem also known as Bottleneck Colouring Problem. Here it is explained how peak toggle minimization may be viewed as a case of Bottleneck Colouring Problem. A test vector ordering algorithm mentioned as interleaved test vector ordering (I-Ordering) having running time O (log (n)) is incorporated here. It is observed that the approach is effective in reducing peak toggles when DP Fill is applied in combination with I-ordering and percentage improvement consistently increases with increase in circuit size. In Table 1 various aspects including merits and demerits of shift power reduction methodologies are pointed out.

Table 1. X-Filling Techniques for Shift Power Reduction

Filling Technique	Key Heuristics	Test Cube	Simulation Benchmark	Claimed Merits	Shortcomings
Non random Heuristic based X-Filling[2]	MT-Fill, 0-Fill, 1-Fill	Tetra MAX	ISCAS'89 and ITC'99	Up to 89% peak power reduction, No DFT cost	Aims to minimize only peak power
SR aware X-Filling and scan stitching[3]	Scan chain reordering, WHD based scan stitching, TP estimation	Tetra MAX	ISCAS'89 and ITC'99	Significant shift power reduction (up to 64%) irrespective of scan chain size.	Increase in computation time and test pattern count
Defect Aware X-Filling[4]	MFA,MFA+P where 'P' is user defined parameter, N-WSA	ATPG	ISCAS'89 and IWLS'05	Higher potential to detect un modeled defects, peak capture power constraint	With the increase in defect coverage, shift power also increases.
DP-Fill[8]	Bottleneck coloring problem, I- ordering	Tetra MAX	ITC'99	Significant drop down in peak toggle by applying I-ordering and DP-Fill jointly.	Peak input toggle increases with number of iterations

4. X- FILLING FOR CAPTURE POWER REDUCTION

In [9] a test cube is processed based on its case type and four numbers of X- cases are formulated based on the combination of whether PPI and PPO are with X bits or without X bits. In respect of fourth X-case of a test cube, depending on corresponding bit-pair values (i.e. '0','1' and 'X') of PPI and PPO type classification (type A-D) is considered. As for example, in case of Type-B or Type-C bit-pairs Case-2 or Case-3 processing is carried out and for Type-D bit-pairs X-filling was done through assignment justification. Hence, depending upon the applicability of an X-case and its type, justification, assignment and assignment justification are applied to conduct X-Filling in order to get fully specified test vector which is expected to yield reduced capture power.

Reduction of switching activity specifically for single capture pulse may result in inadequacy in IR-drop reduction for launch-off-capture clocking based at-speed scan testing which applies two capture pulses and this problem is addressed in [10]. The method in [10] generates 'Cool' test vectors capable of reducing capture switching activity irrespective of any fault coverage, timing, and area overhead impact. Here also eight numbers of X-types are defined based on the pattern in which X types occur. Balanced reduction of first and second capture transitions are achieved by dynamically opting a target capture. The target capture selection is made based on the heuristic total estimated capture transition activity (TECTA). TECTA is derived from existing capture transitions (ECTs) and potential capture transitions (PCTs). Capture switching activity is evaluated through the weighted sum of capture transitions at all FFs which is defined here as a metrics named weighted switching activity at FF (FF-WSA). Larger the value of justification easiness JE(s) results in easier the justification of a logic value on s.

The OJ Fill approach [11] focuses on additional fault detection and compaction aspects instead of looking for only WSA reduction and produces 'silent' test cubes leaving unspecified bits spared for detecting additional faults. SAT- based justified target extraction process is carried out to selectively specify X-values for preserving the likelihood to detect additional faults by ATPG.

Minimization of the total weighted switching activity cropped up in the CUT is done through the formulation of ILP based zero-one linear problem (ZOLP) in [12]. ZOLP equations are formulated to minimize test mode switching activity by filling X bits of partially specified test patterns. Transformation of the Boolean functionality of CUT into LP equations with an optimization function was done in the first phase to achieve the above. Afterwards, specified bits values are assigned to input variables in ZOLP model

SAT– Fill [13] assumes that the transition probability of a flip-flop cause those of other flip-flop is different as for all flip-flops and such transition probability is estimated for an individual flip-flop. SAT solver is used for searching such value assignments not causing transitions. Assuming unequal effects of power dissipation for transitions for each flip-flop, a strong effect on power dissipation at launch-on capture

cycle makes selection order of the flip-flop high and this order is settling on by applying the correlation amid the transition of a flip-flop and power dissipation at launch-on capture cycle.

In the state sensitive X –Filling approach [14], a probability-based WSA model for capture operation was formulated and aimed to reduce transitions of both scanned flip-flops and internal gates. X-bits in PI s are state dependent and owing to this filling individually would compromise the filling effectiveness and hence a state-based method was formulated in [14] which warrant that the total capture switching activity (TCSA) of any test cube is to be kept as minimum as possible.

5. SHIFT AND CAPTURE POWER REDUCTION

The heuristic minimum set of primary inputs (MSPI) is applied AB-Fill [15] approach to control the number of transitional FFs in order to lower down capture power. The filling process is classified into four different types (A-E) of filling. A backtracking table computes clarity of correlation among scan-in cubes and scan-out bits and specifies the value of each shift-in cube to assign the appropriate line. The specified value can effectually control the capture switching activity for each flip-flop. Minimization of the Hamming distance amid PPI and PPO in each test pair is the prime objective behind this X-filling [15] approach.

BA fill [16] was put forwarded to reduce peak capture switching activity by managing the relationship between the capture and stimulus values of the combinatorial logic without needing any extra DFT. Weighted transition count (WTC) metric was used to compute shift switching activity for scan-in and scan-out data. Bitwise XOR operation was applied to input test stimuli and response vector of each scan cell and thus the extent of capture activity was estimated.

The impact of an X-bit on a CUT’s shift- and capture-power (mentioned as S-impact and C-impact) is modelled in [17] and applied these to steer the X-filling (mentioned as S-fill and C-fill). Initially, X-filling was done for shift-power reduction (termed S-filling) subject to the constraint that capture power laid within the CUT’s peak power limit. Upon violation of the constraint X-filling aiming to capture power reduction (named C-filling) was performed. After capture power reduction, remaining X-bits are filled up with S-filling and the further violation of capture power if any was checked once again and such steps iterate among themselves. Shift-In Transition Probability (SITP) and Shift-Out Transition Probability (SOTP) are estimated for filling any X-bit and sum of SITP and SOTP is termed as Shift Transition Probability (STP). The value of STP against ‘0’ and ‘1’ determines the filling binary value of the next X bit. Likewise, Capture Transition Probability (CTP) plays a decisive role in X-filling.

It was attempted in [18] to cluster the scan flip-flops with common successors into single scan chain so that the specified bits per pattern was distributed over minimal scan chains and on the basis of this arrangement it became possible that all the bits to some scan chains in a vector found as don’t care(X). Segment-based X-filling was proposed for such scan chains in order to reduce test power and also to keep defect coverage consistent.

CSP Filling [19] begins with the application of the MTC-filling technique to fill the entire unspecified bits in the test cube. Capture-transitions of each pattern are computed after filling all X-bits with a logic value of ‘0’ or ‘1’. The capture power threshold is checked against each pattern and if any violating pattern is found then that individual pattern is subjected to further capture power reduction in order to bring it within the threshold. Pseudo primary inputs of the capture violated test cube are subjected to minimum capture transition scheme and the MTC-filling. This practice sequence is repeated for every violated pattern with a view to make capture transitions against individual pattern within the capture threshold limit. Don’t care bits in the test pattern are filled with the value of the most near specified bit on the left side for reducing transition between consecutive bits resulting in drop down of shift power. The shift power also depends on the position of transition and weighted transition metric (WTM) used to compute shift-in transitions.

A fan-out aware modified adjacent X-filling technique is proposed in [20] to reduce shift and capture power. Besides the average and peak test power reduction, time complexity and number of iterations are also reduced in this method. The method primarily emphasizes on reducing capture power hence resulting in the slightly higher consumption of shift power as compared to other adjacent filling techniques. The orders of filling X-bits were determined by fan-outs of the logic cells. It was assumed that scan cell with X-bit having larger fan-out corresponding to given test vector bears higher impact on the peak power and these cells are identified accordingly.

In the [21] combination of 0 filling and 1 filling are applied in the test set to reduce test power. The peak switching activity against each test pattern is recorder for 0-fill and 1-fill. The sort of filling which yields lesser peak switching activity was picked. The optimal features of 0-fill and 1-fill are mixed for dropping down average shift switching and average capture switching.

In Table 2 and 3 various aspects including merits and demerits of shift and capture power reduction methodologies are pointed out.

Table 2. X-Filling Techniques for Capture Power Reduction

Method	Key Heuristics	Benchmark	Claimed Merits	Shortcomings
LCP-X Filling[9]	Justification, Assignment, Assignment-Justification	ISCAS'89	In comparison with random *X*-filling, the average and maximum number of node transitions are reduced by 49.3% and 13.3% respectively	It is concerned with only capture power reduction
Double Capture(DC)-X Filling[10]	FF-WSA Metric, TECTA, Justification easiness (JE)	ISCAS'89	Significant IR-drop reduction without any circuit modification and overhead, fault coverage loss	Increased processing time due to multi pass procedure, Justification process consumes much running time
Opt-Justification (OJ)-Fill[11]	Justification target, Un satisfy-able justification target, post ATPG stage	ISCAS'89	Ability to detect additional faults, silent test cubes are produced by switching activity reduction through diversified assignment of X-bits, over pattern count resulting in test cost reduction	Peak switching activity reduction is insignificant in second capture cycle, no any assured peak reduction
ILP based don't care filling[12]	Zero-one linear problem(ZOLP) equations	ISCAS'89	Above 64% and 40 % peak WSA reduction in LOC scheme and LOS scheme respectively	Reduction in capture power is compared with random filling only
SAT-Fill[13]	SAT solvers aided identification of assignments not triggering transitions	ISCAS'89 and ITC'99	Value assignments is guided by the possibility of the transitions of other flip-flops, Probability of transition of individual flip-flop affecting those of other flip-flops at LOC cycle was taken into account.	Increased computational time and this approach is limited to LOC mode only
State-Sensitive X-Filling[14]	Capture switching activity(CSA), Total Capture switching activity(TCSA), probability based WSA model	ISCAS'89	X-bit assignment is done through state-based rigid probabilities. Computing time efficient approach. Significant average and peak capture power reduction.	State changes has got the probability of getting influenced by non determinism
X-Stat-Fill[25]	Test vector reordering for scan based architectures realized with toggle-masking flip-flops	ITC '99	7.4% reduction of average peak capture switching	Increased computational cost Greedy approach makes it suboptimal for peak toggle reduction

Table 3. X-Filling Techniques for Shift and Capture Power Reduction

Method	Key Heuristics	Test Cube	Benchmark	Merits	Shortcomings
Adjacent Backtracking Fill[15]	MPSI, E_{Type} Filling PI Relaxation	Tetra MAX	ISCAS'89	Reduced capture switching activity and shift –in transitions	Increased runtime
Bounded Adjacent Fill[16]	WTC metric, bitwise XOR	Tetra MAX	ISCAS and Industrial circuits	Peak capture power reduced up to 98.86 % and 95.26% reduction in SI and SO switching respectively, no pattern inflation	Pattern rejection
i-Fill[17]	C-impact, S-impact SITP,SOTP,STP, CTP	MINTEST	ISCAS'89 and ITC'99	Reduction in thermal stress, increased test parallelism and shift frequency	Increased runtime, High peak shift power
Segment based X-Filling[18]	Segment filling	ATLANTA	ISCAS'89 and ITC'99	persistent, defect coverage significant reduction in capture power and test time	Involvement of DFT cost
CSP Fill[19]	MTC-filling technique, Capture power threshold, Minimum capture transition scheme, WTM	-----	ISCAS'89	Average shift and capture power is reduced by 40% and 11% respectively when compared to 0-Filling	The % of reduction highlighted is measured against basic 0-filling
Fan-out aware modified adjacent X-filling[20]	Scan cell containing X-bit with maximum FAN-OUT	ATLANTA	ISCAS'89	Up to 40% and 20% reduction in capture & shift power when compared to adjacency and LCP filling respectively, Reduced simulation time.	Increased shift power dissipation
Combined 0 and 1-Fill[21]	Peak switching activity	Tetra MAX	ISCAS'89	Up to 73.7% & 69.83% reduction in average shift and capture transitions respectively w.r.t. random fill approach	Power reduction largely depends on X-bits count and internal design of the circuit.

6. COMPARISON OF TEST POWER REDUCTION ON BENCHMARK CIRCUITS

In this section we compare the percentage power reduction among various X-Filling methods. Here we compare the percentage of average shift power, as shown in Figures 1-8, peak power and capture power reduction on selected benchmark circuits.Variour X-filling methods are mentioned in comparison with their abbreviations.

FA, MFA, MFA+10 and MFA+20 [4] represents fill adjacent, modified fill adjacent, modified fill adjacent technique with another 10% of X bits are specified to reduce capture power and modified fill adjacent technique with another 20% of X bits are specified to reduce capture power respectively. SB and SB-MC fill [18] represent segement based fill and segment based fill with multiple chain. B-fill represents balanced fill [22]. MTR Fill [23] represents minimum transition random X-filling. *i*- fill [17] is the impact-oriented X filling method for shift and capture power reduction. BA Fill signifies the bounded adjacent fill [16] and 4m filling scheme is described in [24]. X filling for capture and shift power reduction represented as CSP fill [19].

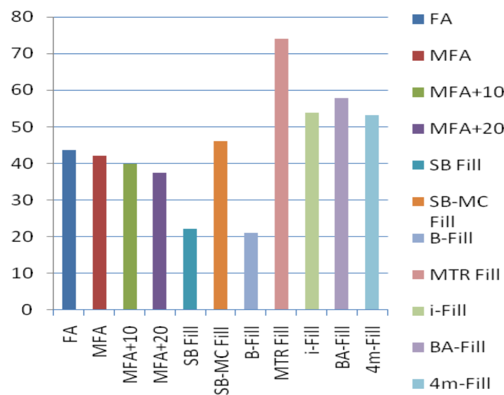

Figure 1. Percentage of Power Reduction in s13207

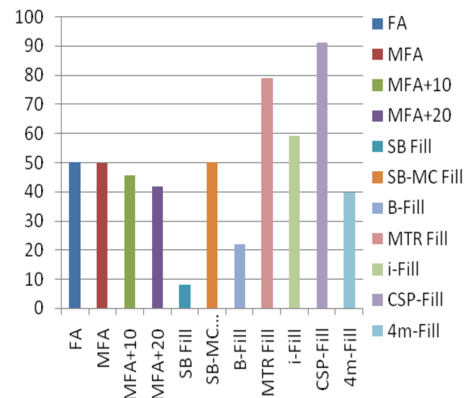

Figure 2. Percentage of Average Power Reduction in s15850

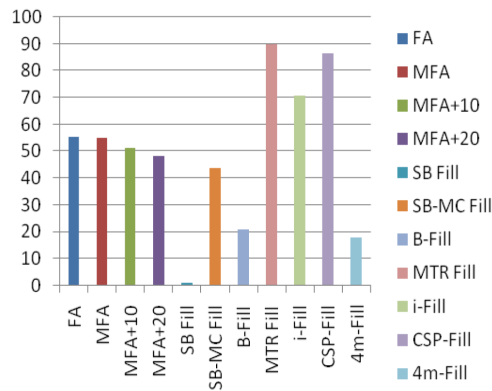

Figure 3. Percentage of Average Power Reduction in s38417

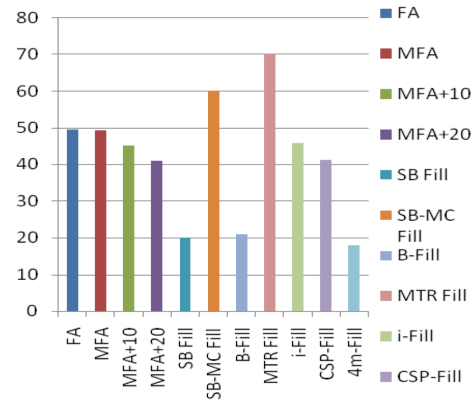

Figure 4. % of Ave Power Reduction in s38584

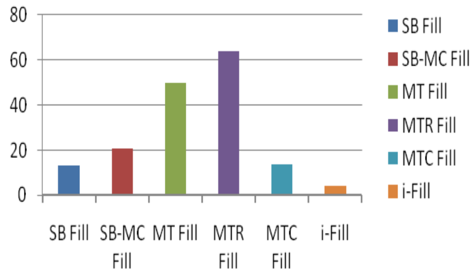

Figure 5. % of Peak Power Reduction in s13207

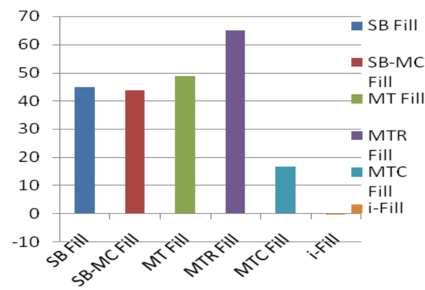

Figure 6. % of Peak Power Reduction in s15850

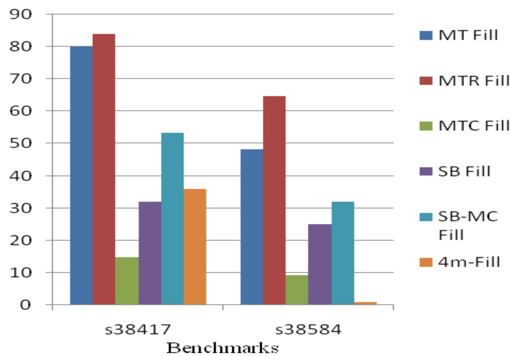

Figure 7. Benchmark wise % of Ave. Capture Power Reduction

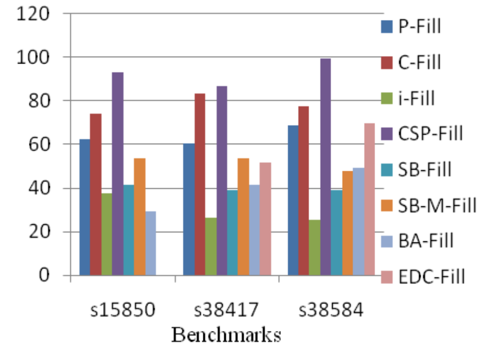

Figure 8. Benchmark wise % of Ave. Capture Power Reduction

7. CONCLUSION

Low power VLSI designs [26, 27] and low power testing strategies are gaining significant attention of this ubiquitously growing silicon industry. We have analyzed state of the art capture power, shift power and shift and capture power reduction methodologies based on filling of unspecified bits in the test cube. This analytical review work focuses on merits and short comings of various don't care filling methods applied to reduce test power i.e. capture power, shift power etc. Finally we put up a comparison of test power reduction potential of respective filling methodologies with the parameter of test power reduction percentage on selected benchmark circuits. This comparison with respect to test power reduction percentage on selected benchmarks provides us the useful comparative information regarding the performance of test power reducing methodologies and may serve as a fruitful input to further research and development works in this field.

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