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SEC-TAED Based Error Detection and Correction Technique for Data Transmission Systems

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Article Info	ABSTRACT
	In the OFDM communication system channel encoder and decoder is the part of the architecture. OFDM channel is mostly affected by Additive White Gaussian Noise (AWGN) in which bit flipping of original information leads to fault transmission in the channel. To overcome this problem by using hamming code for error detection and correction. Hamming codes are more attractive and it easy to process the encoding and decoding with low latency. In general the hamming is perfectly detected and corrects the single bit error. In this paper, design of single Error Correction-Triple Adjacent Error Detection (SEC-TAED) codes with bit placement algorithm is presented with less number of parity bits. In the conventional Double Adjacent Error Detection (DAED) and Hamming (13, 8) SEC-TAED are process the codes and detects the error, but it require more parity bits for performing the operation. The higher number of parity bits causes processing delay. To avoid this problem by proposed the Hamming (12, 8) SEC-TAED code, it require only four parity bits to perform the detection process. Bit-reordered format used in the method increases the probability detection of triple adjacent error. It is more suitable for efficient and high speed communication.

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1. INTRODUCTION

In an Orthogonal frequency division multiplexing (OFDM) consists of channel encoder and channel decoder for encoding and decoding purpose [1]. Source encoder and source decoder are used to convert the analog signals into digital one and digital signals to analog one respectively. The purpose of channel encoder and decoder in OFDM System is to transmit the multiple discrete signals into single channel. Channel encoder and channel decoder contains two types of binary codes. These are block codes and convolutional codes. The combination of cyclic code and linear code is called as block codes.

Block codes are generally used for error corrections, which encode the data into blocks. Linear block codes are an error correction code in which the linear code set is represented as codeword. It is used for forward error correction and transmitting the bits on the channel used for communication. Likewise cyclic codes are also the block codes used for forward error corrections. In this block code, cyclic shift of each word considered as another code word belong to that code. Different types of decoder are available in the communication system for error detection and correction mechanism. Some of the decoders are hamming decoder, viterbi decoder, adaptive viterbi decoder, cyclic redundancies check (CRC), Reed Solomon decoder and so on [2] [3].

Xu J et al., [1] described the multi-path communications using hamming code for error free transmission of data. Hamming codes are able to perform detecting and correcting the errors. Forward error correction (FEC) provides reduced packet delay and improved the reliability for high error rate communications. Satellite communication, under water acoustic networks, underground networks etc. this type of communication networks needs error free communication. Here the packets are reconstructed by segment based voting method. Source node delivers the packets to the destination in multi paths. The transmitted data packet is coded using hamming coding.

In the study of Sanchez-Macian, [2] selective shortening and bit placement techniques are used for hamming SEC-DAED and Extended Hamming SEC-DED-TAED. Shortening algorithm is the best algorithm for hamming codes to increase the probability detection. In addition to SEC-DED and TAED, SEC-DED-TAED is developed in this brief. The approach of handling the codeword is same but extending the more number of bit to detect the more number of bits. A new parity check matrices for SEC-DAED hamming codes and SEC-DED-TAED hamming codes are developed in this brief.

In the literature of Nutan Shep, [3] conventional hamming codes for (7, 4) is implemented in Very Large Scale Integration (VLSI) System design environment. With the help of Verilog Hardware Description Language (Verilog HDL) and Very high speed integration circuit Hardware Description Language (VHDL), algorithm for hamming codes is implemented in this literature. The minimum hamming distance of SEC design is 3, which mean three parity bits are used to detect and correct a single bit error using hamming code.

In the brief of Noorbasha, F [4] optimized encoding and decoding process of hamming codes is presented by using Complementary Metal Oxide Semi-conductor (CMOS) technology. Hamming ECC codes are verified using 50nm, 70nm and 90nm technology. Field Programmable Gate Array (FPGA) implementation methods for developed Hamming ECC codes are provided in this brief. They have simulated and tested the system and got an excellent performance at 50 GHz. The reliability of developed hamming SEC-DEC codes measured at a voltage of 1V, 0.7V and 0.5V. The decoding of hamming codes can give accurate result even transmission technique has a single bit error.

In the study of Cha, S, [5] Check bit Pre-computation methods is used for SEC and DED. The H-matrix of the developed SEC-DED code is the same as that of the odd-weight-column code during the write operation and is designed by replacing 0's with 1's at the last row of the read operation. This design achieves reductions in the number of gates, latency and power consumption of the ECC processing circuits by up to 9.3%, 18.4% and 14.1% for 64 information bits in a word. This literature provides alternate solution for the design of SEC-DED.

Usually, reliability problem of data transmission is improved by channel coding which employs forward error correction (FEC) techniques. FEC technique can detect and correct a single bit error with the help of check or redundant bits. These check bits are determined from data bits and appended to data bits to get the codeword of original data bits. If AWGN affects the data bits other than check bits of codeword, error could be easily detected and correct. If check bits are also corrupted by AWGN, then FEC cannot detect and correct an error. Hamming (40, 32) SEC-DED code is developed to increase the Error Detection and Correction (EDAC) ability. Hamming (40, 32) SEC-DED codes have 8-bits parity memory for single error correction and double error detection. An algorithm based mutual expressions are developed in this review to minimize the EDAC circuit area, and delay parameters. The results of (40, 32) hamming SEC-DED codes are compared to (39, 32) Hsiao code. The critical path of encoder and decoder computation causes more delay and power. But hamming codes have only smoothened path for encoding and decoding process than Hsiao codes. The developed hamming (40, 32) SEC-DED codes offers 2.97% reduction of encoding delay than Hsiao (39, 32) error correction code.

The mentioned block codes are either linear or cyclic error correction codes. Among those techniques, hamming encoder and decoder are the efficient error correcting codes for very large scale integration (VLSI) implementation. Error free data transmission from one end to other end in the wireless channel is not possible. So to detect and correct the errors in the receiver side is the important process to get an error free data. Hamming codes are widely used to find and correct the errors. In general soft errors are generated by SRAM memory device this can be reduced by hamming decoder. Single error correction codes are used to correct the errors without any delay of the circuits. Hamming code is used to protect the external memory, when parity bit is added to the codeword; it takes more amount of memory. Hamming codes are easy to construct [4]. Viterbi and turbo codes are mostly used in the encoder part during the transmission of data. In the hamming error detection and error correction codes are used to detect and correct a single error [5]. The correction and detection of errors in the hamming codes can be done by minimum distance and within the block length. The distance can be measured by calculating the difference between the parity bits and input word length. Because of this reason hamming codes are used in the OFDM communication system.

2. HAMMING CODE FOR ERROR DETECTION AND CORRECTION

Hamming code comes under the family of linear block code. The main purpose of the hamming code is to detecting and correcting the error in the receiver. It was invented by Ritchard Hamming in 1950. Hamming code has ability to detect and corrected the single bit error, with a minimum hamming distance [6]. In general the parity bits are used to detect and correct the single error. Hamming distance (m) is nothing but difference between the input word length and parity bits. The numerical representation of hamming codes are characterized for m≥3 with the following,

$$n = 2^m - 1 \tag{1}$$

$$k = n - m \tag{2}$$

$$d_{\min} = 3 \tag{3}$$

Where, n represent the size of block, k represents the number of information bits, the number of parity bits can be represented as m, dmin is the minimum hamming distance. Number of parity bits is equal to the minimum hamming distance. If the hamming distance is three, it needs three parity bits for single error correction (SEC). The following algorithm to generate the Hamming codeword of information bits,

Step 1: Number the positions of bits starting from 1 to n, where n is the last position of the bits.
Step 2: All positions are represents in binary form 1, 10, 11, 100, 101, 110, 111, 1000, 1001, etc.
Step 3: All bit positions that are power of two considered as a parity bits.

Parity bits are important in the hamming code for single error detection and correction. The position of the parity bits is mentioned as follows,

First Parity Position 2^0: Check 1 bit and skip 1 bit step positions are followed such as 1, 3, 5, 7, 9.......

Second Parity Position 2^1: Check the 2 bits and skip 2 bits step positions are followed such as 2, 3, 6, 7, 10, 11, 14, 15.......

Third Parity Position 2^2: Check 3 bits and skip 3 bits step position are followed such as 4, 5, 6, 7, 12, 13, 14, 15, 20, 21, 22, 23, 24........

Fourth Parity Position 2^3: Check 8 bits and Skip 8 bits step positions are followed such as 8-15, 24-31, 40-47.............

The total number of 1's in the position is even, the parity is set to 0. The total number of 1's in the position is odd, the parity set to 1. This is the method to find the codeword of hamming codes. Single bit error in the hamming code can be detect and correct by using syndrome vectors. The product of lexicographic matrix and codeword of the information is called as syndrome vector. The value of syndrome is zero; assume there is no error in the data transmission.
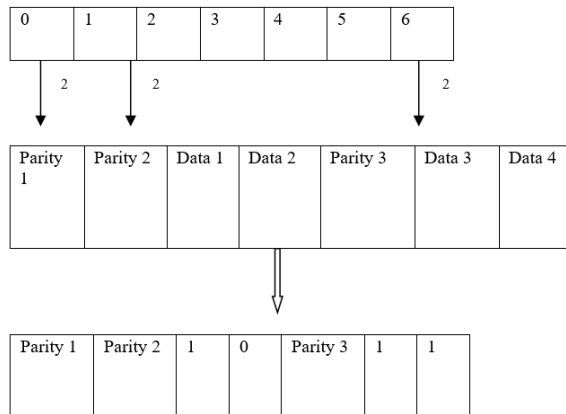
3. SINGLE ERROR CORRECTION (SEC) HAMMING CODES

Lexicographic hamming matrix is used to determine the erroneous bit in the SEC hamming code. Generally, hamming code is represented as (n, k). Where n represents the block size, k represents the number of information bits. Let us consider (7, 4) hamming code, '7' represents the block size, '4' represents the information length. The code can be written as follows,

$$H = \begin{vmatrix} 0 & 0 & 0 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 & 1 \end{vmatrix} \tag{4}$$

Let, the four bit information, input = 1011
Codeword length = Information bit length + Parity bit length = 4+3 = 7
Code word can be formulated as follows,

0	1	2	3	4	5	6

Parity 1	Parity 2	Data 1	Data 2	Parity 3	Data 3	Data 4

Parity 1	Parity 2	1	0	Parity 3	1	1

Parity 1= Even Parity of [parity 1, 1, parity 2, 1] = 1 ^ 1 = 0
Parity 2 = Even Parity of [parity 2, 1, 1, 1] = 1^ 1^ 1 = 1
Parity 3 = Even parity of [0, parity 3, 1, 1] = 0^ 1^ 1 = 0
Now the code word is "0110111"
Next to find the syndrome vector for detecting the error,

$$\text{Syndrome} = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \\ 1 & 1 & 1 \end{bmatrix} \tag{5}$$

In eqn (5) represents the syndrome vector, it is formed by transpose of lexicographic matrix. Multiply the codeword with the syndrome matrix for identify the error.

$$S = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} 0 & 1 & 1 & 0 & 0 & 1 & 1 \end{bmatrix} \tag{6}$$

$$S[0 \quad 0 \quad 0] \tag{7}$$

Eqn (7) represents the syndrome vector; the above vector is null vector, so assume there is no error in the data transmission. If suppose, S= [0 1 0] the received contain some error in the place of syndrome vector. After finding the error location of the syndrome vector, correct the single bit error.

4. SINGLE ERROR CORRECTION – TRIPLE ADJACENT ERROR DETECTION (SEC- TAED) TECHNIQUE

In the SEC-TAED technique detects and correct the error based on the hamming code. In this method the parity bit can be extended to detect the single error as well as triple adjacent errors. The Extended Hamming SEC-TAED code is similar to double error detection method. Hamming (12, 8) SEC-DAED code could cause miscorrection for detecting triple adjacent errors. It requires more than one parity bit 'p' for performing the SEC-TAED operation. So the SEC-TAED method process with (13, 8) hamming code. In the extended method bit-reodered in the code word provide more detection efficiency than the normal method [7]. Hamming (13, 8) SEC-TAED method contain some drawbacks, it reducing the performance in terms of larger time consumption due to the additional parity bit 'p'. In order to overcome the problem by enhanced the extended hamming code.

5. PROPOSED EXTENDED (12, 8) HAMMING CODE FOR SEC-TAED

Overcome the above problem by developed the enhanced extended hamming (12, 8) code for detection and correcting a single error as well as triple adjacent errors [8]. In the proposed method, the bit replacement algorithm is effectively used to change the order of the code word and to maximize the probability detection of triple adjacent error process. The conventional hamming (13, 8) SEC-TAED code needs five parity bits to detect the triple adjacent errors. To avoid the problem, the method used hamming (12, 8) code to detect the triple adjacent error. The proposed bit-reordered format is used to maximize the probability of detecting the triple adjacent error. In conventional bit order, out of '10' combinations only one can help to detect the triple adjacent error. In the proposed bit-order scheme, out of '10' combinations '9' can help to detect the triple adjacent error. This method achieved 90% probability detection efficiency. The proposed bit ordered format expects 5-9-12 are triple error combinations. Hence it helps to improve the bit detective probability. The characteristics of SET such as Coulomb blockade and Coulomb diamonds were observed [9].
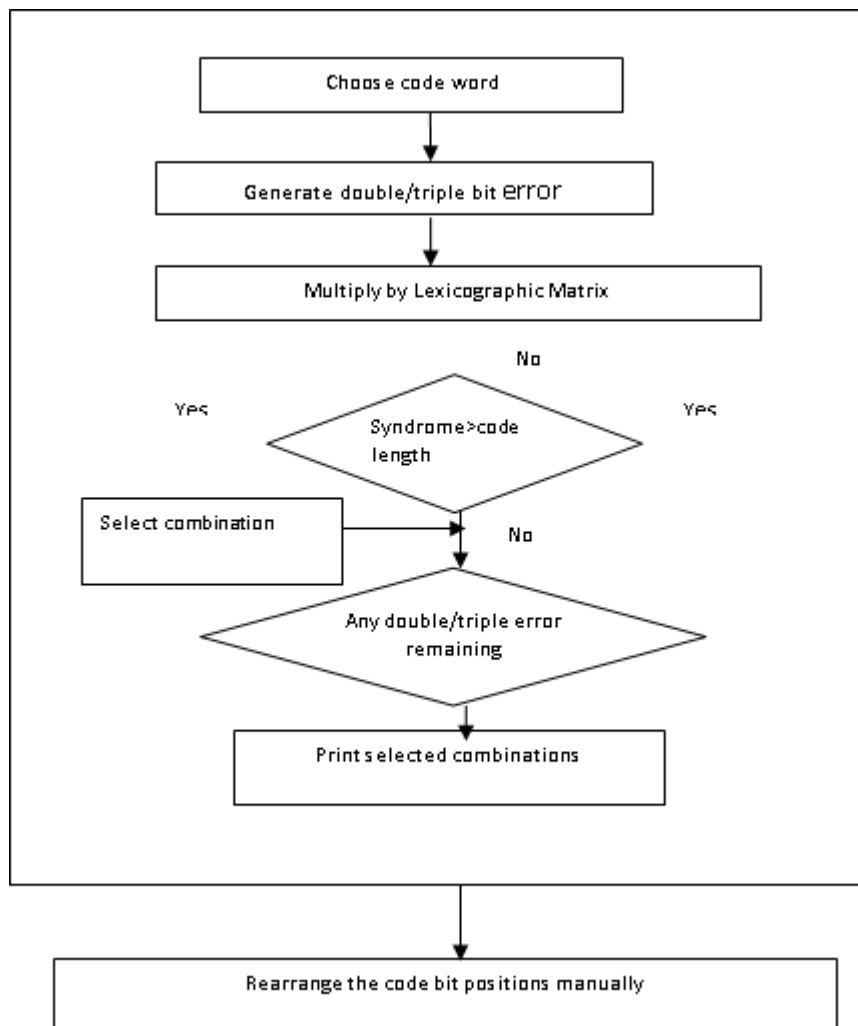

Figure 1. Flow Chart of Bit Placement Strategy

In the double adjacent error detection has only 7-8 combination of bit placement will detect the error. Hence, it detects only 8% of the errors based on the hamming code. In the modified bit placement strategy has '9' combinations of bit placement for detect the triple adjacent errors. The combinations are 1-12, 2-12, 4-9, 4-10, 5-10, 5-11, 6-8, 7-8 and 7-9. It achieves more detection efficiency than the existing one. Bit error rate (BER) analysis is to be performed to verigy the quality of the communication network devices [10]. High speed error detection and correction techniques and FFT architectures are widely used in the MIMO OFDM networks to achieve the high data rate [11] [12].

6.   RESULTS AND DISCUSSIONS

In order to increase the probability of double and triple adjacent error detection and modify the bit replacement algorithm. Bit Replacement algorithm is effectively used to improve the detection of triple adjacent error detection (TAED). The conventional (13, 8) hamming code is used in the TAED process. It achieves 82% efficiency of triple adjacent error detection. The proposed hamming (12, 8) SEC-TAED code achieves 90% efficiency of triple adjacent error detection method. Hamming (12, 8) code for Double Adjacent Error Detection (DAED) is illustrated in Table 1. Likewise the bit ordered format for Hamming (13, 8) triple adjacent error detection (TAED) and proposed hamming (12, 8) triple adjacent error detection is shown in table 2 and table 3. The comparison analysis is represented in the table 4.

Table 1. Double Adjacent Error Detection for Hamming (12, 8)

Bit Placement												Detection	
1	2	3	4	5	6	7	8	9	10	11	12	1/11	9%
1	12	2	3	6	8	7	9	4	10	5	11	9/11	82%

Table 2. Triple Adjacent Error Detection for Hamming (13, 8)

Bit Placement												Detection	
1	2	3	4	5	6	7	8	9	10	11	12	p	1/11	9%
6	8	1	7	11	3	5	9	2	4	p	10	12	9/11	82%

Table 3. Proposed Triple Adjacent Error Detection for Hamming (12, 8)

Bit Placement												Detection	
1	2	3	4	5	6	7	8	9	10	11	12	1/10	10%
7	11	2	6	10	1	4	8	3	5	9	12	9/10	90%

Table 4. Comparison Analysis of the Hamming and Viterbi based Erro Detection and Correction Techniques

Methodology	Slices	LUT	Delay(ns)	Power(mW)
Hamming Decoder	187	247	6.239	252
Adaptive Viterbi Decoder	65	115	20.719	249

The simulation results of proposed extended hamming code are shown in fig. 2, the status of the signal is displayed in the simulation. If the encoding process under process means, 'PROCESSING' status displayed in the simulation. If the decoding process does not detect any error means, 'NO ERROR' status will displayed. If suppose error occurred in the code, could able to detect the error by TEAD method, and printed the status as TED.
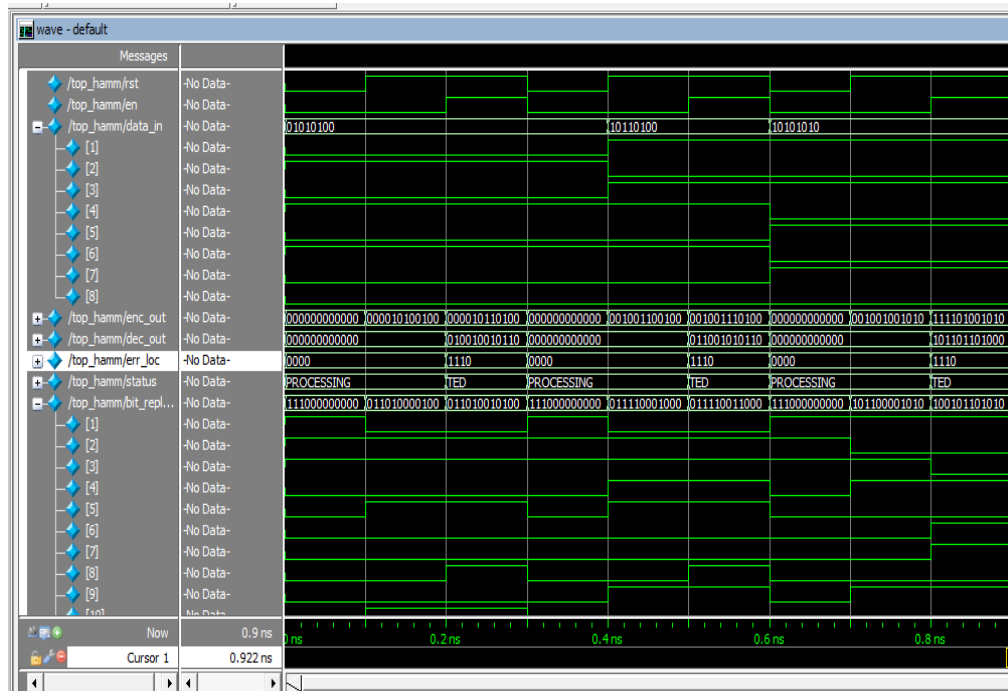
Figure 2. Simulation results of Proposed Hamming (12, 8) SEC-TAED code
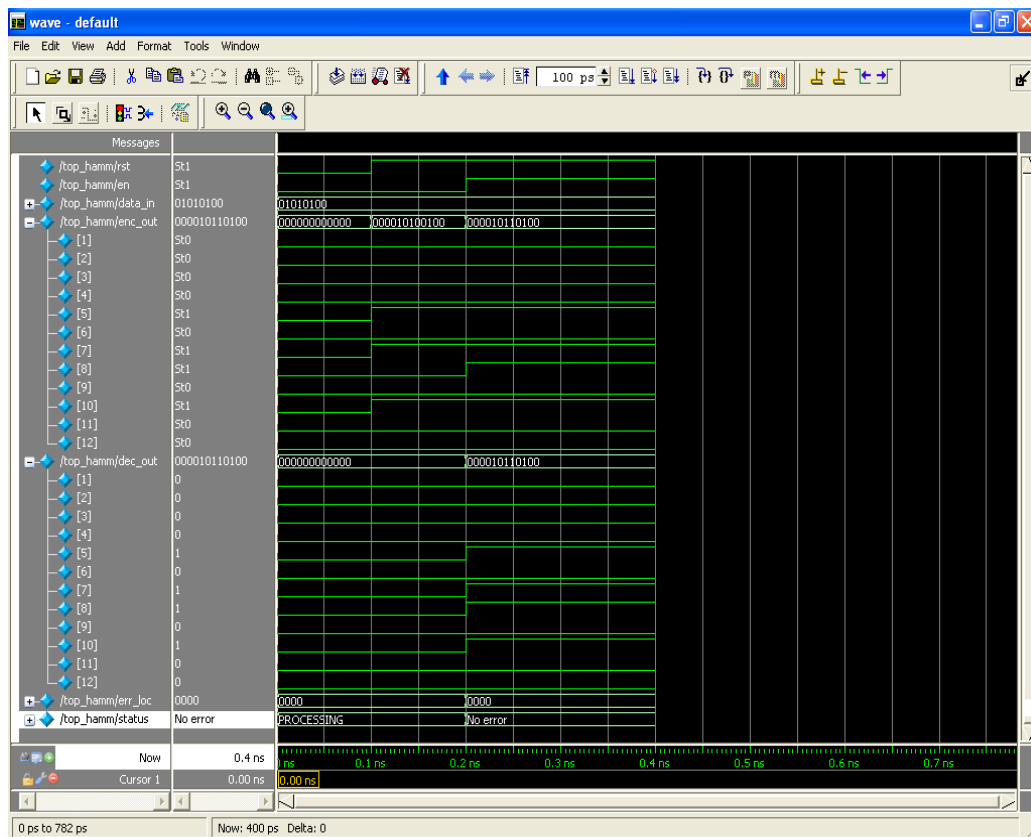

Figure 3. Simulation Result of Hamming (12, 8) SEC-TAED Error-less Data Transmission: Status Displayed as "No error"

7.   CONCLUSION

Channel Encoder and Decoder part of the OFDM architecture performs error correction process. OFDM channel is mostly affected by additive white Gaussian noise, in order to overcome this problem by Hamming error detection and correction codes were used. Generally it detects and corrects the single error perfectly. The proposed hamming code enhanced the detecting performance, the enhance hamming (12, 8) SEC-TAED code was presented by using four parity bits. It offers 90% triple adjacent error detection efficiency. The proposed hamming code offers 8% improved detection efficiency than the conventional hamming (13, 8) SEC-TAED code. Also the proposed method needs four parity bit for detects the triple adjacent error detection.

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