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Design of Low Power Low Noise Amplifier using Gm-boosted Technique

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ABSTRACT

This paper presents the development of low noise amplifier integrated circuit using 130nm RFCMOS technology. The low noise amplifier function is to amplify extremely low noise amplifier without adding noise and preserving required signal to a noise ratio. A detailed methodology and analysis that leads to a low power LNA are being discussed throughout this paper. Inductively degenerated and Gm-boosted topology are used to design the circuit. Design specifications are focused for 802.11b/g/n IEEE Wireless LAN Standards with center frequency of 2.4 GHz. The best low noise amplifier provides a power gain (S21) of 19.841 dB with noise figure (NF) of 1.497 dB using the gm-boosted topology while the best low power amplifier drawing 4.19mW power from a 1.2V voltage supply using the inductively degenerated.

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1. INTRODUCTION

The fast growth of wireless communication system has made radio frequency integrated circuit, CMOS-based technology, an attractive package for radio transceiver front-end circuits in numerous wireless communication systems. In the communication system, Low noise amplifier is the first block of receiver [1]. This amplifier is one of an electronic amplifier that used to amplify very weak signals. Mobile handphones and wireless local area network (WLAN) communication are becoming a part of our daily lives. Design of LNA involves many trade-offs between between its requirements. Thiese involve getting simultaneous high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible current draw from the amplifier. The LNA design in this paper used inductively degenerated topology with Gm-boosted technique to minimize the noise figure and reduce the power consumption at the same time.

2. RESEARCH METHOD

Figure 1 presents the typical inductively degenerated CMOS LNA topology.The inductively degenerated CMOS LNA are chosen because it is widely used and its low noise performance [2-3]. It is nowadays used both in single and multi-standard transceivers because of the better NF and the lower power consumption with respect to other topologies for narrow band applications [3-5]. Inductively degenerated cascode LNA consists of an input signal source RFin. The source resistance Rs of 50Ω, an inductance gate, Lg, source inductor, Ls, load inductor Ld, additional capacitor Cext. Lg and Ls are used to match input impedance while Ld is used to match output impedance. The LNA designed in this paper uses a Gm-boosted technique structure with inter-stage inductors as shown in Figure 2. In this circuit M1, M2 are the cascade

transistors, M3 is used to build the bias for the LNA, Lg and Ls are used for the input matching. While Ld, Lg and Cext are the inter-stage components.

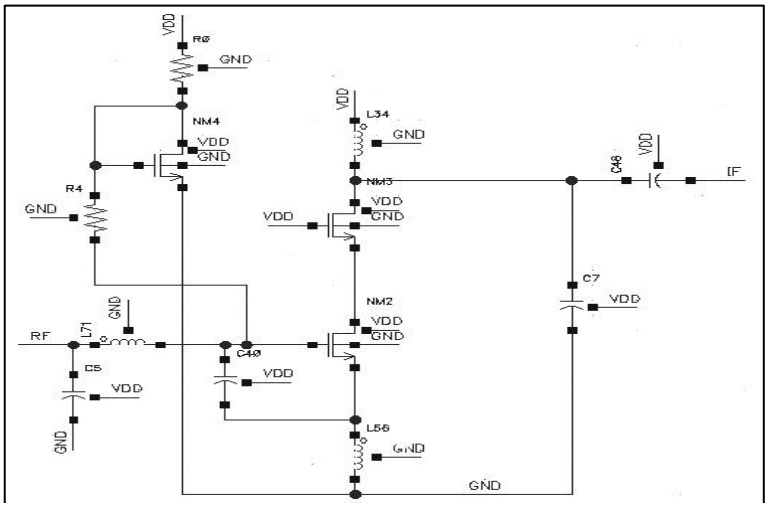


Figure 1. Circuit topology of inductively degenerated LNA

In this LNA design, the suitable value of inductor, L_s is chosen. Then the value of gm and C_{gs} are calculated to give required Z_{in} [6]

$$Z_{in} = \frac{Vg}{Ig} = \frac{IgRg + Vc + j\omega IsLs}{Ig} \quad (1)$$

$$Z_{in} = \frac{Ls.gm}{Cgs} \quad where\ Zin\ may\ be\ 50\Omega \quad (2)$$

Degeneration Inductor L_s can be found by using equation 2. Then the optimal Q factor of inductor L_s can be calculated by using equation 3.

$$\omega_T = \frac{gm}{Cgs} = \frac{Rs}{Ls} \quad (3)$$

Optimal Q of Inductor,

$$Q_L = \sqrt{1 + \frac{1}{P}} \quad (4)$$

$$Where\ p = \frac{\delta.\alpha^2}{5.\gamma}$$

The value of inductor Lg can be found by using equation 5.

$$L_g = \frac{Q_L R_S}{\omega_0} - L_s \quad (5)$$

After obtaining the gate-source Capacitance and then the width, W of the transistor can be found by using the equation below;

$$C_{gs} = \frac{1}{{\omega_0}^2(L_{gs} + L_s)} \quad (6)$$

$$W = \frac{3\ C_{gs}}{2\ C_{OX.} L_{min}} \tag{7}$$

Where, $\varepsilon_{ox} = \varepsilon_{ox}\ .\varepsilon_o$ and $C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}}$

Then. The optimum Noise Figure can be estimated as below:

$$NF_{opt} = 1 + \frac{2\gamma}{\alpha}\left(\frac{\omega_o}{\omega_T}\right)\sqrt{P}\ (|c| + \sqrt{p} + \sqrt{1+p} \tag{8}$$

Gain-boosting is a well-established technique that uses and amplifier in place of A(s) to increase the dc gain of a cascade stage [7-10]. A gm-boosted MOS cascade with enhanced bandwidth as shown in Figure 2 can increase the transconductance of M2 by factor of [1 + A(s)], $g_m = [1 + \text{A(s)}]g_{m2}$

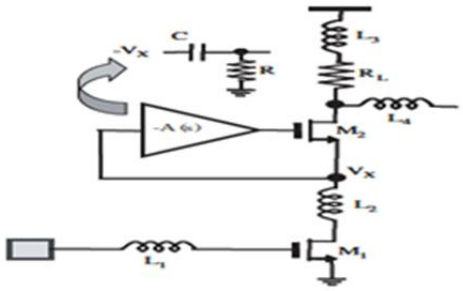


Figure 2. A Gm-boosted Technique Circuit

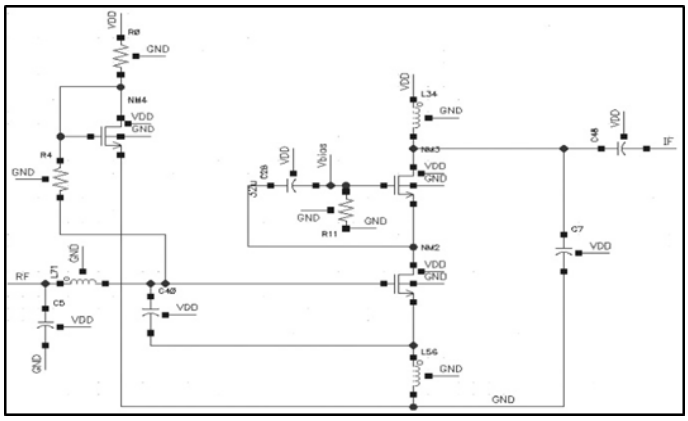


Figure 3. Inductively degenerated LNA with Gm-boosted Circuit

In order to reduce the even-order harmonics of the receiver, the LNA is needed to act as a single-to-differential conversion as well [8]. The cross connection can be used in a fully-differential circuit to provide the polarity of the feedback. The first order of high pass response can be provided by using a simple CR-section for the cross connection.

$$\text{A(s)} = \frac{RC_S}{1 + RC_S} \tag{9}$$

The formula for frequency dependent transconductance can be obtain by substituting equation (2) into (1).

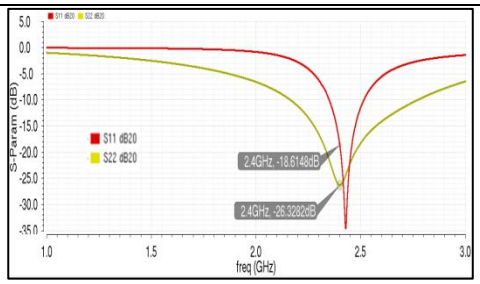
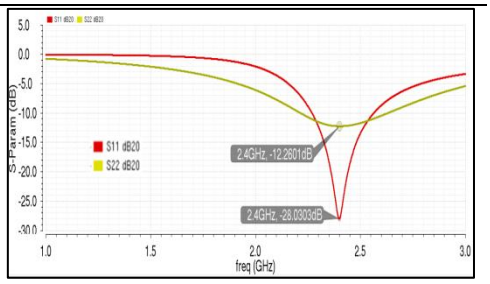
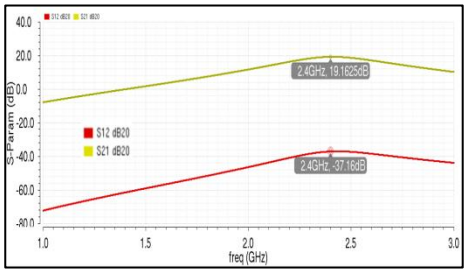
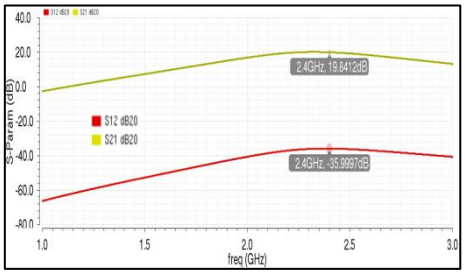
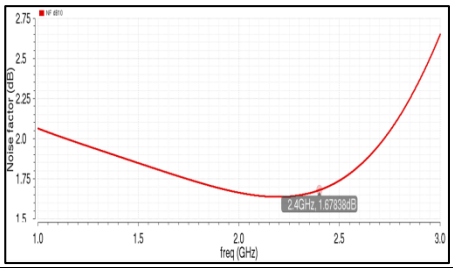
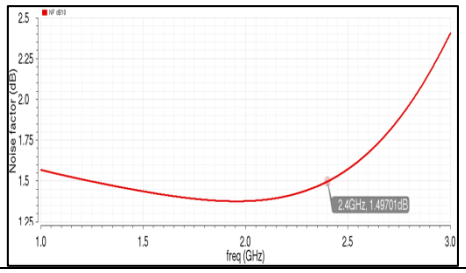
$$g_{m1} = \frac{1 + 2RC_S}{1 + RC_S}\ g_{m2} \tag{10}$$

Thus, $g_{m1} \approx g_{m2}$ when $f \ll \frac{1}{2\pi RC}$ or at low frequency. While at high frequency $f \gg \frac{1}{2\pi RC}$, $g_{m1} \approx 2g_{m2}$. The schematic as shown in Figure 3 is the combination technique between inductively degenerated and gm-boosted. Both techniques are used in one circuit to optimize the result of the gain bandwidth and noise factor.

3. RESULTS AND ANALYSIS

Table 2 compares the Scattering parameter graphs obtained from the simulation of LNA circuit design utilizing inductively degenerated topology and Gm-boosted techniques. What stands out in the table is that, by using Gm-boosted technique to the inductively degenerated topology the gain obtained higher which is 19.841dB.

Table 2.1 Graph Comparison of LNA performance using Gm-boosted technique

Parameter	Inductively degenerated topology only	With Gm-boosted
S_{11} and S_{22}		
S_{21} and S_{12}		
Noise Figure (NF)		

The output matching circuit does not change the bias of the active device. It is very easy to achieve the required output matching without any filter network at the output since the LNA has very low output impedance. The graph of S22 illustrates the inductively degenerated LNA manage to get -26.329 dB instead of the gm-boosted value is -12.260 dB. The output reverse isolation is very important criteria to ensure better stability and lower NF. The simulated noise figures of the LNA topologies is 1.68 dB for the inductively degenerated while the gm boosted is 1.497 db. The power dissipation for inductively degenerated topology is 4.19 mW while for gm-boosted topology is 6.933 mW. Table 2 presents the comparison of LNA design with other published works.

Table 2.2 Performance comparison with other published works

	References			This work	
	[9]	[10]	[11]	Inductively degenerated	Gm-boosted
Process technology	180nm	180nm	130nm	130nm	130nm
Frequency (GHz)	1.5-11.7	1.4-9.5	1.25-11.34	2.4 GHz	2.4 GHz
Power supply (V)	1.8	1.8	1.2	1.2 V	1.2 V
S_{21} (dB)	12.26	13	11	19.16	19.84
S_{11} (dB)	-8.6	-9.5	-11	-18.61	-28.02
S_{22} (dB)	n.a	n.a	n.a	-26.32	-12.26
S_{12} (dB)	-26	n.a	-35	-37.16	-40.00
Noise Factor (dB)	3.74-4.74	4.3	2.38-3.4	1.67	1.49
Power Dissipation (mW)	10.34	20	5.8	4.73	6.19

Figure 4 shows the layout design of the combination between inductively degenerated and gm boosted topology. The size of this layout is 693µm x 723µm. All the component chosen to make this layout are using the RFCMOS technology.

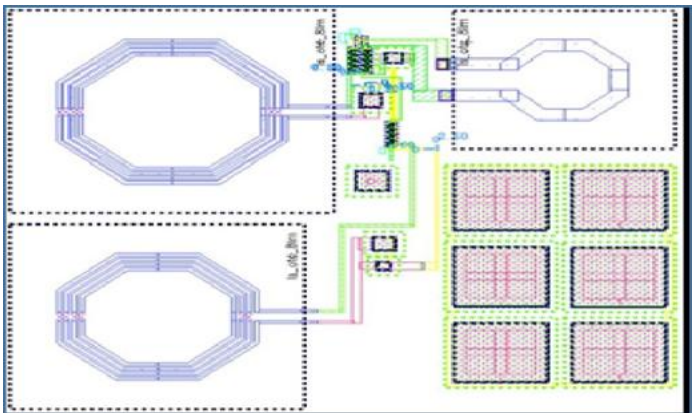


Figure 4. Layout of LNA

4. CONCLUSION

The design of low power LNA were successfully implemented using Inductively Degenerated topology and gm-boosted topology. The LNA design achieved a power gain (S21) of 19.841 dB with noise figure (NF) of 1.497 dB while also managed low power at 4.19mW.

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