

Optimization of Arithmetical Operators for the Enhanced Wallace Stage

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ABSTRACT

In the field of Digital signal processing (DSP), the reduction of some logical elements counts is one of the main considerations. To minimize the area, computational delay, and power, the digital form FIR filter is to be implemented. The optimization of the ATP (Area, Time and Power) is achieved by using the efficient multiplication and accumulation unit (MAC). In this work, the direct form FIR filter with the efficient MAC unit is presented. At the initial stage, the half adders and full adders are to be modified by the reduction of the logical gates. The modified half and full adder are implemented in the Wallace tree multiplier for performing the efficient multiplication process. Carry save adder is divided into the two stages to reduce the computational delay of arithmetical operators. The proposed MAC design is implemented in the direct form FIR filter by using the HDL language.

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1. INTRODUCTION

The demand for low power Digital Signal Processing (DSP) applications and high-speed multi-standard wireless communications is quickly growing. The Unstable growth in portable multimedia and mobile computing applications has mostly depended on the signal processing technique [1]. Finite Impulse Response (FIR) filter is one of the key features of Signal Processing approach. FIR filter requires the two factors known as low complexity and reconfigurability for low power applications. The major factor of low complexity depends on the adder and multiplier structures in filter [2]. To reduce the complexity and delay of the computations, various types of adders and multipliers are introduced. The second major factor for FIR filter is reconfigurability. The direct form of FIR filter consumes more area and delay to perform the filter operations [3]. The direct form FIR filter performs the filter operations for fixed type of filter order only whereas the reconfigurable FIR filter performs the filter operation for dynamically changes the filter order. In this research work, the Russian Peasant Multiplier is introduced to reduce the area and delay for computation [4].

The high-performance adders and multipliers are essential for reducing area and delay in reconfigurable FIR filter. Therefore, the above-mentioned efficient adder and multiplier are incorporated into reconfigurable FIR filter to concern low area and delay.

2. RELATED WORKS

In this paper, the efficient implementation of reconfigurable FIR filter is presented. The direct form FIR filter is used only for fixed coefficient filter operations whereas the reconfigurable FIR filter is used for both fixed as well as dynamically changing filter coefficient values [5]. A Reconfigurable FIR filter to

Tradeoff Filter Performance for Dynamic Power Consumption had proposed reconfigurable FIR filter consists of Multiple Control Signal Decision Window (MCSW) technique for increasing the filter performance for dynamic power consumption. Studies and Evaluation Performance of Vedic Multiplier using Fast Address are carried out. In this paper Vedic Multiplier is designed by Urdhva Tiryagbhyam (UT) technique.

In this paper described that the An efficient approach for the removal of bipolar impulse noise using median filter [6]. Vedic Multiplier is one of the fast and low power multiplier compared to all another multiplier. In this multiplier design, performance was analyzed by using different existing adders such as Carry Lookahead Adder (CLA), Carry Select Adder (CSLA) and Parallel Prefix Adder (PPA). Reactive power optimization using firefly algorithm is presented in this paper [7]. A study of Architecture's for Low Power and Reconfigurable FIR Filters is carried out. The key requirements of FIR filters are low complexity and reconfigurability. In this paper, low power reconfigurable FIR filter is proposed by using Constant Shift Method (CSM), Programmable Shift Method (PSM) and Computation Sharing Multiplier Method (CSHM). The performance of each method is analyzed and compared in this study. SVC created Single Input Fuzzy Logic Controller SVC for self-motivated presentation augmentation of Power Systems.

3. MINIMIZED HALF AND FULL ADDER STAGE FOR DIGITAL FIR FILTER

In Multiplier and adder unit, the half adder and full adder is one of the necessity stages for performing the arithmetical operations. The reduction of the half and full adder is used to reduce the logical elements counts as well as the computational delay of the arithmetical operator stage. A logical block of the minimized half and the full adder is shown in Figure1 and Figure 2. The reduced half adder performs the same additions like traditional half adder stage with the reduction of the one logical AND gate and one inverter stage. In Figure 2, the optimized full adder performs the same three-bit additions like conventional full adder with the optimization of the logical OR gate and logical AND gate. These optimized adders are used to implement the several multipliers and adders stages to achieve the efficient area, delay, and power. By using the Demorgan's theorem, the adder stages are optimized.

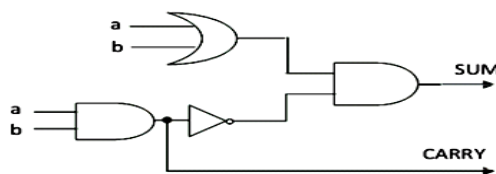


Figure 1. Optimized half adder stage

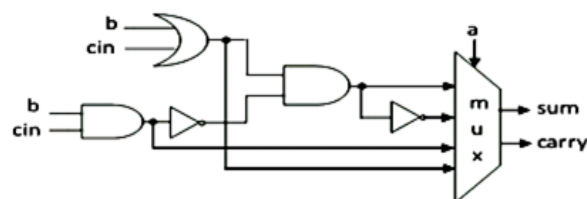


Figure 2. Optimized full adder stage

4. MATHEMATICAL EXPRESSION FOR THE OPTIMIZED HALF AND FULL ADDER STAGE

$$\begin{aligned}
 Sum &= X\bar{Y} + Y\bar{X} \\
 &= (X + Y)(\bar{X} + \bar{Y}) \\
 &\quad (X + \bar{X})(Y + \bar{Y}) \\
 &= (X + Y).(X + \bar{Y})
 \end{aligned}$$

$$\begin{aligned}
 Sum &= (X+Y).XY \\
 Carry &= X.Y
 \end{aligned}$$

5. PROPOSED WALLACE TREE MULTIPLIER WITH THE OPTIMIZED HALF AND FULL ADDER

To provide the efficient multiplications with the minimum number of logical elements counts, the optimized half and the full adder is used to perform the arithmetical operations. The proposed Wallace tree multiplier stage is further used for the digital FIR filter. Proposed MAC unit is generating the efficient ATP product compare than the traditional method.

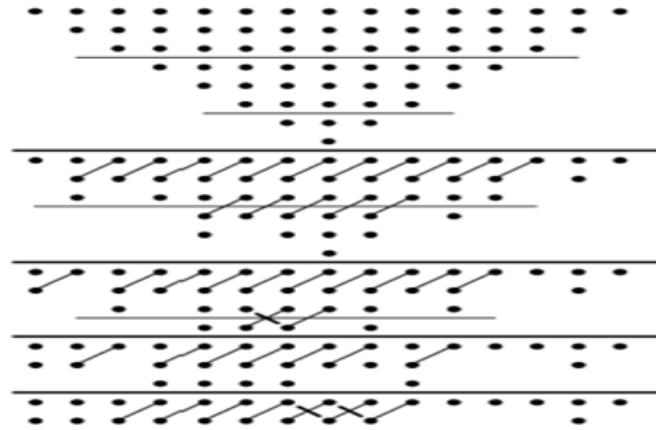


Figure 3. Wallace tree multiplier structure

Table 1. Synthesis Results for the traditional and proposed stages

Parameters	Classic stage	Optimized stage
Computational Delay (ns)	23.854	20.655
Number of Slices	40	32
Look-Up-Tables	71	57

6. EXPERIMENTAL RESULTS AND ANALYSIS

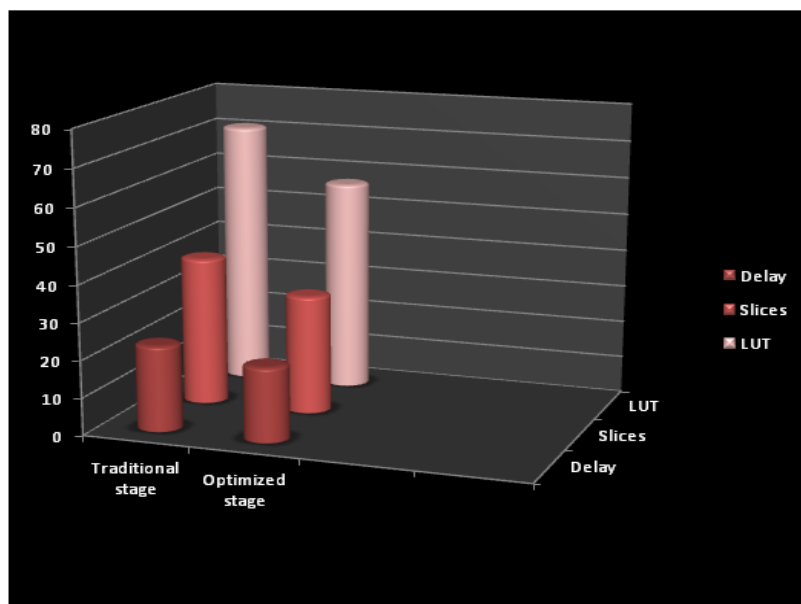


Figure 4. Graphical Representation of the synthesis results

7. CONCLUSION

In this work, the optimized half and full adder based reduced Wallace tree multiplier is implemented by using Verilog Hardware Description Language (HDL). The simulation of the proposed work is evaluated by using Modelsim XE and also the design is synthesized by using Xilinx ISE. Enhanced adders stages are highly used to reduce the number of logical elements counts as well as the computational delay of the Wallace tree multiplier stage.

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