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Multiplexer Based Multiplications for Signal Processing Applications

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Article Info	ABSTRACT
	In signal processing, Filter is a device that removes the unwanted signals. In any electronic circuits, Filters are widely used in the fundamental hands on tool. The basic function of the filter is to selectively allow the desired signal to pass through and /or control the undesired signal based on the frequency. A signal processing filter satisfies a set of requirements which are realization and improvement of the filter. A filter system consists of an analog to digital converter is used to sample the input signal, traced by a microprocessor and some components such as memory to store the data and filter coefficients. Filters can easily be designed to be "linear phase" and it is easy to implement. In this paper, the birecoder multiplier (BM) is designed in terms of VLSI design environment. The proposed multiplier is implemented by using VHDL language and Xilinx ISE for synthesis. The multiplier is mainly used for image processing applications as well as signal processing applications.

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1. INTRODUCTION

Digital filters process is digitized or sampled signals. A digital filter determines a quantized time-domain representation of the convolution of sampled input time function and a representation of the weighting function of the filter. They are recognized by an extended sequence of multiplications and additions carried out at a uniformly spaced sample interval. It is used to perform mathematical operations on sampled and discrete time signals to enhance certain aspect of the signals. A new method of high performance digital filters are based on the simulation of analog LC passive ladder filters .The digital filter consists of an A-D converter block to convert the analog form of signal to digital form of signal. To perform the numerical operations on the sampled data, digital signal processors are used. This processor is used in general purpose processor such as pc or a microprocessor or a DSP chip. FPGA is used instead general purpose processor or specialized DSP with specific parallel architecture for performing operations such as filtering, in high performance applications. It carries the numerical calculations on sampled data. These calculations involve input values are multiply by constants and the product values are added together. Memories are used to store the data. Finally, a digital-to-analog converter block is used to convert the processed digital signal to corresponding analog signal.

2. RELATED WORKS

Reference [1] described the design of FIR filter. Multiplier unit high speed is completed using XOR-XNOR column by column reduction compressors using full adder. Multiple pairs of Ripple Carry Adders

(RCA) are used in CSLA structure. Carry select adder eually divides the word size of the adder into blocks of 4-bit each. FIR filter is designed to increase the speed of addition and decrease the power taken by the multiplier unit. The carry propagation delay and area of carry select adder is decreased by splitting carry select adder into equal bit groups. Reference [2] explained the carry select adder is used in many data processing processors to perform fast arithmetic operation. Gate level modification is used to decrease the area and delay of CSLA. The RCA with BEC in the architecture is a good advantage to reduction in the number of gates. Modified SQRT CSLA has slightly large area for lower order bit which decreases for higher order bit and also delay is reduced. The number of bits required for BEC logic is 1 bit more than the RCA bits. Reference [3] presented vector-scalar multiplications with programmable scalars are commonly found in application specific digital circuits. Generation of quasi-minimum EDBNS has been proposed. Extended Double Base Number System can be directly mapped to an efficient Time-Multiplexed Multiple Constant multiplication (TM-MCM) architecture consisting of only adders, multiplexers, programmable shifters and a LUT. Fiter coefficients change either dynamically or periodically, the search for common sub expressions multiplierless implementation. Reference [4] explained that the constrained Lp magnitude error design of FIR filter has been equivalent to a convex constrained Lp frequency response error problem with a phase response of the optimal FIR filter of the original constrained Lp magnitude error problem [5]. The convergence and its parameter and initial condition dependence are shown through the design of FIR filters without time domain constraints. The repetition method is applied to the minimax design of evidence filters, Nyguist filters and step response filters and to the Lp design of pulse shaping filters for ultra wideband systems.Genetic algorithm for image super resolution using wavelet transformation [6]. Image super resolution reconstruction [7] is represented using iterative adaptive regularization method and genetic algorithm.

3. PROPOSED METHODOLGY

In 8×8 Bi-Recoder multiplier, partial products are generated using multiplexer. Based on multiplier bit values, multiplexer is used to perform the partial product generation process. In Figure 1, the value of 'a' represents multiplicand value and the value of 'b' is multiplier value. For each multiplexer produces 10-bit partial product value.
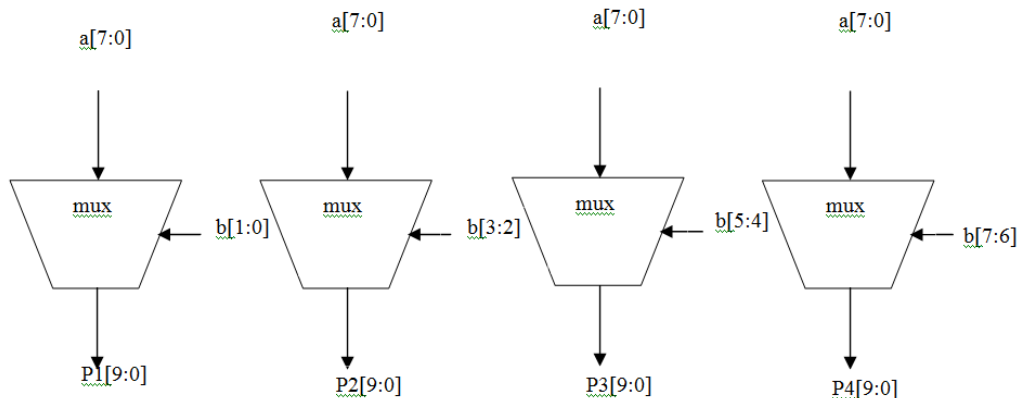

Figure 1. Bi-Recoder architecture

Multiplier bits are divided into four groups and each group is having two bits. So four set of multiplexer is needed to generate the partial products. If value of 'b' is "00" means, it passes simply 0 to the partial product generator else if it is "01" means it simply passes multiplicand value to the partial product generator else if it is "10" means it passes 1 bit left shift of multiplicand value in terms of 10 bits else it is "11" means add the results of multiplicand and 1 bit left shift of multiplicand value.

4. ANALYSIS OF SIMULATION

Simulation result of Bi-Recoder multiplier is shown in Figure 2. Then multiplier result is represented as final. First of all it takes one clock cycle for initialization of the result. Here initialization input reset is as "0" at the time final value is "0000000000000000". For next clock cycle "a" is given as "00110111" and "b" as "00011001", the final value is "00000101010111111".
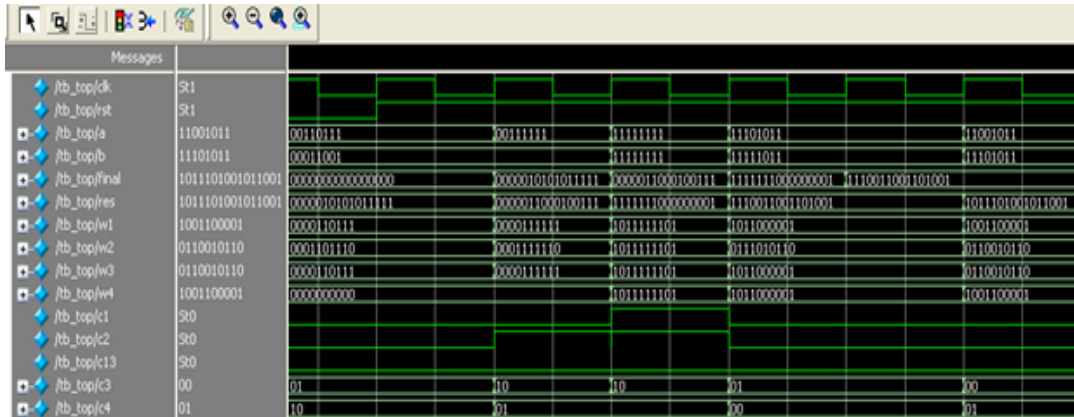
Figure 2. Simulation result

Area occupancy is represented in slices and Look Up Table. In Wallace Array multiplier, value of slices is 82 and value of LUT is 155. But in Bi-Recoder multiplier value of slices is decreased as 77 and value of LUT is decreased as 145. Power consumption of conventionalArray multiplier is 2.478W and in Bi-Recoder multiplier 0.978W. From the results clearly show that area and power consumption of Bi-Recoder multiplier is lesser than conventionalArray multiplier.

Table 1. Comparisons of Bi-Recoder Multiplier and Conventional Array Multiplier

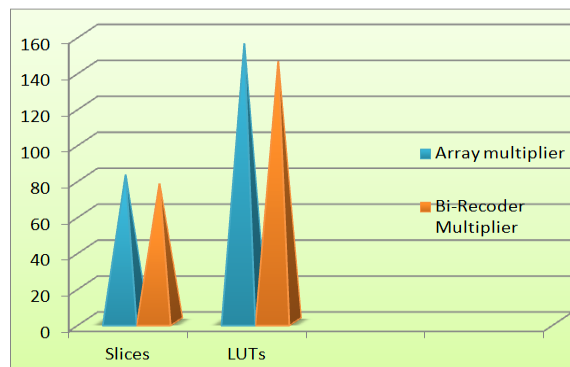| Descriptions	Slices	LUT
Bi-Recoder Multiplier	77	145
Array Multiplier	82	155

Figure 3. Graphical representations for the synthesis results

5. CONCLUSION

This paper presents a Bi-Recoder multiplier design for image processing applications. The proposed multiplier is designed by using multiplexers. The multiplexers are one of the simple logical circuits in the digital electronics. Mux design consumes many numbers of logical gates utilizations as well as computational delay. Due to its less area and low power performance, Bi-Recoder multiplier will be implemented in some applications such as Finite Impulse Response (FIR) filter, Digital Signal Processor (DSP) and Arithmetic Logic Unit (ALU) in future.

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