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Cascaded Ripple Carry Adder based SRCSA for Efficient FIR Filter

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ABSTRACT

Filter is one of the key components of all signals processing elements. Both the FIR and IIR filter are used to reduce the unwanted signal in the original signal. Here discussing the FIR filter and design the efficient FIR filter using Dual Ripple Carry Adder (RCA) based SQRT-carry select adder (CSLA). Many components present in the FIR filter, one of the main component is Adder. Adder is used to combine the signal for avoid the noise occurring in the output. Proposed a Dual RCA based SQRT-CSLA for speed up the filtering process. The filter performance can be analyzed by Xilinx simulation environment.

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1. INTRODUCTION

Filter is a device that removes the unwanted signals. In any electronic circuits, Filters are widely used in the fundamental hands on tool is discussed in [1]. The basic function of the filter is to selectively allow the desired signal to pass through and /or control the undesired signal based on the frequency. A signal processing filter satisfies a set of requirements which are realization and improvement of the filter is presented in [2]. A filter system consists of an analog to digital converter is used to sample the input signal, traced by a microprocessor and some components such as memory to store the data and filter coefficients is described in [3]. Filters can easily be designed to be "linear phase" and it is easy to implement. Filters have two uses, signal separation and signal restoration. The concept of ideal filters is used filter transfer function characteristics and implementation techniques for determining their electronic filter and signal processing needs is explained in [4]. An ideal filter will have amplitude responses as unity at a fixed gain for the frequency of interest called as pass band ratio everywhere else called as stop band. The frequency at which the responses changes from pass band to stop band is called as cut-off frequency is discussed in [5]. The frequency boundary between the pass-band and the stop-band is defined by all filters offer a pass-band, a stop-band and a cutoff frequency. Energy efficient voltage conversion range of multiple level shifter design in multi voltage domain is presented in [6].

2. RELATED WORKS

Yousuf, R. et al, 2008 presented and verified a new methodology for CSA. In this methodology, sum was determined for carry-in of '0' and other sum for carry-in of '1'. These sums were computed by making use of one XOR gate and an inverter. Final sum-out was obtained by making use of multiplexer whose strobe signal was the carry of the previous stage (Cin) [7]. For high speed applications carry select

adder is mostly preferred because it contain output for both cases Cin=0 and Cin = 1. Based on the selection line from the previous stage the output can be selected and generate the output without any delay.

Kim, Y. et al, 2001 explained a design of ripple carry adder, in general SQRT CSLA is designed by only one RCA adder. Here using two RCA for designing the carry-select adder. The circuit of zero finding and MUX to decrease the area power without any affection in the output side [8]. For bit length n=32, the proposed carry-select adder requires 19 % of transistors it is higher than the dual ripple-carry-select adder.

Kumar, D.J. et al, 2014 presented FIR filter implementation of Wallace multiplier, using Modified Carry select Adder (MCSLA) and Carry Skip Adder. It reduces both area and delay in booth multiplier using modified carry save adder. Due to parallel addition process in modified carry save adder, it achieves very high speed [9]. This type of FIR filter is also applicable in communication purpose.

Sahoo, S.K. et al, 2008 presented a novel architecture for a high speed Finite Impulse Response (FIR) Filter. CSHM converts the multiplication process into a series of shift and add operations. CSHM offers a markedly improved performance over Carry Save Array Multiplier CSAM implementation. The adder in the last stage lies in critical path uses a carry save adder. The use of Dual Channel Adder and Compressor at every intermediate stage to reduce computational delays [10], propagating sum and carry separately to the end and then using a very high speed adder like a Carry-Look Ahead Adder.

3. OVERVIEW OF CARRY SELECT ADDER (CSLA)

Carry select adder is used to speed up the overall circuit. The carry select adder comes in the group of conditional sum adder. It works with some conditions based on architectural design. Sum and carry are expected by assuming input carry as1 and 0 prior the input carry comes. Carry Select hybrid adder is a better choice for high speed applications. It contains two ripple carry adder and one multiplexer (MUX). Adding two n-bit numbers with two adders in order to perform the calculation one time, the assumption of carry being zero and the other assuming is one. The number of bits can be uniform. Efficiency, flexibility, stability are the factors are required to achieve a high speed, Low power, area efficient, adders. The CSLA circuit is widely used to reduce the problem of delay in the filter by generating multiple carries and then select a carry to generate the sum.

4. DUAL RCA BASED CSLA

The structure of Dual RCA based CSLA is shown in Figure 1. This structure of the Dual RCA is simple because it contains only two RCA adders. The Cin input to the adder is 1 and 0. One RCA take the ‘0’ input and the other RCA takes the ‘1’ as input to generate the output. RCA generally generate propagation delay to avoid the delay by adding another RCA in the circuit. One of the RCA is initially starts with Cin = 0 and the other RCA initiate with Cin=1, both the results are ready to give the output. Finally based on the previous results the output can be selected. The final outputs are selected by the 2:1 MUX. CSLA has two units, one is the sum and carry generator unit (SCG) and the other is the sum and carry selection unit (SCS). Due to dual RCA, traditional CSLA does not provide better performance. In order to overcome this problem, BEC circuits are used in CSLA for generating the sum and carry. Some of the BEC based circuits with Cin=1 in the traditional CSLA to achieve lower area and power consumption. The RCA has lowest speed among all the adders because of large propagation delay but it occupies the least area. Carry i.e. 0 and 1.

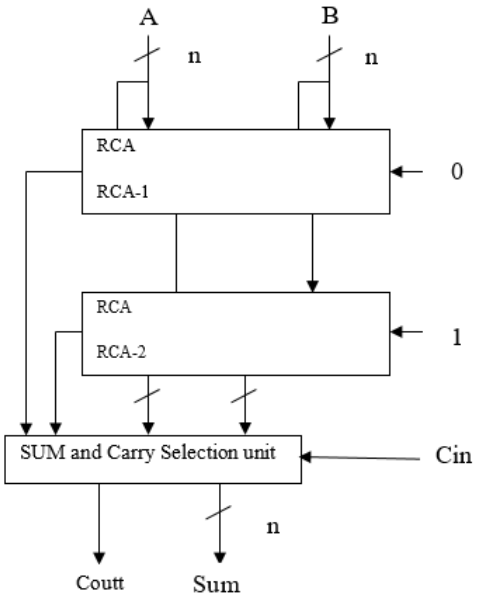

Figure 1. Dual RCA based SQRT-CSLA

5. RESULTS AND DISCUSSION

Simulation of the Dual RCA based SQRT-CSLA is done by Modelsim 6.3c simulation environment. It is a tool to simulate the design in individual manner. The simulation output is shown in Figure 2. It clearly shows the simulated output of the adder, and also shows the input and output in clear manner.

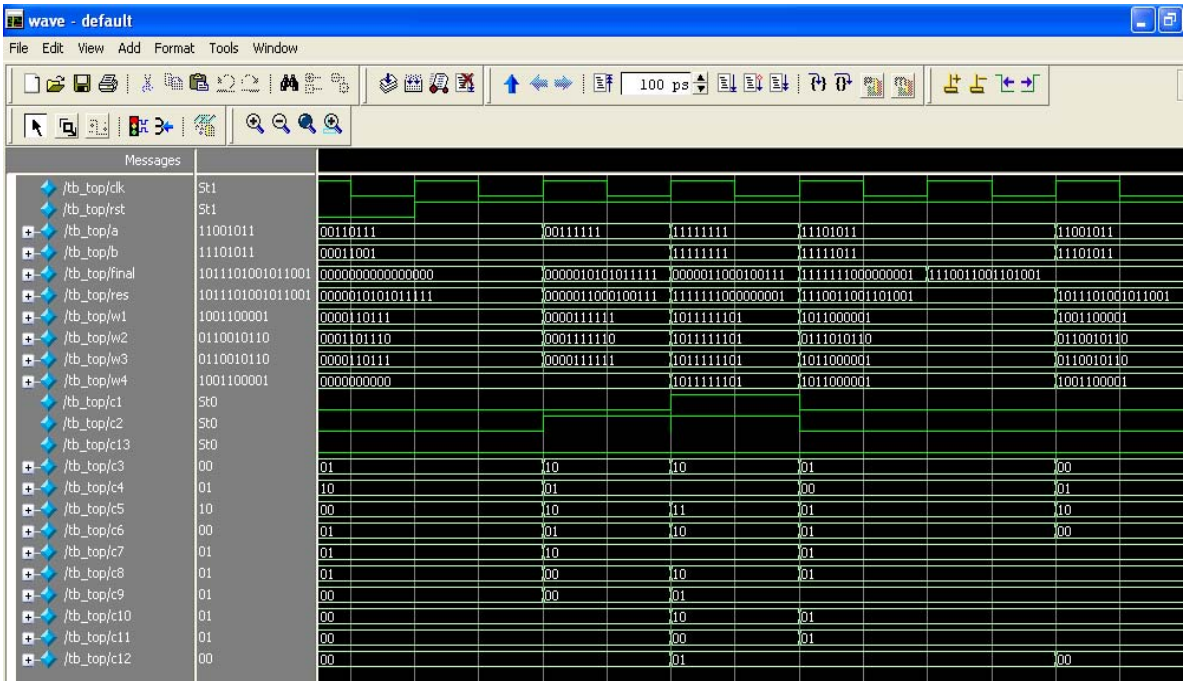

Figure 2. Simulation Output of Dual RCA based SQRT-CSLA

On the other hand the performance of the adder can be synthesized and evaluated by using Xilinx ISE 10.1 Simulation environment. It is used to evaluate the performance for the proposed adder. Performance

can be analyzed by Spartan 3 device with package (pq-208) and set the speed as -5. The analyzed results show in Table 1.

Table1. Comparison of Normal and Dual RCA based SQRT-CSLA

Parameters	Normal SQRT-CSLA	Dual RCA based SQRT-CSLA
LUTs	21	16
Occupied Slices	15	10
Delay (ns)	2.3ns	1.7ns
Power (W)	0.25w	0.21w

6. CONCLUSION

In this paper, Dual RCA based SQRT-CSLA adder was designed for high speed and low power applications. The efficient adder is applied into the FIR filter MAC unit. The performance of the adder is individually computed by using xilinx ISE tool. The proposed adder provides better results for area, delay and power. It takes less number of LUT and slices; also delay of the circuit is reduced. So it is suitable for efficient FIR filter design. It reduces the LUT and slices count up to 24% and achieves 26% reduction in delay and 16% reduction in power in the proposed adder.

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