High efficiency step-up converter using single switch with coupled inductors

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ABSTRACT

Due to high demand for voltage boosting in the field of renewable energy sources, a novel topology of step-up converter with single switch is proposed in this paper. The converter uses single switch with coupled inductors architecture. The proposed topology enables to control the stepping-up gain by adjusting the duty cycle and selecting appropriate turn ratio of the coupled inductors. The two coupled inductors in the circuit can act as a step-up transformer. Moreover, the proposed technique aims to harness the turning off voltage stresses across the switching element and suppress the stress by transferring it to the load. The switching induced voltage was reduced by forwarding the power to charge a capacitor then transfer the power through a diode to the output. Circuit configuration, principles of operation and the gain transfer function of the converter are demonstrated. The proposed circuit is verified by comparing the practical results to the theoretical.

Keywords: Continuous conduction mode Coupled inductors DC converter High voltage gain converter Step-up converter Switched capacitor

1. INTRODUCTION

Voltage boosting converters are widely used at front-end for many applications such as photovoltaic panels, fuel cells, batteries, renewable energy and micro-grid applications [1]-[11]. High gain, high efficiency with large current capability are the main concerns for designing step-up converters nowadays. However, the operation of traditional step-up direct current (DC) converters is companied with a considerable rate of voltage stresses on the switching elements of the converter. As the voltage gain of such converters is increased, the challenge to overcome the above concerns become much harder to solve. Therefore, during design process if the converter could not provide an alternative solution then it will end-up with an undesired content of switching losses that lead to poor efficiency. The switching noise is a result of the induced emf across the main inductor of the converter. Where the induced emf is a result of chopping the current through the main inductor during switching, according to $V_L = (L \cdot \frac{dI}{dt})$. Consequently, the induced emf is a function of the current magnitude, inductor value, and the rate of change.

Reducing voltage stress during the design was accomplished using the coupled inductors architecture with a capacitor. As an advantage of the new architecture, it reduces switching losses across the metal oxide semiconductor field effect transistor (MOSFET). Previous literatures investigated different connection of coupled inductors based on the coupled inductors’ ordination. Where the coupling ordination could be either inversely or directly; interleaved or loosely. Additionally, the inductors can be wound on multiple magnetic cores or composite on mutual magnetic core [12]-[14]. Moreover, the coupled inductors structure is preferable solution for higher power application, as it can provide weight and size reduction, and minimise losses of the electric and magnetic components. Therefore, this topology were the chose for different applications such as

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electric railway traction and electric vehicles [15]-[17]. Step-up converters using coupled inductors with switched capacitors are widely utilised for high voltage gain applications [18]-[27].

2. METHOD

2.1. Circuit description

The proposed circuit layout of the step-up converter is demonstrated in Figure 1. The circuit offers an improvement on the boost configuration [28]. The main input inductor \( L_{\text{in}} \) is connected in series with the source side. The delivered power is supplied to inversely coupled inductors \( L_1 \) and \( L_2 \), a snubbing capacitor is connected across \( L_2 \) to act as active snubber circuit. Power diodes \( D_1 \) and \( D_2 \) are connected to the end side of \( L_{\text{in}} \) and \( L_1 \), respectively, while the output filter capacitor \( C_o \) is connected at the load side to maintain the output voltage.

When the current passes through the input inductor \( L_{\text{in}} \), the line current is divided into two branches. These currents represent the power flow paths in the proposed converter circuit. The first route links the far end side of the main inductor \( L_{\text{in}} \) to the tap point of the inversely coupled inductors \( L_1 \) and \( L_2 \) which they are wound on the same toroidal core to configure both sides of the transformer \( T \). The second route links the far end side of the primary winding \( L_1 \) is linked into the power switch \( Q_1 \), while the far end side of the winding \( L_2 \) is linked into the load side of the converter circuit through the power diode \( D_2 \). At the output side of the converter circuit, the two power routes are combined by connecting the cathode sides of the two power diodes \( D_1 \) and \( D_2 \). A capacitor \( C_o \) is installed at the load side to filter out the undesired ripple.

2.2. Principle of operation

Relying on the duty cycles of the switch \( Q_1 \) and the turn-ratio of the transformer \( T \), the proposed converter gain can be controlled. The principles of continuous conduction mode (CCM) of operation for the step-up mode is debated in this section. In order to clarify the proposed converter operation, assumptions have been made:

- The parasitic components of power switches MOSFET and diodes are neglected.
- The internal resistance and parasitic capacitors of inductors are neglected.
- All diodes are considered ideal switches with zero forward voltage drop.
- The turn ratio of the transformer \( T \) is unity.
- The magnetic field of the main inductor \( L_{\text{in}} \) is not saturable.
- The mutual inductance of the \( (T) \) transformer is integrated to the primary winding \( L_1 \).

The proposed converter shown in Figure 1 has two states during operation depending on the switch condition, as it will be explained.

2.2.1. On status, \([Q_1 \text{ is on}]\)

When the transistor \( Q_1 \) is conducting, the line current (current through the input inductor \( L_{\text{in}} \)) is divided in to two divisions. The first path is through the \( L_1 \) and the MOSFET. However, when the applied voltage at the anode side of \( D_2 \) diode is reached to the value of potential on the load side, the diode turns into forward biased. As a consequent, the secondary windings of the transformer provides an alternative route for current to outflow through diode \( D_2 \) to the output side. Meanwhile, the capacitor \( C_1 \) will start charging to up
to $L_2$ voltage level $V_{L2}$ and cathode of $D_1$ diode is subjected to the load side voltage which results in being reversed biased. The proposed converter when $Q_1$ is on state is illustrated in Figure 2 with currents routes.

![Figure 2](image2.png)

**Figure 2. On status of the proposed step-up DC-DC converter**

### 2.2.2. Off status, [$Q_1$ is off]

When the transistor $Q_1$ is switched off, the $V_{L2}$ will rise suddenly due to the sudden rate of change in the $L_1$ current, during this period the $C_1$ act as reservoir to store turning off energy produced across $L_2$. By the end of transient period, the circuit will conduct through two paths. The first path is conducted, when the induced voltage by $L_{in} + V_1$ is higher than the load voltage causing the diode $D_2$ to conduct in forward biased leading to feed the load from the energised $L_{in}$ and the source. By the end of the off period, the voltage across the $L_{in}$ will be reduced causing a drop in the load voltage level. At this moment, the voltage across $C_1$ is higher than the voltage across $C_2$, causing the diode $D_2$ to switch into forward bias to feed the load with the charged power from $C_1$. Meanwhile, the body diode of the MOSFET is in conducting mode to close the circuit. Figure 3 shows the equivalent circuit of the proposed DC converter during Off state with currents path.

![Figure 3](image3.png)

**Figure 3. Off Stat of the proposed DC converter**

### 2.3. Transfer function

The proposed DC converter is capable to work as a high gain step-up power converter depending on the exercised sets of the duty cycles of the power switch $Q1$ and the turn ratio $n$ of the transformer $T$. The turn ratio can be any integer number taking into consideration the maximum permissible limits of voltage and current (rated values) of the used components in the converter prototype. The transfer function of the new step-up DC converter in CCM and normal loading condition is introduced in this section. The transfer function could be extracted by determining the rate of alteration in the line current at the two operating conditions of the converter (on and off statuses). The current in the converter circuit means the outflowing current in the prime inductor $i_{L_{in}}$. 
Starting with the key variable’s definitions in the below derivation: \( i_{\text{max}} \) is the maximum amplitude value of \( i_{\text{Lin}} \), \( i_{\text{min}} \) is the minimum amplitude value of \( i_{\text{Lin}} \), \( t_1 \) is the duration time of on status interval, \( t_2 \) is the duration time of off status interval, \( t_1 + t_2 = \tau \), where \( \tau \) is the period of one cycle of the applied frequency.

\[
    i_{\text{in}} = i_{\text{Lin}}
\]

\[
    V_{\text{Lin}} = V_{\text{in}} - V_{\text{out}} = L_{\text{in}} \left( \frac{di_{\text{Lin}}}{dt} \right)
\]

Where, \( i_{\text{in}} \) is the line or input current, \( V_{\text{in}} \) is the supply or input voltage, \( V_{\text{out}} \) is the output (terminal) voltage, \( V_{\text{Lin}} \) is the applied voltage across the prime inductor \( L_{\text{in}} \). The final expression of the duty cycle of the proposed step-up DC-DC converter can be expressed as in (3),

\[
    \frac{V_{\text{out}}}{V_{\text{in}}} = 1 + \frac{\eta D}{2}
\]

where, \( D \) is the applied duty cycle of the power switch \( Q_1 \), \( \eta \) is the turn ratio of the transformer \( T \).

3. RESULTS AND DISCUSSION
3.1. Experimental results
A prototype of the proposed converter was designed and fabricated. The gain equation was derived and the performance of the proposed converter was evaluated. The obtained practical results were compared to the theoretical results. The results obtained from both schemes were in accordance to each other. A single case study was selected to demonstrate the performance in this section. Table 1 shows the applied supply voltage, the applied load, and the duty cycle \( D \) of power switch \( Q_1 \). The parameters values of the prototype used for this case study is presented in Table 2. Figure 4 shows the obtained current waveforms during the experimental test.

Table 1. Testing conditions of case study

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{in}} )</td>
<td>14 V</td>
</tr>
<tr>
<td>( D )</td>
<td>50 %</td>
</tr>
<tr>
<td>( R_{\text{load}} )</td>
<td>11 Ω</td>
</tr>
</tbody>
</table>

Table 2. Experimental parameters value

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_1, L_2 )</td>
<td>150 μH</td>
</tr>
<tr>
<td>( L_{\text{in}} )</td>
<td>1.5 mH</td>
</tr>
<tr>
<td>( C_0 )</td>
<td>100 μF</td>
</tr>
<tr>
<td>( C_1 )</td>
<td>20 nF</td>
</tr>
</tbody>
</table>

Figure 4. Experimental waveforms of currents of selected case study: (a) diode current \( i_{D1} \), (b) diode current \( i_{D2} \), and (c) output current \( i_{\text{out}} \)
Figure 4(a) shows the current through the diode D1, where the current is passing through it during the off time of the MOSFET. Likewise, Figure 4(b) shows the current will appear through D2 when the MOSFET is on. Figure 5 shows reduction of voltage stress on the transistor, where Figure 5(a) shows the effect of the capacitor C1 during switching. When C1 was removed the voltage on the MOSFET increased to 66 V as in Figure 5(b). It is clear that the capacitor contributed to reduce the voltage by 30 volts, which verify the design.

![Figure 4(a)](image)

**Figure 4.** Current through the diode D1, (a) MOSSFET is off, (b) MOSSFET is on

![Figure 5(a,b)](image)

**Figure 5.** Reduction of voltage stress drain to source voltage: (a) with C1, and (b) without C1

### 3.2. Case studies results

A case studies was undertaken to verify the performance of the proposed system. The following experimental cases Table 3 were applied. During each case, full range of duty cycles to control the power switch Q1 was considered. During each test, the operating frequency was set to 120 kHz. The results of the tests are illustrated in Figure 6.

<table>
<thead>
<tr>
<th>Supply voltage (V)</th>
<th>Equivalent load resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>22</td>
</tr>
<tr>
<td>14</td>
<td>44</td>
</tr>
<tr>
<td>20</td>
<td>66</td>
</tr>
</tbody>
</table>

![Table 3. Test conditions](image)

**Table 3. Test conditions**

The experimental results prove the validity of the derive transfer function noted in (3). The y-axis represent the ratio of $V_{out}/V_{in}$, while the x-axis is the characterise the duty cycle D. For distinctness the line (y=x), which symbolize (3) is also presented. The linearity performance of the proposed system is clearly demonstrated in Figure 6. It shows the examined performance of the new converter under vast variety of loading conditions and duty cycles. Likewise, the Figure 6 shows there is a slight perversion in several test points from the equivalence line of the analytical deduced duty cycle line. The perversion being

![Figure 6](image)

**Figure 6.** Experimental results of range of case studies

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distinguishable as the applied duty cycle of the power switch $Q_1$ exceed the rate of 50%. The test outcomes confirm the correspondence between the experimental and analytical outcomes of the new converter circuit. The small differences between test points were caused by the effect of the neglected parasitic elements. Furthermore, results are considered as clear indicator for slight rate of switching noise and losses for the proposed converter.

4. CONCLUSION

The proposed topology of the DC converter employs inversely coupled inductors architecture. This topology can provide high voltage gain when working on transformer mode. Secondly, the inversely coupled inductors provided an auxiliary current path, where the current flows to the load even when the switch $Q_1$ is closed. Furthermore, during the turning off process of the switch, the induced e.m.f across the L1 transferred to the load, which reduces voltage stress across the switching element. However, the C1 value should kept to minimum and tuned to the off time of the MOSFET. The proposed architecture, successfully maintaining the current ripple in the main inductor to minimum. Maintaining low ripple in the input current will lead to reduce the input inductor size. Consequently, minimizing the input inductor value and voltage stress helped to reduce losses and improve the converter efficiency, where it reached to 96%. Likewise, the reduction in current ripple and voltage stress reduced the electromagnetic interference (EMI) level of the converter. The prototype of the proposed step-up converter was designed, build and tested. The purpose is verified theoretically and experimentally, where the obtained results of both cases were identical.

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REFERENCES


High efficiency step-up converter using single switch with coupled inductors ... (Ali Hassein Al-omari)
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