Design of 130nm RFCMOS differential low noise amplifier

Maizan Muhamat¹, Hanim Hussin², Norhayati Soin³

¹,²Faculty of Electrical Engineering, Universiti Teknologi MARA, Malaysia
³Department of Electrical Engineering, Faculty of Engineering, University of Malaya, Malaysia

ABSTRACT

In this paper, an inductively degenerated CMOS differential low noise amplifier circuit topology is presented. This low noise amplifier is intended to be used for wireless LAN application. The differential low noise amplifier proposed provide high gain, low noise and large superior out of band IIP3. The LNA is designed in 130 nm CMOS technology. Simulated results of gain and NF at 2.4GHz are 20.46 dB and 2.59 dB, respectively. While the simulated S11 and S22 are −11.18 dB and −9.49 dB, respectively. The IIP3 is −9.05 dBm. The LNA consumes 3.4 mW power from 1.2V supply.

1. INTRODUCTION

Nowadays the wireless communication demand is increasing due to the development of technology. A wireless system comprises of a back-end and front-end section. Analog signal is being process in the front-end section in the high radio frequency, While analog and digital signal is processed at the back-end section in baseband of low frequency range. Radio frequency (RF) refers to the frequency range in the electromagnetic spectrum that is used for radio communications [1]. Typically, the frequency lies from 100 kHz to 100 GHz. In general baseband frequency is below 1 GHz while those bigger than 1 GHz describes as RF. The mainstream of radio frequency communication receiver is the Low Noise Amplifier (LNA). Low noise amplifier which is in the RF front-end circuit has the great value in this field [2]. It main purpose is to provide gain while preserving the input signal-to-noise ratio of the output which is important characteristic because the receiver signals usually weak [3, 4]. Besides that, the characteristic of good LNA is shown in Figure 1.

There are many topologies in the LNA which are series shunt feedback, resistive termination, common gate connection and inductive degeneration. In LNA circuit architecture, inductively degenerated common source is the most used topology as the ability of good input impedance matching. Due to the basic topology of the inductively degenerated cascode LNA it is chosen to be implement to most of varisties of presently available of LNA. It allow maximum gain under low power constraint [5-7].

This paper present a design of 2.4 GHz RFMOS Differential LNA which is used to improve performance of differential LNA. The aim of this paper is to provide differential LNA that have low power consumption but still have acceptable performance of noise, linearity that acceptable and high range of dynamic.
2. **RESEARCH METHOD**

In order to gain simultaneous input and noise matching, the source inductor is used. The value of desired input resistance is 50 Ohm. Structure of cascode is a combination of a common-gate load and it effect the increasing of output impedance. Device of additional cascode has a diode. The inductor between the cascode source and supply blocks any RF is leaking to the supply rail and maybe varied in value to optimize the gain response of the LNA. Figure 2 represents a half of final differential LNA. By using the inductive degeneration $L_s$ the topology is matched to 50 $\Omega$. The parameter is often expressed by $S_{11}$. LNA input impedance expression is defined in (1).

$$Z_{in}(s) = L_s \parallel (L_{GS} + L_{SS} + \frac{1}{C_{TS}} + \frac{g_m L_s}{C_T})$$ (1)

The $Z_{in}$ should be 50 $\Omega$ to achieve input matching, so:

$$Z_{in} = \frac{g_m}{C_{gs}} L_s$$ (2)

In most LNA design the value of $L_s$ was assumed and the values of $g_m$ and $C_{gs}$ are calculated based on the formula to find the required for $Z_{in}$ [8]:

$$\omega_T \approx \frac{g_m}{C_{gs}} = \frac{R_s}{L_s}$$ (3)

where $\omega_T$ is defined as a cut-off frequency. The value of the $R_s$ is 50$\Omega$ [9], the optimal Q factor of inductor;

$$Q_L = \sqrt{1 + \left(\frac{1}{\rho}\right)}$$ (4)

where $\rho = \frac{\sigma \alpha^2}{g_Y}$. For parameter $\rho$ usually depend on the RFCMOS technology, but typically $\gamma$ is set between 2-3, $\sigma$ is set to 2-3 times the value of $Y$ and the $\alpha$ assumed to be 0.8-1 [9]. The gate inductance, $L_g$ obtained based on;

$$L_g = \frac{Q_L R_s}{\omega_0}, L_s$$ (5)

while the gate source capacitance, $C_{gs}$ was determined by:

$$C_{gs} = \frac{1}{\omega_0^2 (L_g + L_s)}$$ (6)

$$C_{gs} = \frac{2}{3} C_{ox} W \cdot L_{min}$$ (7)
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(8)

\[ W = \frac{3}{2} \frac{C_{gs}}{C_{ox \cdot L_{min}}} \]

Where \( \varepsilon_{0} = \) dielectric constant for free space 8.854E\(^{-14}\) F/cm and \( \varepsilon_{o} = \) dielectric constant for silicon 3.9 \[9\]. Then, the optimum noise figure, \( NF_{\text{Opt}} \), can be found as below in (9):

\[ NF_{\text{Opt}} = 1 + \frac{2\gamma}{\alpha} \left( \frac{\omega_{o}}{\omega_{T}} \right) \sqrt{p} \left( |c| + \sqrt{p} + \sqrt{1 + p} \right) \]

(9)

circuit is stable unconditionally when \( K > 1 \) it means that \( \Delta < 1 \). According to the meaning of the stability figure;

\[ K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|}{2|S_{22}S_{12}|} \]

(10)

\[ \Delta = S_{11}S_{22} - S_{12}S_{21} \]

(11)

Figure 2(a) shows the schematic circuit of a single ended cascode common source amplifier for input impedance matching with the gate inductor. The differential of LNA schematic circuit is shown in Figure 2(b). Many advantages can be gain by the differential LNA over single ended LNA. A stable reference point is offer by the DLNA compared to the single ended. Second, the noise in the circuit can be reduced by using the differential LNA. The composite signal swing of the differential signal can be twice that of the single ended swing on the same power supply, increasing the signal-to-noise ratio \[10 - 12\]. The amplifier alternatively can be increased on the same power supply, distortion will be low, or a low power supply voltage can be used in order to provide same signal swing and lowering the power dissipation \[13 - 15\]. Besides that, an image rejection scheme and the use of Gilbert mixers are required to be fed from a differential source \[16\].

The signal of the differential amplification ensures an attenuation of the common mode signal which is in the most system the common mode signal will be noise \[17\]. The virtual ground formed at the tail removes the sensitivity to parasitic ground inductances which makes the real part of the input impedance purely controlled by \( L_s \) \[18, 19\]. The balun transformer supply the differential input voltage in the circuit. The balun (a contraction of balanced-unbalanced) is a two-port component placed between a source and load when a differential, balanced RF functional block must connect to a single-ended, ground-referenced one \[20\]. While at the tail of this stage the ideal current source is added. Source impedance of an ideal current source is an infinite. Table 1 shows the list of components and value for the differential LNA design.

![Figure 2](image-url)
### Table 1. List of components and values

<table>
<thead>
<tr>
<th>Components</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_1$</td>
<td>10 KOhm</td>
</tr>
<tr>
<td>$R_2$</td>
<td>10 KOhm</td>
</tr>
<tr>
<td>$C_1, C_2, C_3, C_4$</td>
<td>10 pF</td>
</tr>
<tr>
<td>$L_g$</td>
<td>0.5nH</td>
</tr>
<tr>
<td>$L_s$</td>
<td>9nH</td>
</tr>
<tr>
<td>$M_1, M_2$</td>
<td>W= 2 um, L= 0.13um</td>
</tr>
<tr>
<td>$M_3, M_4$</td>
<td>W= 126 um, L= 0.13um</td>
</tr>
<tr>
<td>$M_5$</td>
<td>W= 136 um, L= 0.13um</td>
</tr>
</tbody>
</table>

### 3. RESULTS AND ANALYSIS

The $S$-parameter plots, and noise performances are shown in Figure 3 to Figure 4 respectively. As can be seen from Figure 4, the circuit’s input and output were matched to the 50 Ω required at the operating frequency of 2.4 GHz. The LNA is simulated using 0.13 um technology of CMOS process with 1.2 V supply.

From the Figure 3(a), the simulation of LNA show the input matching, $S_{11}$ gained versus frequency is -11.18 dB. The maximum gain that the differential amplifier provides is 23.46 dB as shown in Figure 3(a) while the output matching $S_{22}$ is -9.492 dB. The $S_{12}$ is -39.71 dB at 2.4 GHz. As depicted in Figure 4, the noise figure reading is 2.58 dB and the IIP3 is -9.05dBm.

From all the above result gained from the simulation, the circuit provide high gain, high stability, low noise figure and low IIP3. In Table 2, a comparison of the simulated LNA characteristic is included. The proposed CMOS LNA in this paper is reported to have a best value among the other CMOS LNA while comparing the characteristic.

![Figure 3. Graph of simulated s-parameter for pre-layout performance of differential LNA: (a) $S_{11}$ and $S_{22}$, (b) $S_{21}$ and $S_{12}$](image-url)
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This paper presents a simulation of a 2.4 GHz CMOS differential LNA using 0.13µm technology. The designed LNA achieved a power gain (S21) of 23.46 dB and a minimum noise figure (NF) of 2.5 dB from a supply of voltage 1.2V. While the power consumption of the proposed design is 3.24 mW. All the results obtained meet the specifications of RFCMOS Differential LNA which is low NF, high gain performance, high stability and low consumption power.

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REFERENCES


BIOGRAPHIES OF AUTHORS

Maizan Muhamad graduated from Universiti Tenaga Nasional (Uniten) with the B. Eng (Hons) in electrical & Electronic Engineering in 2002. She was with Panasonic Electronic Devices (Pedma) serve as a Quality Control Engineer in Petaling Jaya from 2002 until 2005. She obtained her M.Sc degree from Universiti Kebangsaan Malaysia (UKM) in 2007. She is currently a senior lecturer in Universiti Teknologi MARA (UiTM), Selangor, working in the area of RF integrated circuit (RFIC). She received her Ph.D degree in the field of analog IC design from Universiti of Malaysia in 2019. Dr Muhamad is a member of the Institute of Electronics, Information, and Communication Engineers. She is a Professional Engineer registered under the Board of Engineers Malaysia.
Hanim Hussin received the B. Eng (Hons.) and M.Sc degrees from the National University of Malaya (UKM), Malaysia, in 2004 and 2006 respectively, and the Ph.D degree from the University of Malaya (UM) Malaysia, in 2015. She is currently a Senior Lecturer in Universiti Teknologi MARA and focusing on reliability issues of nano-CMOS devices and CMOS circuit application.

Norhayati Soin received the B. Eng. (Hons) degree in electrical and electronics engineering from the Liverpool Polytechnic, United Kingdom and MSc from Liverpool John Moores University in 1999. She got her PhD in Universiti Kebangsaan Malaysia (UKM) in 2006. She is currently a Professor at University of Malaya and focusing on modelling of nano-CMOS devices.