## Novel Zeta Converter with Multi Level Inverter Connected to Grid

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Article Info	ABSTRACT				
Article history:	The usage of multilevel inverter has increased in a drastic manner for the past				
Received Nov 25, 2017 Revised Jan 9, 2018 Accepted May 27, 2018	years. These novel inverters are useful in various mega power applications. As they are having the ability to change the output waveforms, they are having good harmonic distortions and better output results. This work proposes a novel five level asymmetrical inverter which is incorporated with the zeta converter. Comparison is made with the existing multilevel inverter				
Keywords:	with the proposed system. The simulation results give the proposed system has less THD [1] when compared to the existing multilevel inverters. The				
Multilevel inverter THD Zeta converter	main objective is that the number of switches and capacitors are reduced which in turn reduces the loss and the cost. From the output results is ha been proved that the proposed topology gives reduced loss and high quality output when compared with the conventional methods.				
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## 1. INTRODUCTION

Multilevel inverters are having the ability of yielding high quality output waveform with the help of low power devices with reduction of switching losses lead to high demand. The array of inverters consisting of power semiconductor devices and capacitor banks will generate stepped up form of output voltage waveforms. Adding of switches allow the voltages across the capacitor to reach at a max level at the output end. The primary merits of the multi level inverters are

- a. They are able to give the output current with less distortion.
- b. Common mode voltages will be eliminated.
- c. They can work with minimum switching frequencies.
- d. They will take the input current with [2] low distortion.

The multilevel inverters have been implemented for several applications like motor drive, power conditioning devices, generation of power from renewable energy sources and also distribution system.

## 2. CONVENTIONAL ZETA CONVERTER

The Figure 1 shows the basic structure of conventional zeta converter. It is basically a fourth-order DC-DC converter. The structure comprises of two inductors and two capacitors which can be operated either in step-up mode or step-down mode. A linear regulator achieves the required output voltage by dissipating power loss in resistors or in pass transistors. It regulates the output voltage or current by sacrificing excessive power as heat and thus the maximum efficiency can be achieved since the difference in voltages are taken as waste.



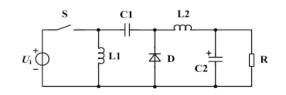


Figure 1. Basic structure of conventional zeta converter

The major disadvantages of zeta converter:

- a. The input current is discontinuous
- b. Voltage gain is limited and low
- c. Gives an oscillating output

## 3. CONVENTIONAL MULTI LEVEL INVERTER

The Figure 2 shows a conventional cascaded H bridge [2] five level multilevel inverter. It consists of two H bridges inverters fed by voltage sources. Here the output voltage wave form will be addition of all independent voltages since the H bridges [5] are arranged in series. The total output voltage is calculated by

$$Vo = V_1 + V_2$$

Where: Vo is the output voltage and  $V_1 \& V_2$  are independent voltages.

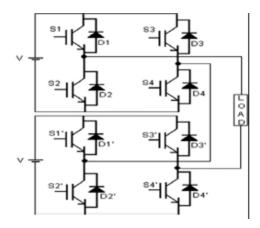


Figure 2. Five level cascaded H-bridge multilevel inverter

It can be noted that this arrangement gives five levels of voltages 2V, V, 0, -V, -2V. The primary merit of this arrangement is that it needs less number of components. Even though it has some demerits like it needs more components when the voltage level needed to be increased. This leads to increase of number of switches, voltage source, cost and weight. These multilevel inverters [4] have been applied and high power application mainly in the field of multilevel motors drive giving distorted output voltage.

## 4. PROPOSED MULTI LEVEL INVERTER FED FROM ZETA

The proposed multi level inverter fed from zeta converter is shown in the Figure 3 this system has a conventional zeta converter properly connected with the five level multi level inverter for high power applications. The zeta converter consists of capacitor, inductor, controlling switch in addition to that Diode  $D_2$  and a switch  $S_1$  is connected in series. Similarly multilevel converter consists of two capacitors ( $C_2$ ,  $C_3$ ), two diodes ( $D_3$ ,  $D_4$ ) and six switches ( $S_3$ ,  $S_4$ ,  $S_5$ ,  $S_6$ ,  $S_7$ ,  $S_8$ ).

The switches  $S_5$ ,  $S_6$  are connected in series but connected in parallel with the switches  $S_7$ ,  $S_8$  as they are connected in series forming H bridge. The load is connected in parallel between the serially connected switches.

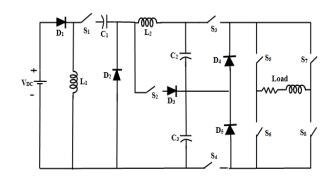


Figure 3. Proposed multilevel five level inverter

By properly controlling the auxiliary switches, different levels of output voltages can be generated. Normally these inverters have five levels of voltages ie 2V, V, 0, -V, -2V. Table 1 shows the switching operations for getting different levels of output voltages. Here  $S_1$  and  $S_2$  switches are ON and  $S_3$ ,  $S_4$ ,  $S_5$ ,  $S_6$ ,  $S_7$  &  $S_8$  switches are switched ON and OFF depending upon the requirement.

	Table 1. Switch	<b>Controls</b>	of the Pro	posed System
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S3	S4	S5	S6	S7	S8	Vout
1	1	0	0	0	0	0
1	0	1	0	0	1	V
1	1	1	0	0	1	2V
0	1	0	1	1	0	-V
1	1	0	1	1	0	-2V

# 5. MODES OF OPERATION Mode I

The inverter is operated in different operating modes for achieving different voltage levels. Figure 4 shows mode I operation where the switches  $S_3$ ,  $S_5$  and  $S_8$  are closed with  $S_4$ ,  $S_6$  and  $S_7$  are opened. Hence the circuit is closed using switches  $S_3$ ,  $S_5$ , Load and  $S_8$  in the forward direction ant the net output available voltage at the load is the voltage across  $C_3$  ie V.

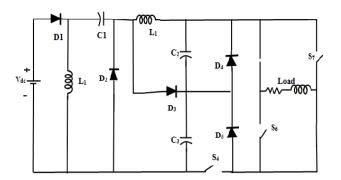


Figure 4. Mode I operation of proposed multilevel five level inverter

## Mode II

In mode II, the switches  $S_4$ ,  $S_6$ , and  $S_7$  are closed leaving other switches to open. The circuit is closed through load in the reverse direction and the voltage available at the load is -V. The operation of circuit is shown in Figure 5.



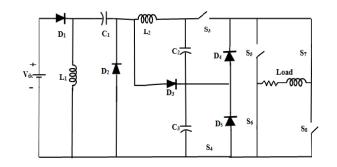


Figure 5. Mode II operation of proposed multilevel five level inverter

## Mode III

In this mode,  $S_3$ ,  $S_4$ ,  $S_5$  and  $S_8$  switches are closed through the load and so the capacitor voltages  $C_2$  and  $C_3$  will be available at the load ie 2V. The operating circuit is shown in Figure 6.

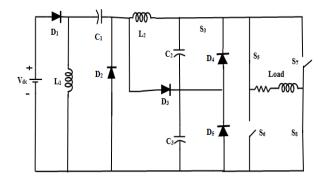


Figure 6. Mode III operation of proposed multilevel five level inverter

## Mode IV

This mode of operation is explained in Figure 7 where the switches  $S_3$ ,  $S_4$ ,  $S_6$  and  $S_7$  are connected through the load. Hence the output voltage available at the load is -2V.

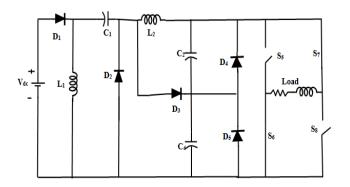


Figure 7. Mode IV operation of proposed multilevel five level inverter

## Pulse width modulation.

For generating the switching pulses multi carrier PSPWM [3] an embedded MATLAB functions are taken. In the multi carrier, the frequency and amplitude of triangular carrier are same as well as the phase[6] shift between adjacent carrier. Figure 8 shows multi carrier phase shift PWM [7] and embedded with MATLAB functions.

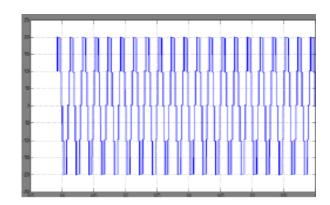


Figure 8. Cascaded multi level H bridge inverter output waveform using multi carrier modulation

## 6. SIMULATION DIAGRAM

The proposed topology was simulated with RL load. The Figure 9 shows the simulation diagram with multi carrier modulation. The output waveform of the proposed five level multi level inverter is given in Figure 10. An analysis was made for total harmonic distortion and the results obtained are given in Table 2. A comparison was made [8]-[10] with zeta converter multilevel inverter and conventional multilevel inverter.

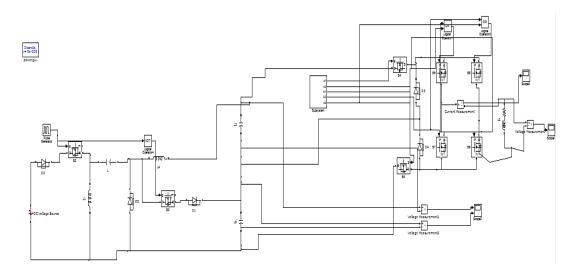


Figure 9. Simulation diagram of proposed method

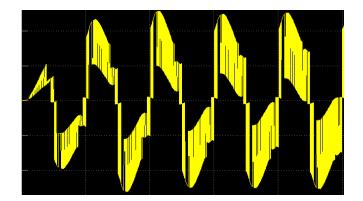


Figure 10. Output voltage waveform of proposed system

Figure 11 shows the voltage waveform after the zeta converter. The converter is fed with DC voltage of 90V and as the converter is the boost converter the source voltage is increased to 170V before the capacitors. The voltage available across the capacitors C1 & C2 is shown in Figure 12.

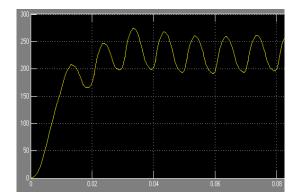


Figure 11. Output voltage waveform of zeta converter

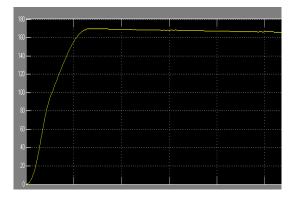


Figure 12. Output voltage across the  $C_1 \& C_2$ 

Figure 13 shows the output current waveform in the RL load and Figure 14 shows the Total Harmonic Distortion in percentage of the proposed system which is around 5.80%.

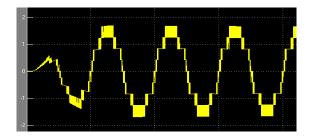


Figure 13. Output current waveform of the proposed system

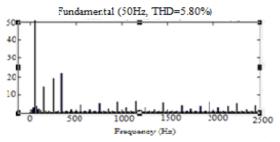


Figure 14. Modified five level multi level inverter THD 5.80%

Table 2. Comparison of Different Five Levels of MLI							
Topology	No of sources	No of capacitors	No of transformers	No of switches	phase to neutral voltage	T otal T HD	
H bridge with singl e input source with transfomer	1	0	6	8	170.5	20.05%	
H bridge with one DC source	1	0	0	8	162.2	17.25%	
Proposed topology	1	2	0	6	240	5.80%	

#### 7. CONCLUSION

In this paper a new multi level inverter injected from zeta converter is proposed. The structure of the zeta converter is modeified and the output voltage of the zeta converter is splitted into two voltages with same voltage levels with the help of capacitors. As the vpltages are equal and is fed to the H bridge of MILa five level 240V output voltage is generated. Here the input dc voltage of 70V DC is increased to 240V AC which can be easily synchronised with the AC grid. The results show that the output voltage of multilevel five level inverter. The simulation output shows that THD of the proposed system is decreased and is 5.80% with reduced number of components which leads to less cost and complexity. The comparison between the proposed system and the existing system shows that the output voltage is increased up to 70V that is 29.19% of increment in voltage.

## REFERENCES

- Nasrudin Abd. Rahim, Mohamad Fathi Mohamad Elias, Wooi Ping Hew, *IEEE transaction. Industry Electronics*, "Design of filter to reduce harmonic distortion in industrial power system", Vol. 60, No: 8, 2943-2956, August 2013.
- [2] J. Selvaraj and NA Rahim, "Multilevel Inverter For Grid-Connected PV System Employing Digital PI Controller", IEEE Trans. Ind. Electron., vol. 56, pp. 149-158, 2009.
- [3] Naderi and A. Rahmati, "Phase-Shifted Carrier PWM Technique for General Cascaded Inverters", *IEEE Trans. Power Electron.* vol. 23, pp. 1257-1269, 2008.
- [4] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications", *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [5] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A Survey on cascaded multilevel inverters", *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197-2206, July 2010.
- [6] S. J. Park, F. S. Kang, M. H. Lee, and C. U. Kim, "A new single-phase five-level PWM inverter employing a deadbeat control scheme", *IEEE Trans. Power Electron.*, vol. 18, no. 18, pp. 831–843, May 2003.
- [7] N. A. Rahim, and J. Selvaraj, "Multistring five-level inverter with novel PWM control scheme for PV application", *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2111-2123, June 2010.
- [8] B. Jyothi, M. Venugopala Rao, "Performance analysis of 3 level 5 phase multilevel inverter topologies" International journal of electrical and computer engineering (IJECE), Vol 7, No 4, 2017, pp 1696-1705.
- [9] Mohd Ruddin Ab Ghani, Nabin Frah, Junifa Lazi,' "Investigation study of three level cascaded H bridge multilevel invertr", *TELKOMNIKA (Telecommunication, Computing, Electronics and Control)*, Vol 15, No 1, March 2017, pp125-137.
- [10] Auzani Jidin. Svamim Sansui, Tole Sutikno, Nik Rumzi Nik, *TELKOMNIKA (Telecommunication, Computing, Electronics and Control)*, Vol14, No 2, June 2016, pp 387-389.