

## A concurrent Dual-band CMOS low noise amplifier at 2.4/5.2 GHz for WLAN applications

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### ABSTRACT

This paper presents a concurrent dual-band CMOS low noise amplifier (LNA) at operating frequency of 2.4 GHz and 5.2 GHz for WLAN applications. The proposed LNA employed cascode common source to obtain high gain using 0.13- $\mu\text{m}$  CMOS technology. The concurrent dual-band frequencies are matched using LC network band-pass and band-stop notch filter at the input and output stages. The filters help to shape the frequency response of the proposed LNA. The simulation results indicate that the LNA achieves a forward gain of 21.8 dB and 14.22 dB, input return loss of -18 dB and -14 dB at 2.4 GHz and 5.2 GHz, respectively. The noise figure of 4.1 dB and 3.5 dB with the input third-order intercept points 7 dBm and 10 dBm are obtained at 2.4 GHz and 5.2 GHz, respectively. The LNA dissipates 2.4 mW power at 1.2 V supply voltage with a chip size of 1.69 mm<sup>2</sup>.

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## 1. INTRODUCTION

Wireless Local Access Network or WLAN has been used tremendously nowadays with various technologies that mounted rapidly. In order to transmit and receive data, wireless LAN uses radio frequency signal, infrared or microwave as medium of transmission without using cables [1]. Whenever a transmitter or an antenna transmit RF signal to the receiver, the signal becomes weak and have high possibility to contaminate with noise from surrounding [2]. Thus, a successful amplifier is needed to amplify the signal and decreasing the noise significantly. This leads to the design of LNA or Low Noise Amplifier. The LNA amplifiers which indeed a low noise and it is appropriate compared to other receiver due to its high selectivity and contain more sensitivity via a narrow-band at just one input frequency [3-4]. In previous proposed LNA project, the implementation on single-band frequencies is reported to reach gain and matching at single band frequencies of interest. However, the needs to have an effective dual-band receiver in RF communication system are crucial because it increase the usability of the LNA for those WLAN applications. Furthermore, the concurrent dual-band topology will utilize the characteristic of wideband in CMOS [5].

The key to achieve dual-band characteristics is by dual-band concurrent technique which allows the matching simultaneously without any switching operation [6]. The switching technique will leads to unnecessary increase in area and cost [7]. In the case of LNA, noise figure are a vital consideration as the LNA receives a very weak input signal [8]. While the LNA is an active block in receiving chain, the noise figure sets at the LNA stages are the minimum value of noise at the entire system. This is due to the noise in each stage will decrease as the gain is increased. Another circumstances involved in designing the low noise amplifier which are the gain that can be produced in entire LNA design [9]. For the number of MOS

transistor used in this design, the internal gain that can possibly be produced by each stages must be enough to contribute a strong signal with adequate gain at the output [10]. Thus, a cascode stages are implemented to improve the entire LNA gain.

**2. DESIGN IMPLEMENTATION**

Figure 1 shows the proposed dual band LNA using CMOS 0.13- $\mu$ m technology. The LNA is implemented using a cascode CMOS stages with a combination of a common-source (CS) and a common-gate (CG) transistor. One of the main advantages of cascode topology is high gain and better reverse isolation. Each gate of the transistor is biased with a 5 k $\Omega$  resistor for R1 and R2. The function of resistor is to control the current flow from the DC voltage of Vg1 and Vg2. The current flowing through each of the transistor is the minimum value of current and hence the transistor can be protected from high current. A bypass capacitor is added at the input and output terminal to block dc sources and bypass ac sources [11]. Capacitor C3 is added to the gate of transistor M2 in order to provide an ac ground. This simply means that an ac signal which passes through the capacitor C3 is to be grounded. Therefore, no current will flow via an AC ground. In order to enhance the gain of LNA, inductor L3 is added at the gate of common gate transistor. A small signal equivalent circuit of CG transistor and L<sub>3</sub> is illustrated in Figure 2.

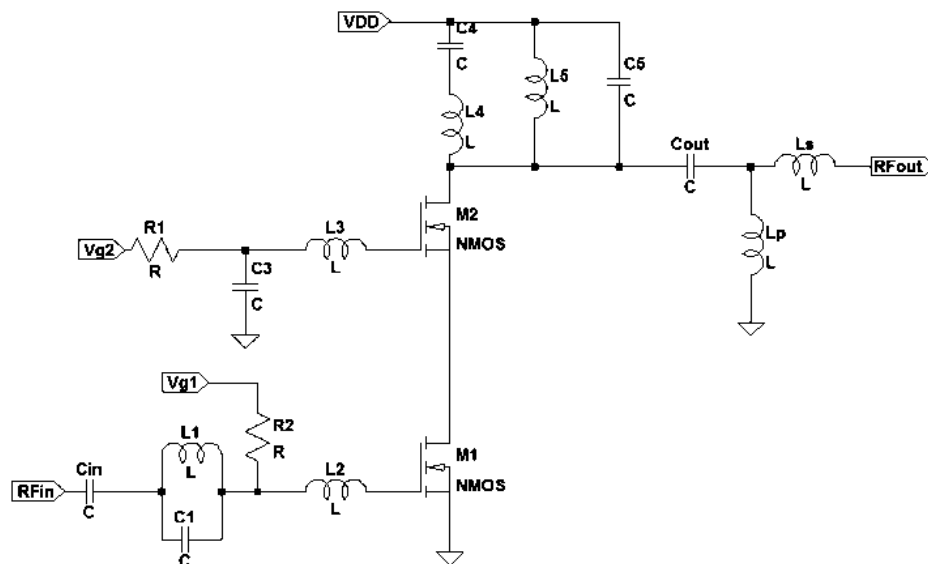


Figure 1. The proposed dual band LNA for 2.4 GHz and 5.2 GHz

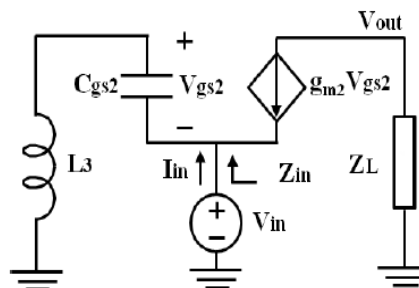


Figure 2. A small signal equivalent circuit of CG transistor and L<sub>3</sub>

Based on the equivalent circuit in Figure 2, the gate to drain capacitance C<sub>gd2</sub> are neglected. Thus, V<sub>gs2</sub> can be expressed as follows:

$$V_{gs2} = \frac{-\left(\frac{1}{j\omega C_{gs2}}\right)V_{in}}{\left(\frac{1}{j\omega C_{gs2}}\right) + j\omega L_3} = \frac{-V_{in}}{1 - \omega^2 L_3 C_{gs2}} \tag{1}$$

The  $C_{gs2}$  and  $\omega$  are the capacitance of gate to source and the operating frequencies of M2, respectively. Referred to (1), the amplitude of gate to source voltage ( $V_{gs2}$ ) of transistor M2 will be increased if  $|1 - \omega^2 L_3 C_{gs2}|$  is less than 1. As a result, the transconductance of M2 are improved uniformly which leads to enhancement of the gain of LNA. However, the improvement of the gain is restricted with value inductor  $L_3$ . If the value is larger, it will contribute to non-stability of the LNA circuit which includes the negative resistance at the common gate transistor. The reason can be shown by deriving  $I_{in}$  and  $Z_{in}$  which is the input current and input impedance respectively at the M1 transistor as follows:

$$I_{in} = \frac{V_{in}}{\frac{1}{j\omega C_{gs2}} + j\omega L_3} + \frac{g_{m2} \left(\frac{1}{j\omega C_{gs2}}\right)V_{in}}{\frac{1}{j\omega C_{gs2}} + j\omega L_3} \tag{2}$$

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{g_{m2} + j\omega C_{gs2}} \times (1 - \omega^2 L_3 C_{gs2}) \tag{3}$$

Another important feature in this LNA design is the absence of inductive source degeneration at the common source of M1. The inductive source degeneration will degenerate the gain of LNA. However, this could leads to linearity distortion and low quality noise figure [12]. The operation of matching networks at input and output of dual-band LNA is accomplished by concurrent technique instead of switching technique. This is due to the concurrent technique allows matching operation simultaneously. Hence, it consumes less power and reducing the chip area. Typically, one of the important factors that reduce the gain of LNA is the low Quality Factor (Q-factor) of CMOS inductor in matching network. Therefore, the cascode topology is implemented to overcome this problem especially at microwave or millimeter wave frequencies.

The input and output frequency response is developed from bandpass and band stop filter networks. Figure 3 shows the gain frequencies response of dual band LNA. The operating frequencies of LNA are  $\omega_1$  and  $\omega_2$  for 2.4 GHz and 5.2 GHz respectively while the notch filter frequencies for input and output matching are as  $\omega_3$  and  $\omega_4$ .

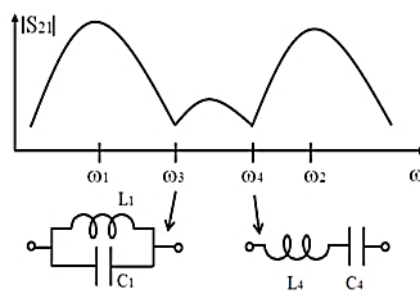


Figure 3. Frequency response of bandpass and band stop filter networks

For the input matching, the equation shows the relationship between notch frequency and resonator of L1 and C1 is given by:

$$L_4 C_4 = \frac{1}{\omega_4^2} \tag{4}$$

The matching network of the input stage is realized by resonator of L2 and also transconductance of M1 ( $C_{gs1}$ ). At  $\omega_1$  of 2.4 GHz frequency,  $L_2$  are function as inductive while  $C_{gs1}$  are capacitive. On the other

hand, at frequency  $\omega_2$  of 5.2 GHz,  $L_2$  and  $C_{gs1}$  are capacitive and inductive, respectively. This will cancelled the imaginary part of input impedance,  $Z_{in}$ . Therefore, the value of  $C_{gs1}$  is decided while the value of inductor  $L_1$ ,  $L_2$  and capacitance  $C1$  are obtain as follows:

$$\frac{\omega_3^2 L_1}{\omega_3^2 - \omega_1^2} = \frac{1}{\omega_3^2 C_{gs1}} - L_2 \quad (5)$$

$$\frac{\omega_3^2 L_1}{\omega_3^2 - \omega_5^2} = L_2 - \frac{1}{\omega_3^2 C_{gs1}} \quad (6)$$

For the output matching stage, the relationship between notch frequency of  $\omega_4$  and resonator that consist of inductor  $L4$  and capacitor  $C4$  is expressed as follows:

$$L_4 C_4 = \frac{1}{\omega_4^2} \quad (7)$$

The resonator is capacitive at  $\omega_1$  while it is inductive at  $\omega_2$ . This condition can be expressed as follows:

$$L_5 (C_5 + C_p) = \frac{1}{\omega_1^2} \quad (8)$$

$$\frac{L_5 L_p}{L_5 + L_p} C_5 = \frac{1}{\omega_2^2} \quad (9)$$

Where  $C_p$  and  $L_p$  is expressed as:

$$C_p = \frac{\omega_1^2 C_4}{\omega_4^2 - \omega_1^2}, \quad L_p = \frac{\omega_2^2 - \omega_1^2}{\omega_4^2 \omega_2^2 C_4}$$

The component parameters including biasing, supply voltage, transistors size, inductors, capacitors and resistors for the proposed dual-band LNA is tabulated in Table 1.

Table 1. Component Parameters for Concurrent Dual-Band 2.4/5.2 GHz LNA

Parameters	Design Value	Parameters	Design Value
M1	172.2 $\mu\text{m}$ / 0.13 $\mu\text{m}$	M2	220 $\mu\text{m}$ / 0.13 $\mu\text{m}$
L1	3.5 nH	C1	0.88 pF
L2	4.5 nH	R1	680 $\Omega$
L3	0.93 nH	C3	1.04 pF
L4	3.9 nH	C4	0.26 pF
L5	0.98 nH	C5	1.96 pF
Cin = Cout	1.0 pF	R2	5.9 k $\Omega$
L <sub>SERIES</sub>	0.56 nH	L <sub>PARALLEL</sub>	2.24 nH

### 3. RESULTS

The proposed design of dual-band LNA is simulated using Cadence SpectreRF simulator at 2.4 GHz and 5.2 GHz in Silterra 0.13- $\mu\text{m}$  technology. The proposed LNA dissipates a total current of 27.4 mA from 1.2 V supply voltage. Figure 4 shows the simulated result of forward gain  $S_{21}$ . The proposed LNA obtains gain of 21.9 dB and 14.2 dB at 2.4 GHz and 5.2 GHz, respectively. The notch frequencies which realized by the bandpass and bandstop filters are 3 GHz and 4.7 GHz, respectively. The gain obtained by the LNA proves that the input and output impedance achieve a maximum power gain transfer and the realization of bandpass and bandstop notch filter can produce a stable peak gain at operating frequency of 2.4 GHz and 5.2 GHz. The gain response also describe the highest gain is achieved at 2.4 GHz compared to 5.2 GHz. This is

due to the presence of inductor L3 at the input of common-gate transistor. The higher value of inductance will limit the gain response of LNA.

The simulated input return loss S11 and output return loss S22 are depicted in Figure 5. The input return loss of -18 dB and -16 dB are achieved at 2.4 GHz and 5.2 GHz, respectively. Meanwhile, the output return loss of -14 dB at 2.4 GHz and -15.8 dB at 5.2 GHz are obtained.

Figure 6 shows the noise figure (NF) simulated result of the proposed LNA. As can be seen, the NFs are 4.1 dB and 3.5 dB at 2.4 GHz and 5.2 GHz, respectively. The basic requirement of noise figure for the common LNA design is 3 dB. Since the LNA is designed by a power matching over a noise matching, it shows that the proposed LNA contribute slightly high in noise compared to design specification. The main reason of the noise contribution by the LNA is due to the high value of inductors use in the proposed design.

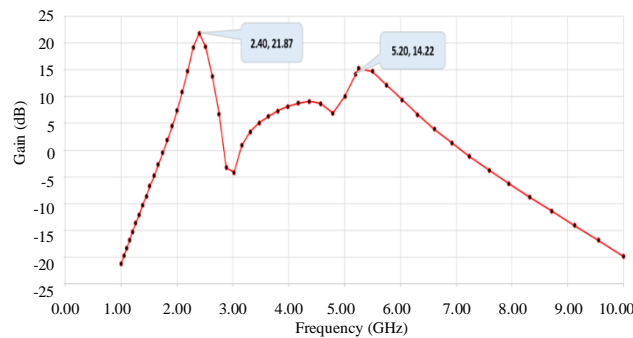


Figure 4. Simulation result of S21

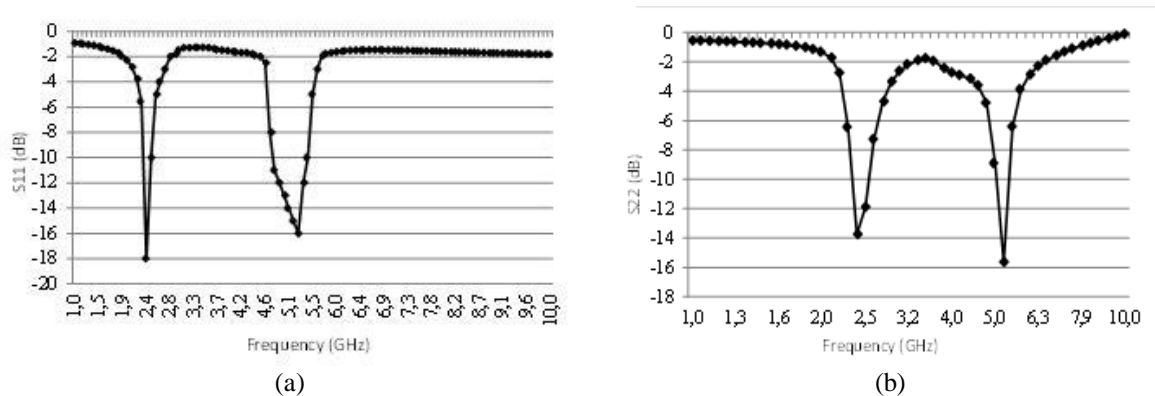


Figure 5. Input and output return loss simulation results: (a) S11, (b) S22

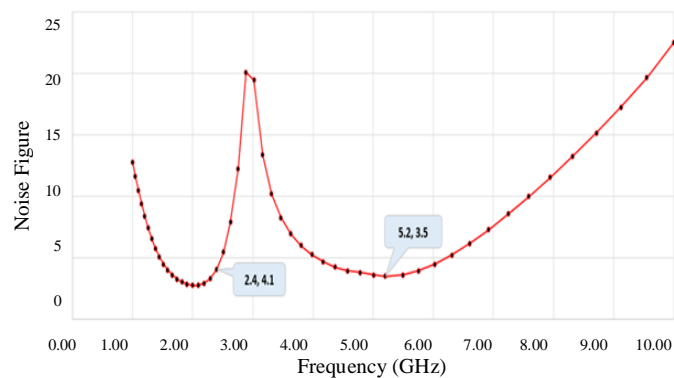


Figure 6. Noise Figure of the proposed dual band LNA

Figure 7 shows the Smith Chart response for the input and output impedance of the proposed LNA. The result shows the impedance of S11 is  $1.3749 + j0.2585$  and  $1.02 + j0.0945$  at 2.4 GHz and 5.2 GHz, respectively. Meanwhile, the impedance of S22 is  $0.7317 - j0.102$  and  $0.7541 + j0.017781$  at 2.4 GHz and 5.2 GHz, respectively.

The simulated third-order intercept points input (IIP3) is shown in Figure 8. The two tone test has been performed for the IIP3 using a periodic steady state (PSS). The input frequency is set at 2.40 GHz / 2.41 GHz and 5.2 GHz / 5.21 GHz with 10 MHz separation. As can be seen, the IIP3 of 7 dBm and 10 dBm at 2.4 GHz and 5.2 GHz are achieved. The stability factor (K-factor) is large that 1 as shown in Figure 9. The proposed LNA is unconditionally stable across the frequency of 1.5 GHz to 6.0 GHz.

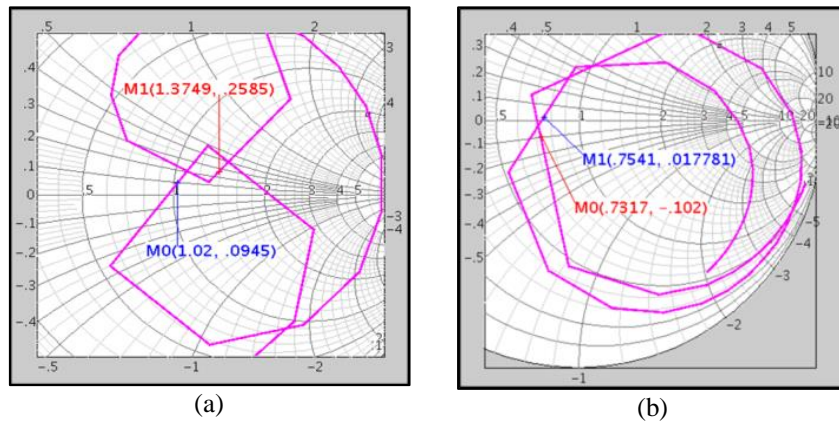


Figure 7. Smith chart response of the proposed LNA: (a) input impedance (S11), (b) output impedance (S22)

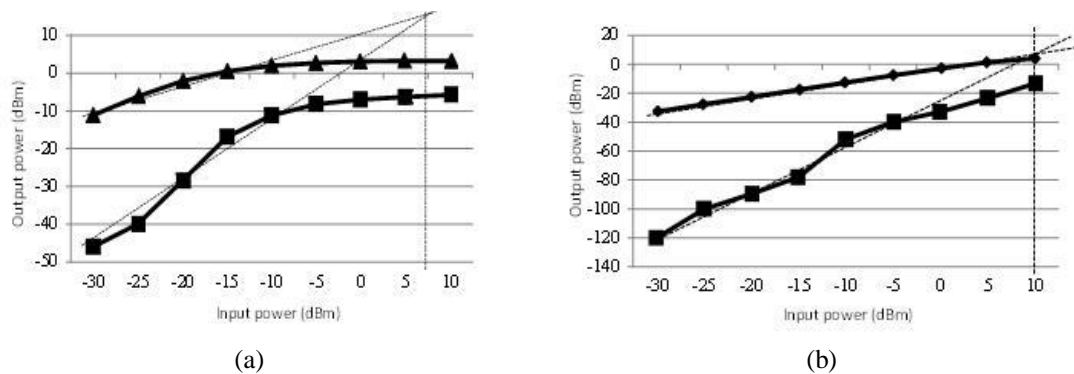


Figure 8. IIP3 of the proposed dual-band LNA (a) 2.4 GHz, (b) 5.2 GHz

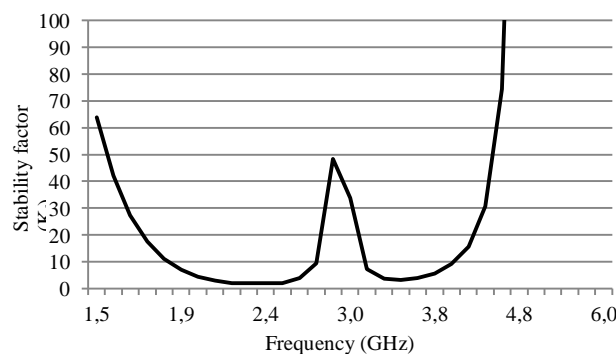


Figure 9. Stability factor (K-factor) of the proposed LNA

Finally, the layout of the proposed dual-band LNA in CMOS 0.13- $\mu\text{m}$  process is presented in Figure 10. The die area including the pads is 1.69  $\text{mm}^2$ . This process has 1-poly and 6-metal layers. The layout is drawn using Virtuoso Layout Editing of Cadence. In the layout, a high metal level (Metal 6) is used for all signal paths for low losses. The signal paths of RF input and output are kept as short as possible between stages to minimize the parasitic effect. Meanwhile, a lower metal level (Metal 1) is used as a ground plane. The input and output pads are arranged in the ground-signal-ground (G-S-G) with the spacing of 100  $\mu\text{m}$  between pads.

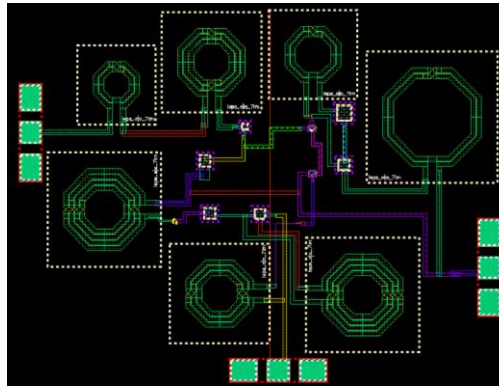


Figure 10. Layout of the proposed LNA in CMOS 0.13- $\mu\text{m}$  technology

Table 2 shows the comparison of performances between the previously published dual-band LNAs and this work. In [12], inductance degenerated cascode structure based on power constrained technique is proposed. A low forward gain is obtained similar with the proposed LNA in [13]. The switched external capacitor is added to the gate-source node of the input transistor to obtain input matching at 2.4/5.2 GHz is presented in [14]. A low gain and moderate input return loss S11 is achieved. In [16], a cascode common source inductive degeneration is proposed with low IIP3.

The proposed LNA in this work obtains high gain and high linearity with the other parameters is comparable. However, the power consumption is slightly high due to large gain has been targeted.

Table 1. Component Parameters for Concurrent Dual-Band 2.4/5.2 GHz LNA

Parameter	[12]	[13]	[14]	[15]	[16]	This work
Technology ( $\mu\text{m}$ )	0.18	0.13	0.18	0.18	0.13	0.13
Supply voltage (V)	1.8	1.2	1.0	1.0	1.2	1.2
Frequency (Hz)	2.6/5.2	2.4/6.0	2.4/5.2	2.4/5.2	2.4/5.2	2.4/5.2
S21 (dB)	15/9.5	9.4/18.9	10.4/11.0	12.9/8.9	19.3/17.5	21.8/14.2
S11 (dB)	-20/-22	-12.6/-21.0	-10/-10	-13.1/-10.5	-16.8/-19.4	-18/-16
NF (dB)	0.65/0.78	2.8/3.8	3.2/3.5	3.7/3.7	3.2/3.3	4.1/5.0
IIP3 (dBm)	0.07/7.04	-4.2/-5.6	-2.9/-3.1	-4/-1	-20.1/-18.1	7/10
Power (mW)	3.6	2.79	2.3	7.6	2.4	32.9
Chip size ( $\text{mm}^2$ )	N/A	0.61	N/A	0.9	N/A	1.69

#### 4. CONCLUSION

A concurrent dual-band CMOS LNA at operating frequency of 2.4 GHz and 5.2 GHz for WLAN applications is presented. The proposed LNA employed cascode common source to obtain high gain using 0.13- $\mu\text{m}$  CMOS technology is successfully designed and simulated. The LC network band-pass and band-stop notch filter at the input and output stages help to shape the frequency response at 2.4 GHz and 5.2 GHz, respectively. The simulation results indicate that the proposed LNA achieves the highest forward gain and input third-order intercept points among the previously published concurrent dual-band CMOS LNAs.



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